WT6615F
USB Power Delivery and Qualcomm® Quick Charge™ 4/4+ Controller

Data Sheet (General Version)

Rev. 1.20

June 2017

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1. General Description

The WT6615F is a highly integrated USB Power Delivery (PD) controller that supports USB PD 3.0 Programmable Power Supply (PPS) specification and Qualcomm® Quick Charge™ 4 or Quick Charge 4+ technologies designed for USB Type-C Downstream Facing Port (Source) charging applications such as power adapters, wall chargers, car chargers, power strip, power banks, and etc.

The WT6615F minimizes external components by integrating USB PD baseband PHY, Type-C detection, shunt regulator, voltage and current monitors, and control circuits of blocking MOSFET, and an 8-bit MCU to allow small form factor and low BOM cost. It supports wide operation voltage range from 3V to 30V without the need of an external LDO. A Multi-Time-Programmable (MTP) ROM is provided for program code and user configuration data.

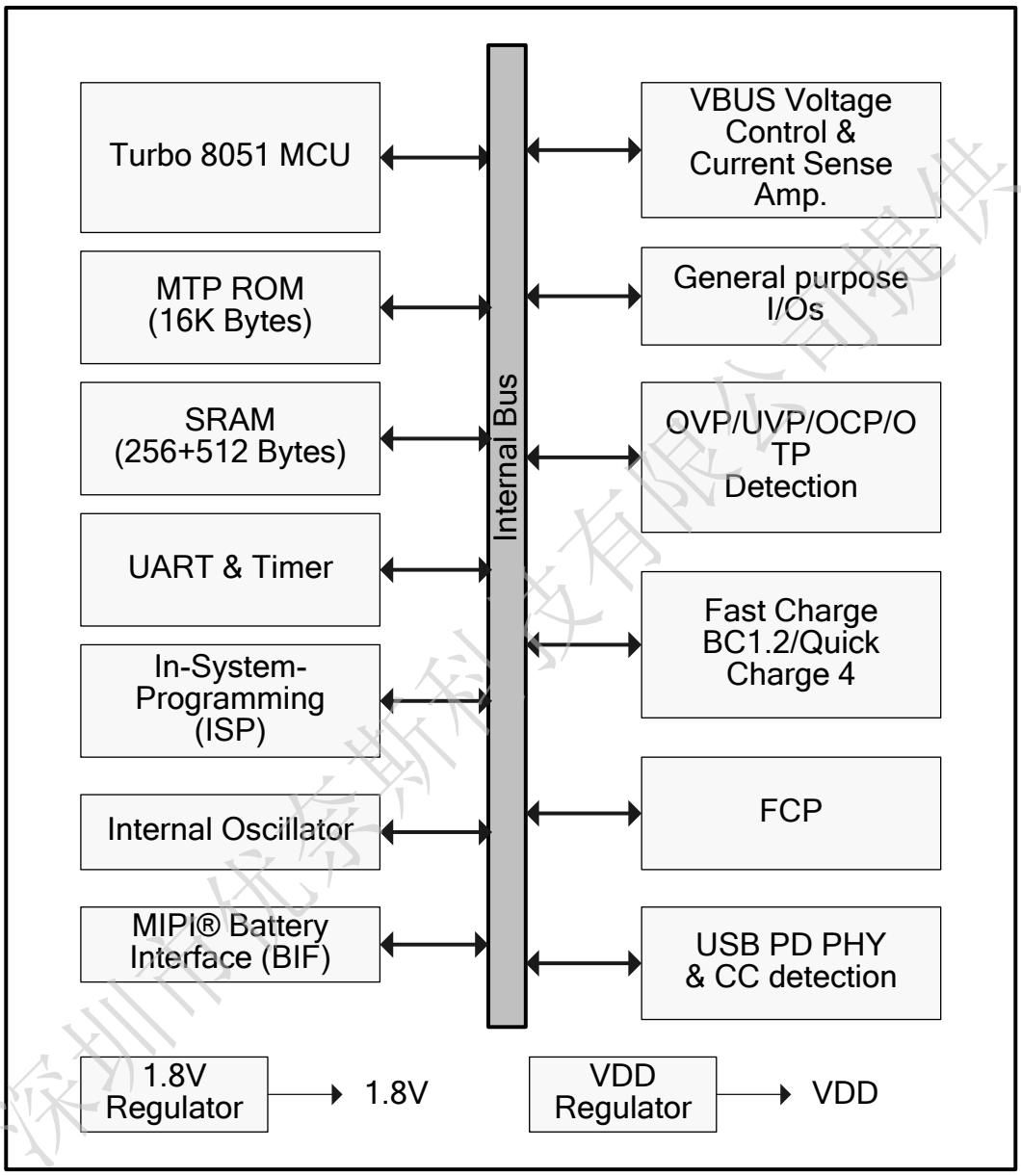
2. Features

- USB Type-C Downstream Facing Port (Source)
- USB Power Delivery Rev. 3.0, Ver. 1.1 baseband communication
- Built-in shunt regulator and support 3V to 20V VBUS output
  - Provide fine tune to increase voltage slightly
  - Constant Voltage
  - Constant Current
- Programmable Over Voltage Protection (OVP), Under Voltage Protection (UVP), Over Current Protection (OCP) and Over Temperature Protection (OTP)
- Low side voltage output current shunt monitor
- Battery Charging specification, Rev. 1.2 (BC1.2) Dedicated Charging Port (DCP), Quick Charge 4, and Quick Charge 4+
- Supports Fast Charge Protocol and Smart Charge Protocol
- Supports MIPI® Battery Interface V1.1 (BIF)
- 10-bit ADC for voltage and current monitoring
- 8-bit MCU
  - implements Power Delivery message protocol and device policy
  - VBUS output control
  - Power supply protection
- Multi-Time-Programmable (MTP) ROM
- External blocking MOSFET control
- Built-in discharge MOS
- Internal RC oscillator
- Internal VDD regulator
- General purpose I/Os
- Serial interface: UART
- Supports power saving mode
- Operating voltage range: 3V ~ 30V
- Operating temperature range: -20°C ~ +105°C
- Package: 16-Pin QFN, 14-Pin SOP

Applications:

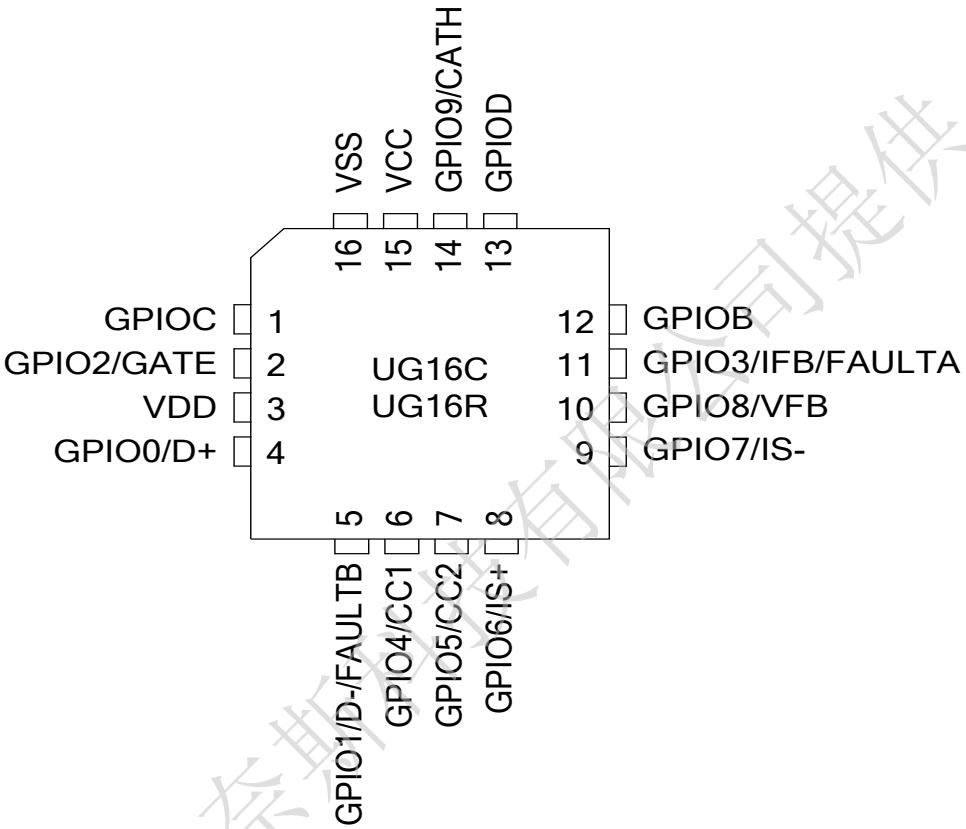
- USB Type-C with Power Delivery power adapters, wall chargers, car chargers, power strip, power banks, and etc.

3. Block Diagram

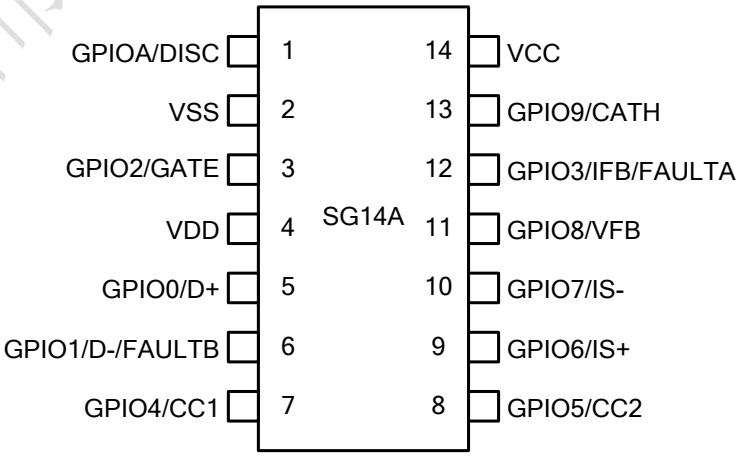


4. Pin Configuration

16-pin QFN



14-pin SOP



4.1 Pin Description

Pin Number		Pin Name	Function	I/O Voltage	Type		Description
QFN16 (UG16C/R)	SOP14 (SG14A)				Input	Output	
15	14	VCC	VCC	HV	-	-	Positive power supply
15	1	GPIOA	GPIOA	HV	TTL	OD	General purpose I/O.
			DISC		-	OD	Discharge
16	2	VSS	VSS	-	-	-	Ground
1		GPIOC	GPIOC	HV	TTL	OD	Serial purpose I/O.
			BIFA		TTL	OD	Serial data
			OTPA		AN	-	Temperature sensing pin
			ADC6		AN	-	ADC input
			P07		TTL	OD	8051 port I/O
2	3	GPIO2	GPIO2	HV	TTL	PP	General purpose I/O.
			GATE		-	PP	Blocking MOS Control
			ADC3		AN	-	ADC input
			P02		TTL	OD	8051 port I/O
3	4	VDD	VDD	LV	-	AN	4.8V regulator
4	5	GPIO0	GPIO0	HV	TTL	OD	General purpose I/O.
			D+		AN	-	D+ for B.C. with USB device side
			BIFD		TTL	OD	Serial data
			ADC7		AN	-	ADC input
			TX		TTL	OD	UART transmitter
			SDAB		TTL	OD	I^2C SDA B path
			P00		TTL	OD	8051 port I/O
5	6	GPIO1	GPIO1	LV	TTL	OD	General purpose I/O.
			D-		AN	-	D- for B.C. with USB device side
			FAULTB		TTL	OD	Fault indication. Outputs low when OVP/OCP.
			ADC2		AN	-	ADC input
			RX		TTL	-	UART receiver
			SCLB		TTL	OD	I^2C SCL B path
			P01		TTL	OD	8051 port I/O
6	7	GPIO4	GP14	HV	TTL	-	General purpose Input
			CC1		CC	PP	USB Type-C Configuration Channel
			OTPD		AN	-	Temperature sensing pin
			ADC10		AN	-	ADC input
7	8	GPIO5	GP15	HV	TTL	-	General purpose Input
			CC2		CC	PP	USB Type-C Configuration Channel
			OTPC		AN	-	Temperature sensing pin
			ADC9		AN	-	ADC input

Pin Number		Pin Name	Function	I/O Voltage	Type		Description
QFN16 (UG16C)	SOP14 (SG14A)				Input	Output	
8	9	GPIO6	GPIO6	LV	TTL	OD	General purpose I/O.
			IS+		AN	-	Positive input of current sensing amplifier.
			SCLA		TTL	OD	I^2C SCL A path
9	10	GPIO7	GPIO7	LV	TTL	OD	General purpose I/O.
			IS-		AN	-	Negative input of current sensing amplifier.
			SDAA		TTL	OD	I^2C SDA A path
10	11	GPIO8	GPIO6	LV	TTL	OD	General purpose I/O.
			VFB		AN	-	Feedback of shunt regulator
			P04		TTL	OD	8051 port I/O
11	12	GPIO3	GPIO3	HV	TTL	OD	General purpose I/O. Open drain output.
			IFB		AN	-	Feedback of shunt regulator
			FAULTA		TTL	OD	Fault indication. Output low when OVE/OCP.
			BIFC		TTL	OD	Serial data
			ADC4		AN	-	ADC input
			P03		TTL	OD	8051 port I/O
12		GPIOB	GPIOB	HV	TTL	OD	General purpose I/O.
			BIFB		TTL	OD	Serial data
			OTPB		AN	-	Temperature sensing pin
			ADC5		AN	-	ADC input
			P06		TTL	OD	8051 port I/O
13		GPIOD	GPIOD	HV	TTL	OD	General purpose I/O
			ADC8		AN	-	ADC input
14	13	GPIO9	GPIO9	HV	TTL	OD	General purpose I/O.
			CATH		-	AN	Cathode of shunt regulator
			P05		TTL	OD	8051 port I/O

Legend: HV = High Voltage (max. 30V), LV = Low voltage (max. 5.5V), OD = Open Drain, PP = Push Pull, AN = analog, TTL = TTL compatible input, CC = USB PD baseband input.

4.2 Pin Function List

Pin Name	Type	Volt	Function									QFN	SOP
			GPIO	Special Function	Fault	BIF	OTP	ADC	UART	I^2C	Port0	16C/R	14A
VCC	P	HV										15	14
GPIOA	I/O	HV	GPIOA	DISC								15	1
VSS	P	-										16	2
GPIOC	I/O	HV	GPIOC			BIFA	OTPA	ADC6			P07	1	
GPIO2	I/O	HV	GPIO2	GATE				ADC3			P02	2	3
VDD	P	LV										3	4
GPIO0	I/O	HV	GPIO0	D+		BIFD		ADC7	TX	SDAB	P00	4	5
GPIO1	I/O	LV	GPIO1	D-	FAULTB			ADC2	RX	SCLB	P01	5	6
GPI4	AI/O	HV	GPI4	CC1			OTPD	ADC10				6	7
GPI5	AI/O	HV	GPI5	CC2			OTPC	ADC9				7	8
GPIO6	AI	LV	GPIO6	IS+						SCLA		8	9
GPIO7	AI/O	LV	GPIO7	IS-						SDAA		9	10
GPIO8	AI/O	LV	GPIO8	VFB							P04	10	11
GPIO3	AIO	HV	GPIO3	IFB	FAULTA	BIFC		ADC4			P03	11	12
GPIOB	I/O	HV	GPIOB			BIFB	OTPB	ADC5			P06	12	
GPIOD	I/O	HV	GPIOD					ADC8				13	
GPIO9	AO	HV	GPIO9	CATH							P05	14	13

5. Functional Descriptions

5.1 MCU and Peripherals

5.1.1 MCU

The WT6615F embeds an 8-bit 1T 8052 compatible microcontroller with 16-bit space addressable and 8-bit data access functions. RAM size is 768 bytes, including 256 bytes of the general 8052 internal RAM and 512 bytes of the external RAM. Program memory is a 16k bytes Multiple Time Programmable (MTP) ROM. In addition, a 256 by 32-bit MTP ROM is provided for user data storage.

5.1.2 Timer/Counter

The MCU contains two general purpose 16-bit timer/counters. Each timer/counter can be configured to operate in a variety of modes as a timer or as an event counter.

5.1.3 Serial Port

Standard 8051 serial port with Mode0~3 is supported. Baud rate range is from 2400 to 115200.

5.1.4 Interrupt

Five Interrupt sources are provided: two 8052 External Interrupts (INT0, INT1), two Timer/Counter Interrupts and one serial port interrupt. The priority of interrupt is programmable for user flexibility.

5.2 VBUS output Control

VBUS output control circuit consists of Constant Voltage (CV) loop and Constant Current (CC) loop, and is illustrated in Fig.5.1.

The constant voltage regulation is implemented by sensing VCC pin via the resistor divider and comparing with internal reference voltage to generate a compensation signal on the CATH pin. The output voltage can be adjusted by programming the resistor, RF2, of the resistor divider. In addition, a current source/sink is added to fine tune the output voltage.

- VBUS voltage 6V ~ 20V, 100mV per step
- VBUS voltage 3V ~ 11V, 20mV per step

The constant current regulation is incorporated with the current sense amplifier. The output current is limited by programming the DAC. When current sense amplifier output is larger than the DAC output, it generates a compensation signal on CATH pin.

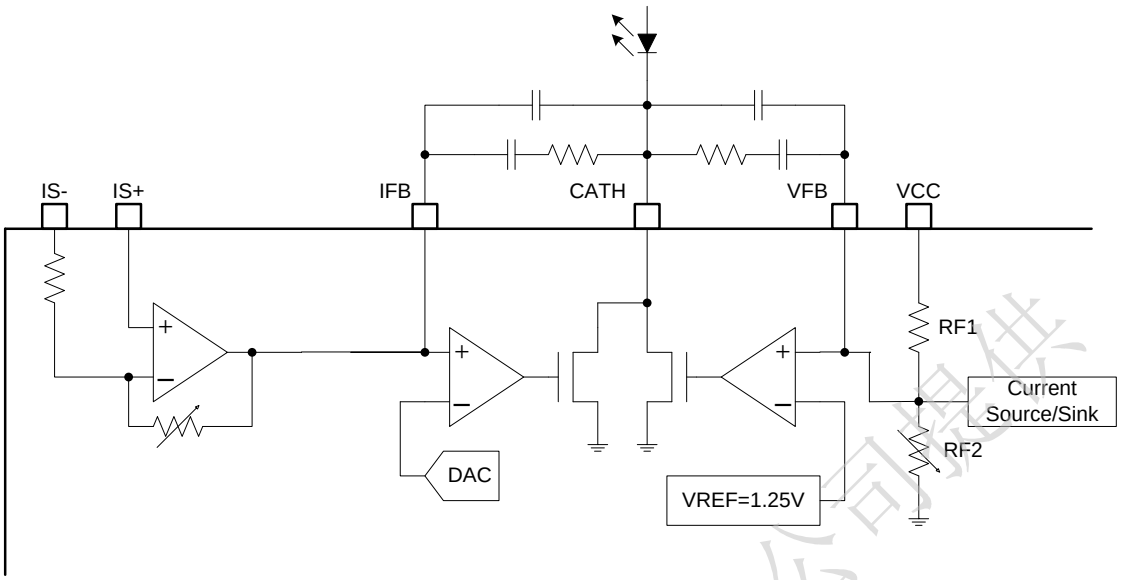


Figure 5.1 VBUS voltage control

5.3 Low Side Current Shunt Monitor and OCP

Load current is sensed by amplifying the voltage drop across the shunt resistor at low side. The gain of amplifier is programmable with 26.6, 53.3, 80, 106.6 and 133.3. MCU can use ADC to read the output of current sense amplifier and perform over current protection (OCP) when load current exceeds protection trip point.

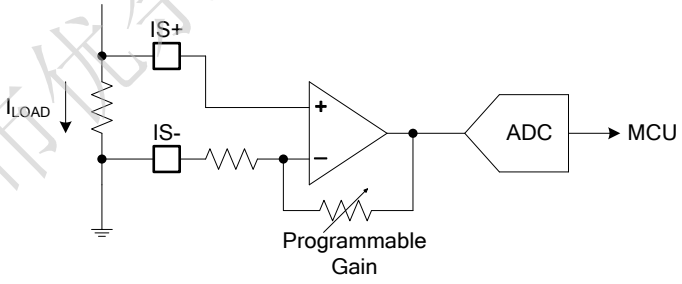


Figure 5.2 Load current monitor

5.4 OVP and UVP

Over Voltage Protection and Under Voltage Protection is implemented by a comparator and a 9-bit DAC (Digital to Analog Converter). When VCC voltage is larger than the OVP trip point or under than the UVP trip point which is set by DAC, GATE pin goes to high level to turn off blocking MOSFET and generates an interrupt to MCU.

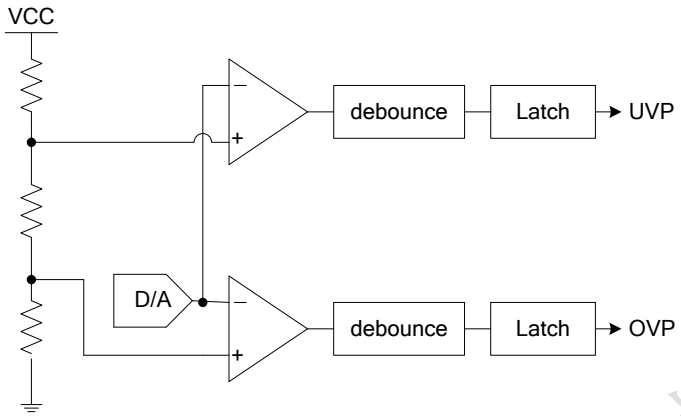


Figure 5.3 OVP and UVP circuit

5.5 Over Temperature Protection

Over Temperature protection (OTP) is implemented by a comparator and a current source. The current source provides a constant current to the selected pin and sense the voltage on the external NTC thermistor. When temperature is larger than the OTP trip point which is set by MCU setting, GATE pin goes to high level to turn off blocking MOSFET and generates an interrupt to MCU. Voltage on the thermistor can also be read through ADC. The NTC thermistor shall use 200Kohm or 100Kohm with B value=4100K. OTP trip point is selectable from 95°C, 105°C, 115°C and 125°C.

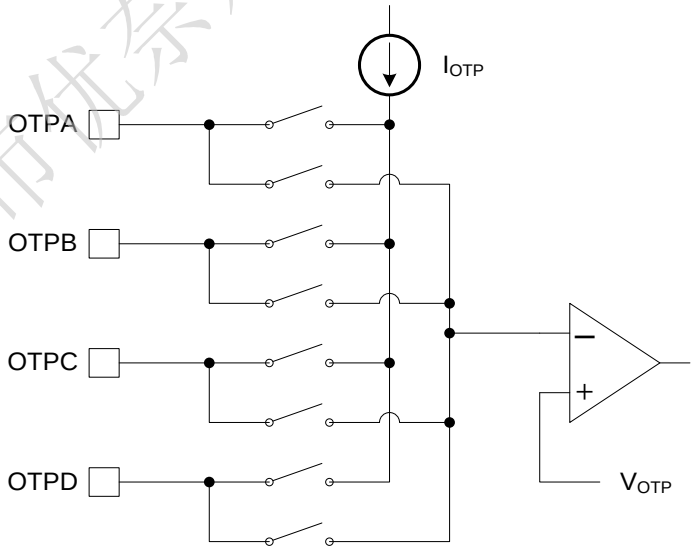


Figure 5.4 Over temperature detection circuit

5.6 ADC

The Analog/Digital Converter (ADC) is SAR type with 10-bit resolution and 12 input channels. It provides a single conversion mode with four selectable conversion rates (1MHz, 500 kHz, 125 kHz, and 31.25 kHz) and a comparator mode. The reference voltage of ADC is 2.5V.

Single Conversion Mode:

The ADC starts to convert by MCU enabling conversion. When the conversion is completed, a flag and an interrupt are generated to inform MCU reading the data.

Voltage Compare Mode:

The input voltage is compared with the DAC and can generate an interrupt either the voltage is higher or lower than the DAC. This function can be used to wakeup MCU when it is stopped during power saving mode.

5.7 Cable Drop Compensation

In order to compensate the voltage drop caused by the cable resistance, a compensation current which is proportional to load current is connected to the FB pin as shown in Fig.5.5

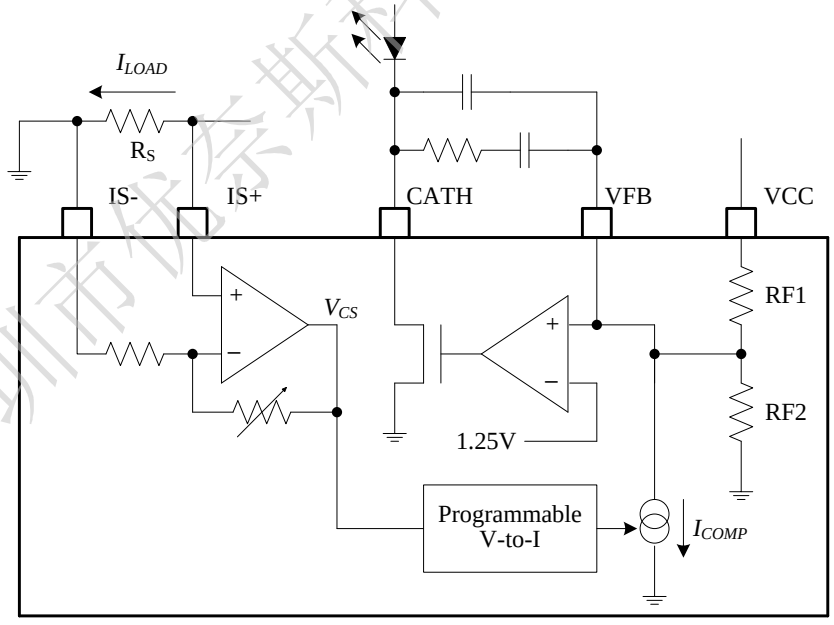


Figure 5.5 Cable drop compensation

5.8 USB Type-C and Power Delivery

5.8.1 USB Type-C CC Termination and connection detect

The termination is implemented by a selectable current source, I_{RP_CC}, which is 80μA, 180μA, or 330μA. By monitoring the voltage on CC1 and CC2, it can detect an UFP is attached or not.

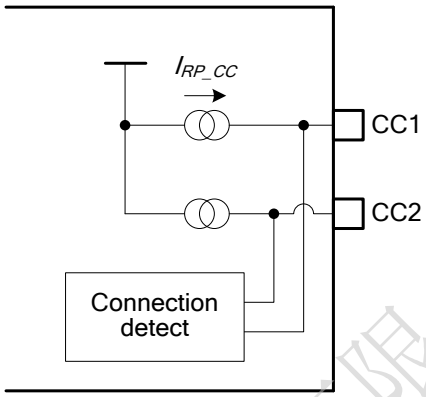


Figure 5.6 CC1 and CC2 pull-up and detection

5.8.2 USB PD PHY

USB PD PHY consists of a pair of transmitter and receiver that communicate across CC wire using Biphase Marking Coding (BMC).

The transmitter performs:

- Receive packet data from the protocol layer
- Calculate and append a CRC
- Encode the packet data including the CRC
- Transmit the Packet (Preamble, SOP, payload, CRC and EOP) across the CC channel using BMC

The receiver performs:

- Recover the clock and lock onto the Packet from the Preamble
- Detect the SOP
- Decode the received data including the CRC
- Detect the EOP and validate the CRC
- If the CRC is valid, deliver the packet data to the protocol layer.
- If the CRC is not valid, flush the received data

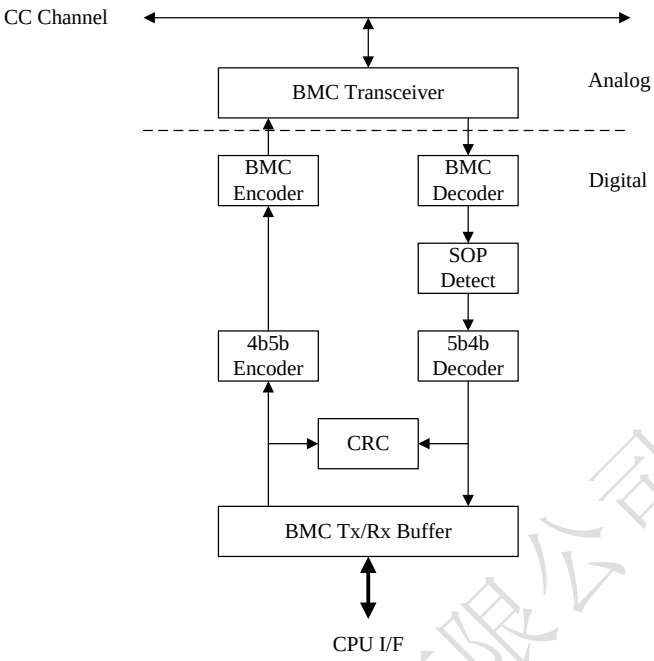


Figure 5.7 USB PD PHY block diagram

5.9 USB BC1.2 and Quick Charge 3.0

The WT6615F supports USB Battery Charging Rev.1.2 (BC1.2) and High Voltage Dedicated Charging Port (HVDCP) Quick Charge 3.0. The HVDCP leverages USB BC1.2 compliant signaling on D+ and D- in order to negotiate voltage requests on VBUS.

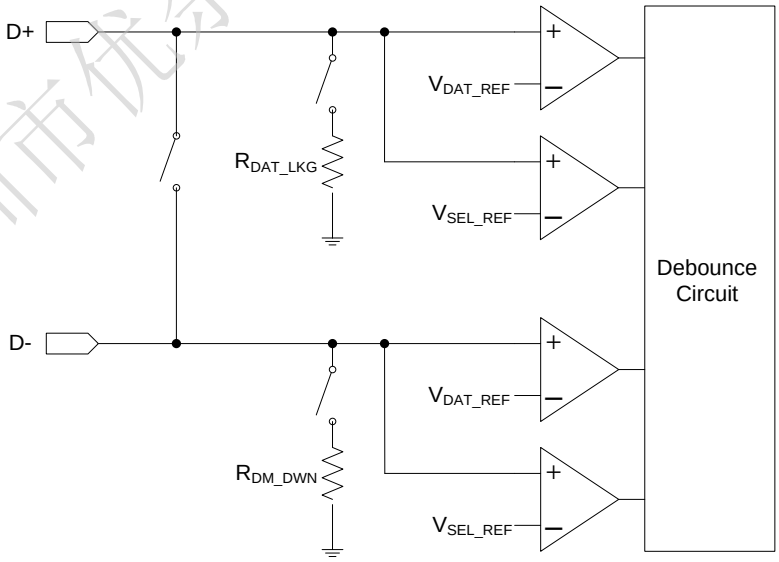


Figure 5.8 BC1.2 and Quick Charge 3.0 block diagram

5.10 Fast Charge Protocol

The Fast Charge Protocol is used to communicate between a mobile device and an adaptive output USB charger. It leverages USB BC1.2 compliant signaling and negotiate voltage and current requests through D- wire. The WT6615F implements a slave mode transceiver which contains transmitter, receiver, receive clock synchronization, parity check and detection of Start of Transfer /End of Transfer/Multi-Byte Transfer.

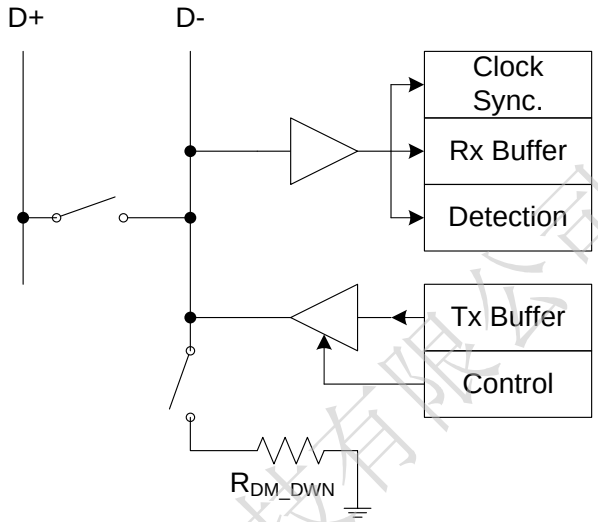


Figure 5.9 FCP block diagram

5.11 BIF Transceiver

The BIF transceiver implements the BIF physical logic. The digital transceiver operates in half-duplex as a BIF master device. It detects parity error using 4-bit-Hamming-15 coding.

5.12 I^2C Interface

The I^2C interface is a two-wire interface which consists of serial data (SDA) and serial clock (SCL). The WT6615F implements slave mode only.

5.13 Discharge

When VBUS transits from a higher voltage level to a lower voltage level, it requires a discharge current to fulfill the transition time specification of USB-PD. There are four transistors can be enabled independently to control discharge time. Care must be taken when discharging with large current at high voltage level.

5.14 Blocking MOSFET Control

In USB-PD application, VBUS should be turn off when the cable is detached. Therefore, a MOSFET switch is required. GATE pin is designed to drive an external PMOS transistor and is controlled by MCU.

5.15 GPIO

All GPIOs can be configured as an input or output except GPI4 and GPI5 are input only. When configured as an output port, it is open drain type.

5.16 Watchdog Timer

Watchdog Timer can be used to detect CPU failures, such as the software deadlock circles caused by noises, voltage disturbance, or power off etc. When the internal counter of the Watchdog Timer overflows, a reset signal will be generated then reset the CPU.

5.17 Reset

There are several reset sources to generate RESET signal:

(1) Power On Reset (POR)
(2) 1.8V regulator Low Voltage Reset
(3) VCC Under Voltage Lockout (UVLO)
(4) VDD Low Voltage Reset
(5) Watchdog Reset
(6) Program Counter Overflow Reset

All reset sources can be enabled/disabled except Power On Reset.

5.18 MTP ROM Programming

MTP ROM can be programmed through CC1 or CC2 pin by using Weltrend's proprietary single wire protocol.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter		Min.	Max.	Units
Supply voltage VCC pin		–0.3	30	V
Input voltage	GPIO0, GPIO2, GPIO3, GPI4, GPI5, GPIO9, GPIOB, GPIOC, GPIOD	–0.3	VCC + 0.3 (max. 30V)	V
	GPIO1, GPIO6, GPIO7, GPIO8	–0.3	5.5	V
Output voltage	GPIO0, GPIO2, GPIO3, GPIO9, GPIOB, GPIOC, GPIOD	–0.3	VCC + 0.3 (max. 30V)	V
	GPIO1, GPIO6, GPIO7, GPIO8, VDD	–0.3	5.5	V
Operating temperature		-40	125	°C
Storage temperature		-55	150	°C

NOTE: Maximum ratings applied to the device are individual stress limit value. Stresses above those listed may cause permanent damage and reliability may be affected.

6.2 Recommended Operating Parameters

Parameter		Condition	Min.	Typ.	Max.	Units
V_{CC_OPR}	Operating voltage		3		30	V
T_{OPR}	Operating Temperature		-20		105	°C

6.3 DC Electrical Characteristics (VCC = 20V, Ta = -20°C ~ +105°C, unless specified)

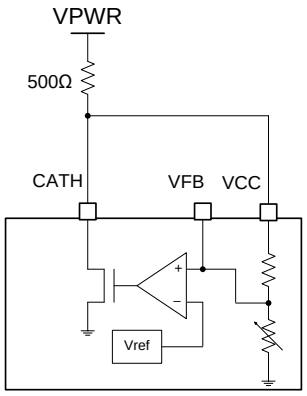
VCC and VDD

Parameter		Condition	Min.	Typ.	Max.	Units
V_{CC}	VCC Operating Voltage		3		30	V
I_{CC_OPR}	VCC Current, normal operating	No load at output and MCU operating @ 10MHz		6		mA
I_{CC_SLEEP}	VCC Current, sleep mode	CC1 pin floating		1	1.2	mA
		CC1 pin 5.1KΩ pull low			1.5	mA
V_{UVLO}	VCC Under Voltage Lockout	VCC rising at Ta = 25°C	2.85		3.5	V
		VCC falling at Ta = 25°C	2.65		2.8	V
		VCC rising at Ta = -20°C ~ +105°C	2.8		3.55	V
		VCC falling at Ta = -20°C ~ +105°C	2.6		2.85	V
V_{DD}	VDD regulator output voltage	I_{DDO} = 0~20 mA		4.8		V

Shunt regulator

Parameter		Condition	Min.	Typ.	Max.	Units
V_{REF}	Reference voltage	V_{CATH} = V_{FB} and I_{CATH} = 1mA Ta = 25°C		1.25		V
		V_{CATH} = V_{FB} and I_{CATH} = 1mA Ta = -20°C ~ +105°C	1.2375	1.25	1.2625	V
V_{OUT}	Regulator output voltage range tolerance*(1)	VPWR = 23V, Ta = 25°C 5V output			±2	%
		VPWR = 23V, Ta = 25°C 6V ~ 20V output			±3	%

*(1) Test circuit of shunt regulator



Over Voltage Protection (OVP)

Parameter		Condition	Min.	Typ.	Max.	Units
N_{DAC}	DAC resolution			9		Bit
INL_{DAC}	DAC INL	Ta= 25°C, V_{REF_DAC} = 2.5V			±2	LSB
DNL_{DAC}	DAC DNL	Ta= 25°C, V_{REF_DAC} = 2.5V			±2	LSB
V_{REF_DAC}	Reference voltage of DAC	Ta = 25°C, VCC = 5V	2.4875	2.5	2.5125	V
R_{DIV}	R divider tolerance	Rdivider = 0.8333, Ta = 25°C			±1	%
E_{OVP}	OVP trip point error	V_{OVP} = 15V, Rdivider = 0.8333 Ta = 25°C			±2.3	%
		V_{OVP} = 15V, Rdivider = 0.8333 Ta = -20°C ~ 105°C			±3.3	%

ADC

Parameter		Condition	Min.	Typ.	Max.	Units
N_{ADC}	ADC resolution			10		bit
INL_{ADC}	ADC INL	Ta = 25°C, V_{REF_ADC} = 2.5V			±5	LSB
DNL_{ADC}	ADC DNL	Ta = 25°C, V_{REF_ADC} =2.5V			±5	LSB
V_{REF_ADC}	Reference voltage of ADC	Ta = 25°C, VCC = 5V	2.4875	2.5	2.5125	V

CC1 and CC2

Parameter		Condition	Min.	Typ.	Max.	Units
V_{OH_CC}	Output high voltage of BMC transmitter		1.05	1.125	1.2	V
V_{OL_CC}	Output low voltage of BMC transmitter		0		0.075	V
V_{IH_CC}	Input high voltage of BMC receiver		0.67		1.45	V
V_{IL_CC}	Input low voltage of BMC receiver		-0.25		0.43	V
Z_{DRIVER_CC}	BMC Transmitter output impedance		33		75	Ω
Z_{BMCRX_CC}	BMC Receiver Input impedance		1			MΩ
I_{RP_CC}	CC1 and CC2 pull-up current	Capability 0.5A @5V	64	80	96	μA
		Capability 1.5A @5V	166	180	194	μA
		Capability 3.0A @5V	304	330	356	μA
V_{Rd_CC}	CC1 and CC2 attachment detection threshold	Capability 0.5A @5V	1.5	1.6	1.65	V
		Capability 1.5A @5V	1.5	1.6	1.65	V
		Capability 3.0A @5V	2.45	2.6	2.75	V

D- and D+

Parameter		Condition	Min.	Typ.	Max.	Units
V_{DAT_REF}	Data detect voltage		0.25	0.35	0.4	V
V_{SEL_REF}	Output selection reference		1.8	2.0	2.2	V
R_{DM_DWN}	D- pull down resistance		14.25	17.5	24.5	KΩ
R_{DCP_DAT}	D+ to D- resistance during DCP mode resistance			30	40	Ω
R_{DAT_LKG}	D+ leakage resistance		300	710	1500	KΩ

GPIO

Parameter		Condition	Min.	Typ.	Max.	Units
V_{OL_GPIO4m}	Output Low Voltage of GPIO1, GPIO6, GPIO7 and GPIO8	I_{OL} = 4 mA			0.4	V
$V_{OL\_GPIO10m}$	Output Low Voltage of GPIO0, GPIO2, GPIO3, GPIO9, GPIOA, GPIOB, GPIOC and GPIOD	I_{OL} = 10 mA			0.4	V
$V_{OH\_GPIO10m}$	Output High Voltage of GPIO2	I_{OH} = 10 mA	V_{CC} -0.4			V
I_{Z_GPIO}	Leakage current of GPIO in Hi-Z				10	μA
V_{IH}	Input high voltage	GPIOA	1.1		4.5	V
		GPIO6, GPIO7, GPIO8	1.4		4.5	V
		GPIO0, GPIO1, GPIO2, GPIO3, GPIO9, GPIOB, GPIOC, GPIOD	1.4		VCC	V
V_{IL}	Input low voltage	GPIOA	0		0.5	V
		Others GPIOx	0		0.8	V

6.4 AC Electrical Characteristics (VCC = 20V, Ta = -20°C ~ +105°C, unless specified)

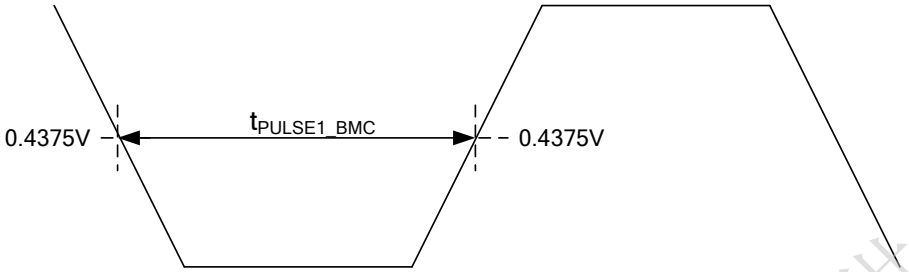
Internal Oscillator

Parameter		Condition	Min.	Typ.	Max.	Units
f_{OSC}	Main oscillator frequency	HFIRC_CLK_SLT=0	9.5	10	10.5	MHz
		HFIRC_CLK_SLT=1	15.2	16	16.8	kHz
f_{LFOSC}	Low frequency oscillator frequency		45.5	65	84.5	kHz

USB-PD BMC Transmitter and Receiver

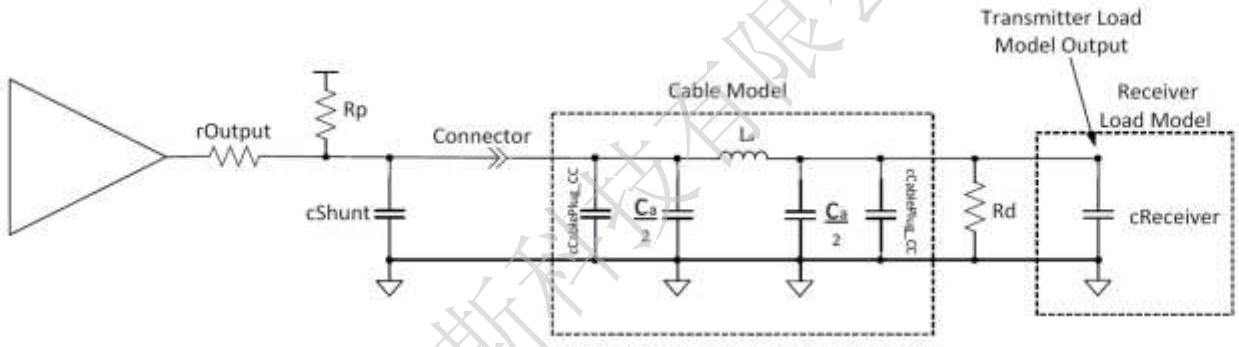
Parameter		Condition	Min.	Typ.	Max.	Units
f_{BMC}	BMC signal bit rate		270	300	330	kHz
t_{RISE_BMC}	BMC signal Tx rise time		300			ns
t_{FALL_BMC}	BMC signal Tx fall time		300			ns
t_{HOLD_BMC}	Time to cease driving the line after the final high-to-low transition		1			µs
t_{IFG_BMC}	Time from the end of last bit of a Frame until the start of the first bit of the next Preamble		25			µs
t_{END_BMC}	Time to cease driving the line after the end of the last bit of the Frame				23	µs
t_{RXFTR_BMC}	BMC receiver bandwidth limiting filter		100			ns
t_{NILDLE_BMC}	Time window for detecting non-idle		12		20	µs
N_{NIDLE_BMC}	Number of transitions to be detected to declare bus non-idle		3			
t_{PULSE1_BMC}	Pulse width of transmitted BMC “ONE” signal*(1)	Ta = 25°C, CC total Capacitance =1010pF *(2,3), CC pin series resistance =47ohm	1.4		1.8	µs

*(1) Pulse width of transmitted BMC “ONE” signal



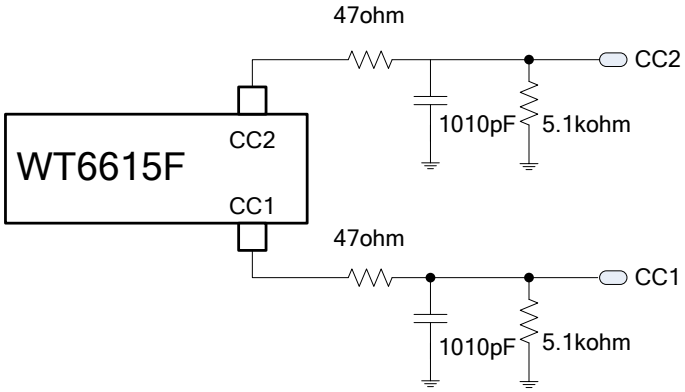
BMC Mark“ONE”

*(2) Reference to USB Power Delivery Specification Revision 3.0. The cShunt=560pF is used and assumes cReceiver is minimum value 200pF, and Cable Model provide 250pF.



Transmitter Load Model for BMC Tx

*(3) Pulse width of transmitted BMC “ONE” signal test circuit



6.5 Thermal Resistance Notice

16-pin QFN

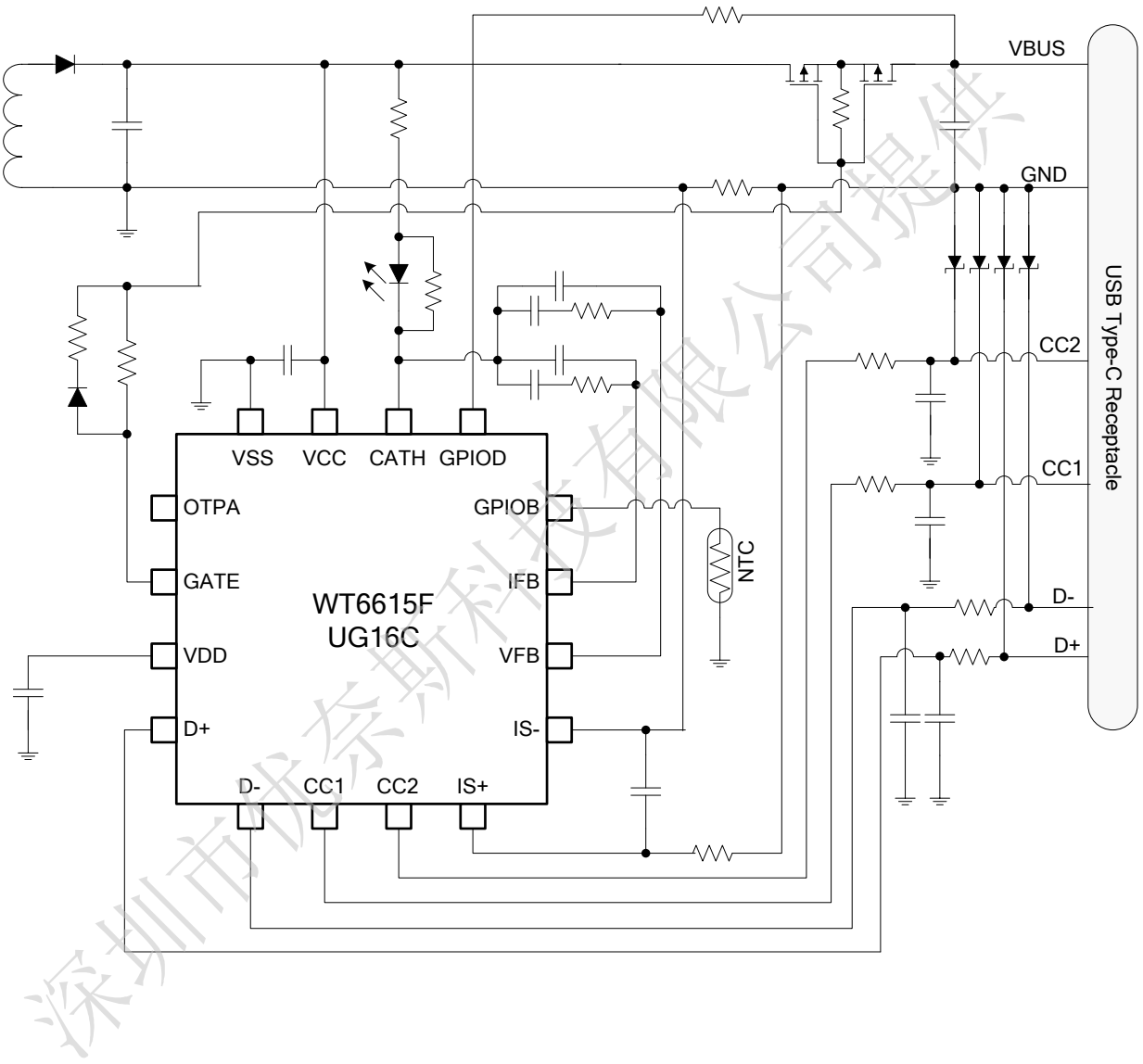
Parameter		Condition	Min.	Typ.	Max.	Units
θ_{JA}	Thermal Resistance (Junction to Air)			47		°C /W
θ_{JC}	Thermal Resistance (Junction to Case)			4.5		°C /W
T_{JMAX}	Maximum Junction Temperature			125		°C

14-pin SOP

Parameter		Condition	Min.	Typ.	Max.	Units
θ_{JA}	Thermal Resistance (Junction to Air)			90		°C /W
θ_{JC}	Thermal Resistance (Junction to Case)			37		°C /W
T_{JMAX}	Maximum Junction Temperature			125		°C

7. Application Circuits

7.1 Travel Charger

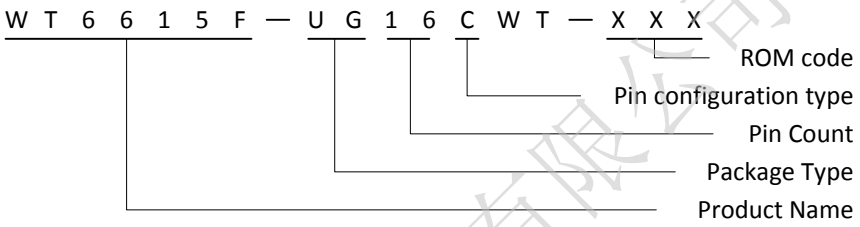


8. Ordering Information

Package Type	Package Outline	Part Number	Ordering Number	Note
16-pin QFN	4mm x 4mm	WT6615F	WT6615F-UG16CWT-XXX	-
16-pin QFN	4mm x 4mm	WT6615F	WT6615F-UG16RWT-XXX	Support Code Write Protection
14-pin SOP	150 mil	WT6615F	WT6615F-SG14AWT-XXX	-

Notes: suffix number number-XXX for difference Firmware code, please refer to Firmware control list.

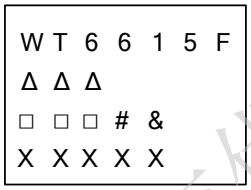
Example



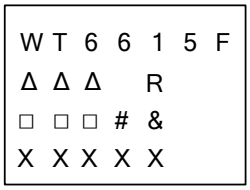
Top Mark

16-pin QFN Top Mark

WT6615F-UG16CWT-XXX



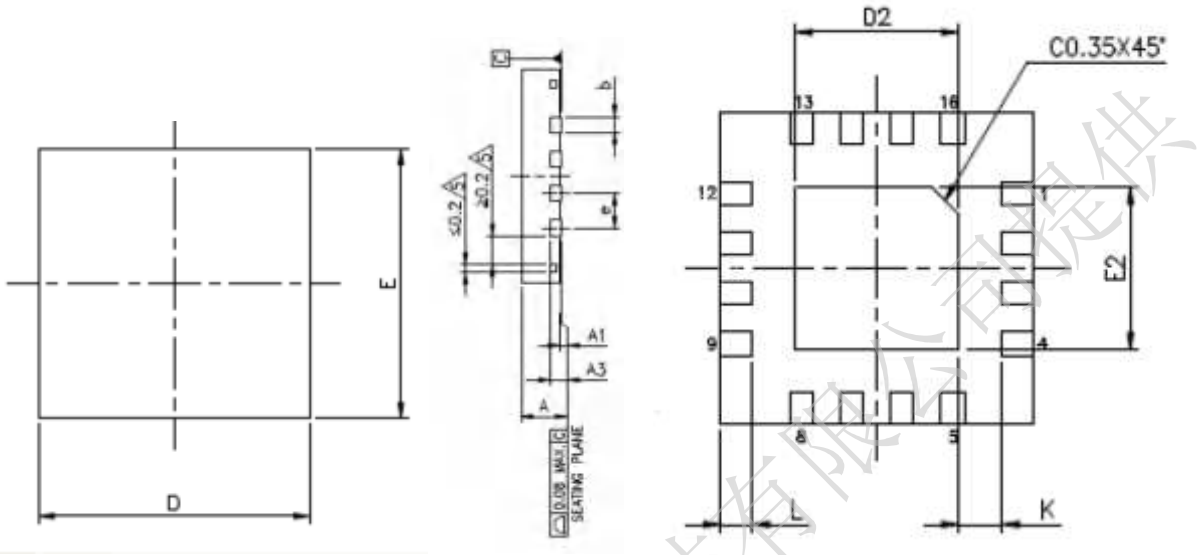
WT6615F-UG16RWT-XXX



Δ	ROM Code
□	Date Code
#	F/W Version Code
&	Pin configuration type
X	Production Tracking code

9. Package Dimension

9.1 16-pin QFN



All dimensions shown in mm

SYMBOL	MIN	NOR	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e		0.65	
K	0.20	-	-
L	0.30	-	0.50
D2	2.00	-	2.80
E2	2.00	-	2.80

NOTE: Dimension “b” applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension “b” should not be measured in that radius area.

9.2 14-pin SOP

All dimensions shown in mm

SYMBOL	MIN.	MAX.
A	-	1.75
A1	0.10	0.25
A2	1.25	-
b	0.31	0.51
c	0.10	0.25
D	8.53	8.74
E	6.00 BSC	
E1	3.81	3.99
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

NOTES :

1. Dimension “D” does not include mold flash, protrusions or gate burrs mold flash. Protrusions or gate burrs shall not exceed 0.15mm.
2. Dimension “E1” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm per side.

10. Revision History

Version	History	Date
1.00	Preliminary	2017/02/21
1.10	1. Update 5.2 VBUS output control description 2. Update Ordering Information	2017/04/18
1.20	1. Add 14pin- SOP package: update “Features”, “Pin Configuration”, “Thermal Resistance Notice”, “Ordering Information” and “Package Dimension” 2. Add Qualcomm Quick Charge 4+ support 3. Update Application Circuits (section 7)	2017/06/13