

Features

- Single stage PFC
- Primary side regulation without Secondary Feedback
- Quasi Resonance (QR) mode with Fly-back topology
- Real-Current control to meet accurate output current
- Flexible current compensation setting in the appointed temperature
- Very less components
- Programmable input AC voltage compensation
- Leading Edge Blanking on CS/FB pin
- Protection Features
 - Building in hysteresis OTP
 - VDD over voltage protection
 - Cycle by cycle current limiting on CS pin
 - Output short to GND protection
 - Output programmable over voltage protection
 - FB and CS pins default

Applications

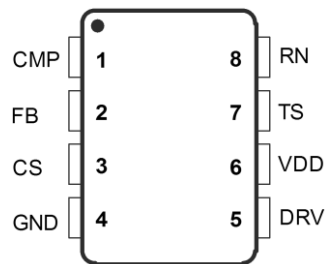
Offline AC/DC Flyback power converters for LED lighting

Typical Application

LZC8620

PSR & PFC LED Driver Controller

Pin Configuration (SOP8)



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD ----- 30V
- Gate pin----- 30V
- other Pins ----- - 0.3V to 6.5V
- Package Thermal Resistance, θ_{JA}
SOP8 ----- 178°C /W
- Junction Temperature -----160°C
- Lead Temperature (Soldering, 10 sec.) -----260°C
- Storage Temperature Range -----55°C to 150°C
- ESD Susceptibility (Note2)
- HBM (Human Body Mode) ----- 2kV
- MM (Machine Mode) -----200V

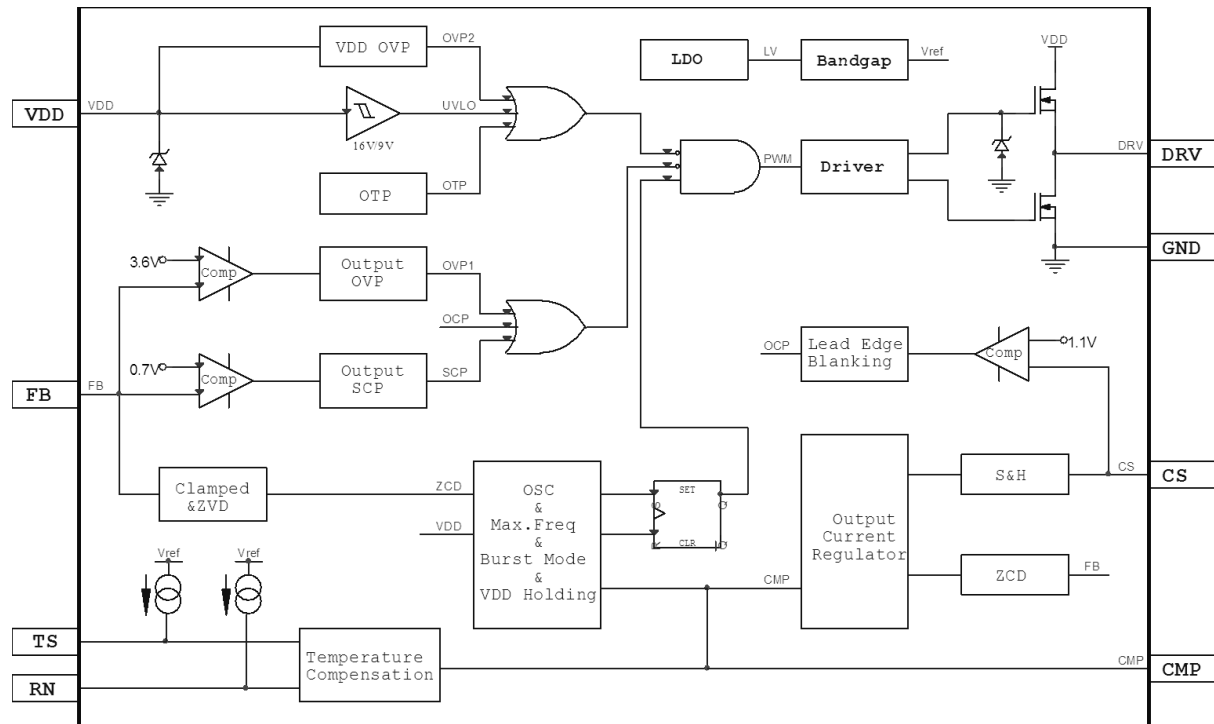
Recommended Operating Conditions (Note3)

- Junction Temperature ----- -40°C to 125°C
- Ambient Temperature ----- -40°C to 85°C
- Supply Input Voltage, VDD ----- 11V to 23V
- VDD capacitor ----- 10uF to 22uF

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Block Diagram



Pin Assignment

Name	I/O	Pin No.	Description
CMP	I	1	Loop compensation for constant current regulation. Output of the OTA. The RC network is placed between it and GND.
FB	I/O	2	Detect output diode zero current to regulate output current. Connected to a resistor divider for sensing the reflected voltage from auxiliary winding.
CS	I	3	Current sense pin, a resistor connects to sense the MOSFET current.
GND	POWER	4	Power Ground.
DRV	O	5	Totem-pole output to drive the external power MOSFET, Maximum Voltage is internally clamped to 16V.
VDD	POWER	6	Power Supply.
TS	I/O	7	Temperature compensation point setting.
RN	I/O	8	Connect NTC resistor for temperature compensation.

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Electrical Characteristics

$V_{DD}=15V$, $T_A=25^{\circ}C$, unless otherwise specified

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
VDD Supply Voltage						
I _{ST}	Startup current	VDD=VDD _{ON} -0.3V		5	10	μA
I _{OC}	Operating current of VDD	C _{DRV} =1.5nF		1.5		mA
VDD _{ON}	VDD Turn on threshold		18.1	19.8	21.5	V
VDD _{OFF}	VDD Turn off threshold		7.0	8.0	9.0	V
VDD _{OVP}	Over voltage threshold			27		V
CMP						
V _{REF}	Reference voltage for OTA input		247.5	253.0	258.5	mV
I _{CMP_SINK}	CMP maximal sink current			106.6		uA
I _{CMP_SOURCE}	CMP maximal source current			32		uA
V _{CMP_MAX}	CMP max. voltage			3.6		V
FB						
V _{FB_SINK}	FB voltage when sink current	2mA sink current		6		V
V _{FB_SOURCE}	FB voltage when source current	4mA source current	-150	0	+150	mV
V _{FB_ZCD}	FB zero voltage detect			0.5		V
V _{FB_OVP}	FB voltage when Output OVP			3.6		V
V _{FB_SCP}	FB voltage when trigger SCP			0.7		V
CS						
V _{CS_LIM}	Cycle by Cycle current limited on CS	FB=0V	0.9	1.1	1.3	V
ΔI _{CS} / ΔI _{FB}	Current compensation with FB source current	R _{CS} =1kΩ		30		mV/mA
T _{BK_CS}	Leading-Edge Blanking Time		300	400	500	nS
TS						
I _{TS}	Reference current	R _{TS} =10kΩ	50	100	200	uA
V _{TS_Max}	TS maximum voltage	Open circuit		3.6		V

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RN						
I_{RN}	NTC monitoring current	$R_{RN}=10k\Omega$	50	100	200	μA
V_{RN_Max}	RN maximum voltage	Open circuit		3.6		V
K	Current compensation point	$R_{TS}=K \cdot R_{RN}$	1.23	1.25	1.27	N
DRV						
T_R	Rise Time	$C_L=1nF$	150	200	220	nS
T_F	Fall Time	$C_L=1nF$	80	100	120	nS
V_{DRV_CLAMP}	DRV clamped voltage			16		V
Oscillator						
F_{MAX}	Maximal Frequency			90		kHz
T_{MAX_ON}	Maximal on time			30		μS
T_{MAX_OFF}	Maximal off time			40		μS
T_{MIN_OFF}	Minimal off time			1.5		μS
Over Temperature Protection						
T_{SD}	OTP protection temp.		140	150	160	$^{\circ}C$
T_{SD_RE}	OTP Release temp.		110	120	130	$^{\circ}C$

- Note 1.** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
- Note 2.** Devices are ESD sensitive. Handling precaution is recommended.
- Note 3.** The device is not guaranteed to function outside its operating conditions.

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Operation

The LZC8620 is a primary side control offline LED controller that incorporates all the features for high performance LED lighting. LED current can be accurately controlled with the real current control method from the primary side information. Active Power Factor Correction (PFC) is included to eliminate the unwanted harmonic noise injected onto the AC line.

Startup

During start-up, the current can charge up the VDD hold capacitor. the turn-on and turn-off thresholds of LZC8620 are approximately 19.8V and 8V respectively. The 11.8V hysteresis voltage is implemented to prevent shutdown from a voltage dip during start-up.

Quasi Resonance mode (QRM)

During the external power MOSFET on time (T_{ON}), the rectified input voltage is applied across the primary side inductor (L_m) and the primary current increases linearly from zero to the peak value (I_{PK}). When the external power MOSFET turns off, the energy stored in the inductor forces the secondary side diode to be turn-on, and the current of the inductor begins to decrease linearly from the peak value to zero. When the current decreases to zero, the parasitic resonant of inductor and all the parasitic capacitance makes the power MOSFET drain-source voltage decrease, this decreasing is also reflected on the auxiliary winding. The zero-current detector in FB pin generates the turn on signal of the external MOSFET when the FB voltage is lower than 0.5V and ensures the MOSFET turn on at a valley voltage.

As a result, there are virtually no primary switch turn-on losses and no secondary diode reverse-recover losses. It ensures high efficiency and low EMI noise.

Active Power Factor Correction (APFC)

LZC8620 is designed with quasi-resonance and constant on time T_{on} to achieve high power factor under normal operation. The on time of LZC8620 vary with input AC voltage $V_p \sin \omega t$ and load condition and its value is constant basically because of very large loop compensation capacitance on CMP pin. According to following equations,

$$I_{L-peak} = \frac{V_p \sin \omega t}{L_m} \times T_{on} \quad I_{L-avg} = \frac{V_p \sin \omega t}{2 \times L_m} \times T_{on}^2 \times f_{osc}$$

The peak current I_{L-peak} and average current I_{L-avg} of transformer will be shaped as AC input sinusoid too because T_{on} and f_{osc} both are constant and then high power factor can be achieved.

Real Current Regulator without Secondary Feedback

The proprietary real current control method allows the LZC8620 to accurately control the secondary side LED current from the primary side information. The output LED mean current can be calculated approximately as:

$$I_{OUT} = \frac{1}{2 \times R_{CS}} \times V_{REF} \times \frac{N_p}{N_s}$$

Where I_{OUT} is the secondary output current of LED, V_{REF} is the inner reference voltage. N_p is number of turns of primary winding and N_s is number of turns of the secondary winding.

Auto Starter

The LZC8620 integrates an auto starter, the starter starts timing when the MOSFET is turned on, if FB fails to send out another turn on signal after 30 μ s, the starter will automatically send out the turn on signal which can avoid the IC unnecessary shut down by FB missing detection.

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Minimal Off Time

The LZC8620 operates with variable switching frequency. The frequency is changing with the input instantaneous line voltage. To limit the maximum frequency and get a good EMI performance, LZC8620 employs an internal minimum off time limiter—1.5μs, show as figure.

Leading-Edge Blanking for CS pin

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance discharging at MOSFET turning on, an internal leading edge blanking (LEB) unit is employed between the CS Pin and the current comparator input. During the blanking time, the path, CS Pin to the current comparator input, is blocked. Figure shows the leading edge blanking.

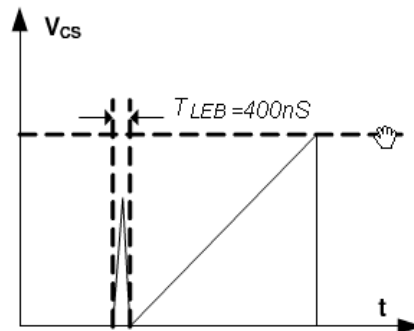


Fig 1

Output over Voltage Protection

Output over voltage protection can prevent the components from damage in the over voltage condition. The positive plateau of auxiliary winding voltage is proportional to the output voltage. The OVP uses the auxiliary winding voltage instead of directly monitoring the output voltage. Once the FB pin voltage is higher than 3.6V, the OVP signal will be triggered and latched, the gate driver will be turned off and the IC work at quiescent mode, the VDD voltage dropped below the UVLO which will make the IC shut down and the system restarts again. The output OVP setting point can be calculated as:

$$V_{OUT_OVP} \approx 3.6 \times \frac{N_S}{N_{AUX}} \times \frac{R_{FBH} + R_{FBL}}{R_{FBL}}$$

V_{OUT_OVP}Output over voltage protection value

N_{AUX}the auxiliary winding turns

N_Sthe secondary winding turns

Current Limit

The current limit circuit senses the current of inductor by CS pin. When this current exceeds the internal threshold, typical is 1.1V, the power MOSFET is turned off for the remainder of that cycle.

Leading-Edge Blanking For FB Pin

As shown in Fig1, when the power MOSFET is turned off, a damping voltage spike will occur at FB pin due to parasitic capacitance of power MOSFET and leak inductor of transformer. An internal leading edge blanking (LEB) was introduced to filter this noise.

Output Short Circuit Protection

When the output short circuit happens, the positive plateau of auxiliary winding voltage is also near zero. The IC will shut down and restart again once FB voltage falls below 0.7V and lasts for about 16mS.

Thermal Shut Down

The thermal shutdown circuitry senses the die temperature. The threshold is set at 150°C typical with a

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25°C hysteresis. When the die temperature rises above this threshold (150°C), the LZC8620 turn off the power MOSFET by DRV and remains turning off until the die temperature falls by 25°C, at which point it is re-enabled.

VDD over Voltage Protection

LZC8620 provides an over voltage protection circuit for VDD pin. The GATE output will shut down once the VDD voltage exceeds 27V (typical value), the IC would restart until VDD drops to 8.0V.

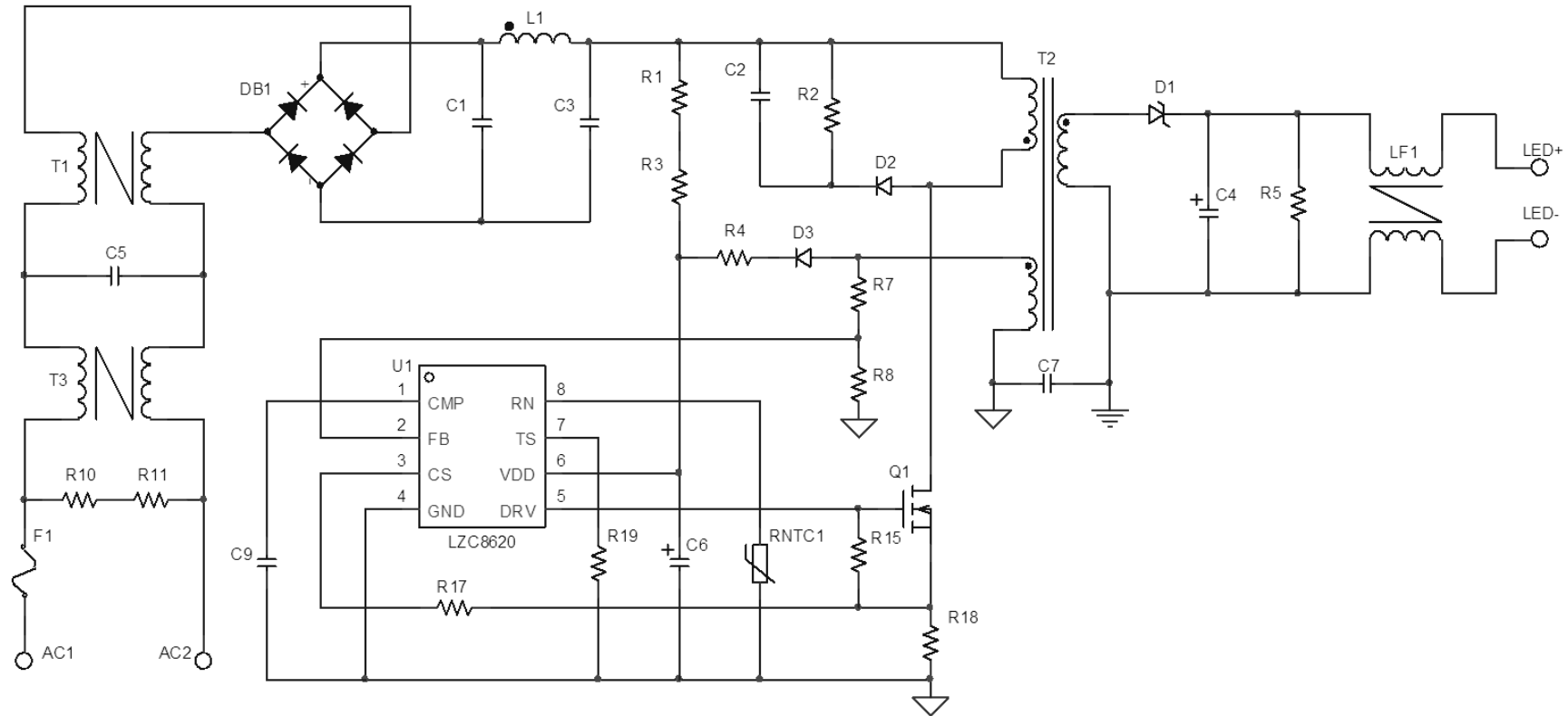
Fault protection

There is several default protections were integrated in the LZC8620 to prevent the IC from being damaged which including FB pin open or short, CS pin open.

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Reference Application Schematic

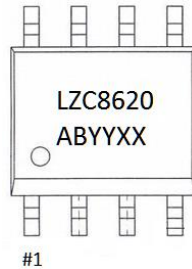


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Ordering & Marking Information

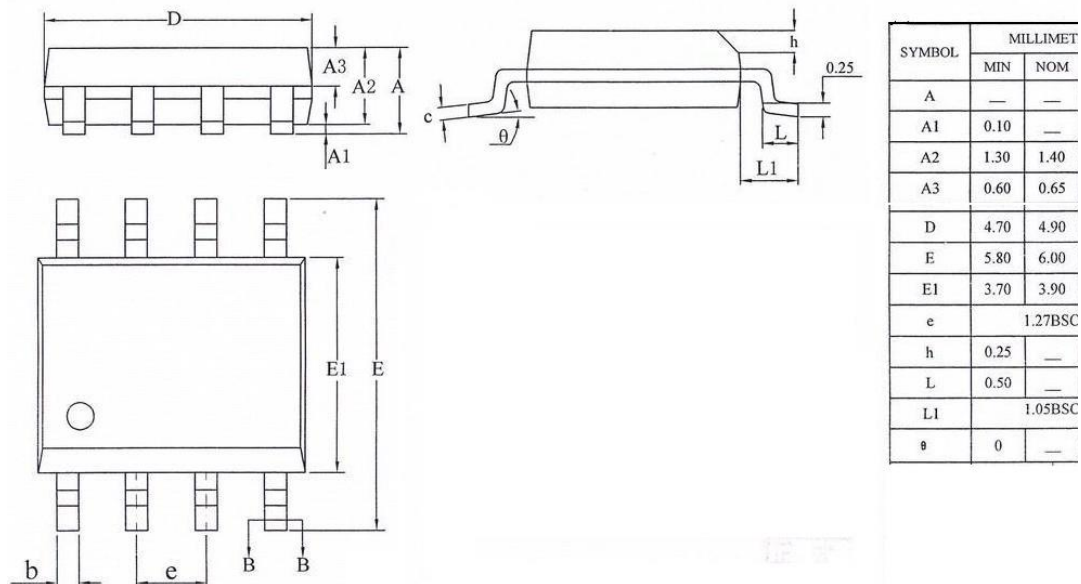
Device Name: LZC8620 for SOP8



LZC8620

ABYYXX: AB for Assembly house, YYXX for Date code

Package information



Compliant to JEDEC Standard MS12F

Controlling dimensions are in inches; millimeter dimensions are for reference only

This product is RoHS compliant and Halide free.

Soldering Temperature Resistance:

[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1

[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; package can withstand 10 s immersion < 270°C

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include inter-lead flash or protrusion. Inter-lead flash or protrusion shall not exceed 0.25 mm per side. D and E1 dimensions are determined at datum H. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outer most extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and inter-lead flash, but including any mismatch between the top and bottom of the plastic body.