GENERAL DESCRIPTION

OB2733x is a highly integrated current mode PWM controller with a 650V GaN FET integrated. It is optimized for high performance, low EMI, low standby power consumption and wide output voltage range PD adapter solutions, together with PD secondary controller, such as OB2621. The controller is as well compatible with cost effective offline flyback converter applications covering a wide output range.

At full load conditions, it operates in the valley switching QR mode both in the low line input and high line input. When the loading goes low, it operates in PFM mode for high power conversion efficiency. When the load is very small, the IC operates in 'Extended Burst Mode' to minimize the standby power loss. As a result, high conversion efficiency can be achieved in the whole loading range. In addition, at high AC line input conditions, it operates in a forced quasi-resonance (QR) valley switching mode with On-Bright proprietary technology for excellent EMI performance.

OB2733x offers complete protection including cycle-by-cycle current limiting (OCP), over load protection (OLP), internal over temperature protection (OTP), output short protection (SCP), output and VDD over voltage protection. Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 20KHz is minimized to avoid audio noise during operation.

OB2733x is offered in EASOP7 package.

FEATURES

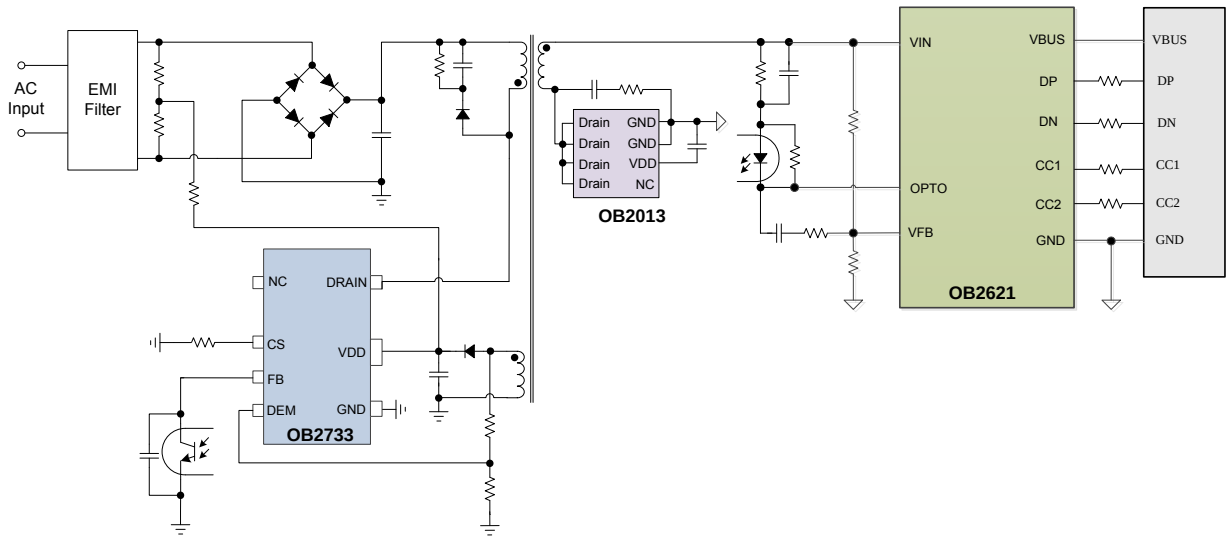
- Multi-Mode Operation
  - 110KHz maximum clamping frequency in QR mode @ high line voltage
  - 25KHz minimum clamping frequency in QR mode @ high line voltage
  - 130KHz maximum clamping frequency in QR mode @ low line voltage
  - 70KHz minimum clamping frequency in CCM mode @ low line voltage
  - Valley switching operation @ Green mode
  - Burst Mode @ Light Load & No Load
- Forced valley switching for EMI optimization
- Extended burst mode control for improved efficiency and low standby power
- Power on soft start reducing MOSFET Vds stress
- Low operating current at no/light load
- Audio noise free operation
- Comprehensive auto-recovery protection
  - VDD under voltage lockout with hysteresis (UVLO)
  - Cycle-by-cycle over current protection (OCP)
  - Overload protection (OLP)
  - Internal over temperature protection (OTP)
  - VDD over voltage protection
  - Output over voltage protection
  - Output short protection (SCP)
  - Output diode short protection

APPLICATIONS

Offline AC/DC flyback converter for

- High power density PD adapters

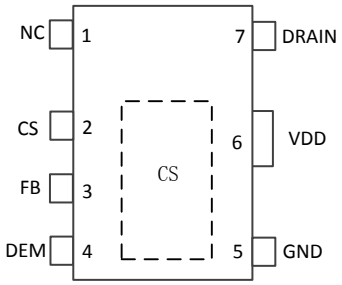
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The OB2733x is offered in EASOP7 package, shown as below.



Ordering Information

Part Number	Description
OB2733VCTP-V	EASOP7, Halogen-free, Tube
OB2733VCTPA-V	EASOP7,Halogen-free, T&R

Package Dissipation Rating

Package	RθJA(℃/W)	RθJC(℃/W)
EASOP7	70	8

Recommended operating condition

Symbol	Parameter	Range
VDD	VDD Supply Voltage	9.5 to 56.5V

Absolute Maximum Ratings

Parameter	Value
DRAIN Voltage	-0.3 to 650V
Transient DRAIN Voltage	-0.3 to 800V Note2
VDD DC Supply Voltage	60V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
DEM Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Min/Max Storage Temperature Tstg	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Note2: The transient DRAIN voltage is relaxed to 800V for surge ratings during non-repetitive events that are<200us and repetitive events that are<100ns.

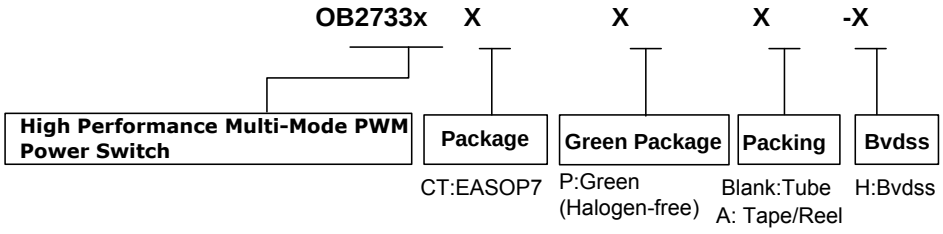
Note3: The negative voltage spike amplitude is relaxed to -1V under the condition that spike duty cycle is in less than 5%, or its equivalent average current is in less than 1mA.

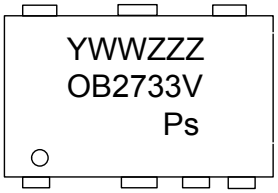
Output Power Table

Product	230VAC±15% Adapter[1]	85-265VAC Adapter[1]
OB2733VCTP-V	25	20

Note: Maximum practical continuous power in an adapter design with sufficient CS pattern as a heat sink, at 40℃ ambient.

Marking Information



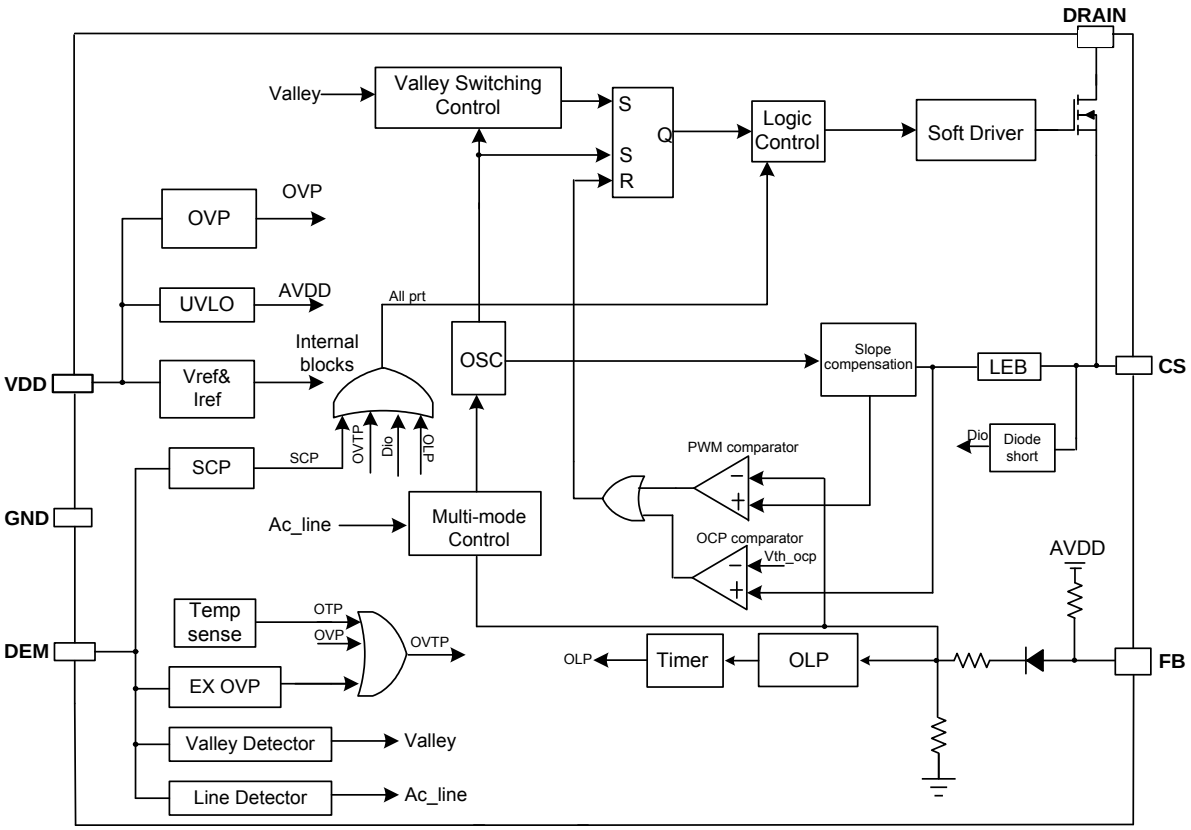


Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
V:Character Code
P:Halogen-free
s:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin NO.	Pin Name	I/O	Description
1	NC		No Connected
2	CS	I	Current sense input
3	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at CS pin
4	DEM	I	Multiple functions pin. Connecting two resistors from Vaux to ground can adjust output OVP trigger voltage, SCP trigger voltage, line voltage detection.
5	GND	P	Ground
6	VDD	P	Power Supply
7	DRAIN	I	GaN FET Drain Pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(T_A = 25℃, VDD=18V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD)						
I startup	VDD Start up Current	VDD=UVLO(OFF)-1V, measure leakage current into VDD		3	5	uA
I_VDD_Operation	Normal Operation Current	V_{FB}=3V, CL=1nF		2.5	3.3	mA
I_VDD_Burst	Burst Operation Current	V_{FB}=0.5V, CL=1nF		0.45	0.60	mA
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		15.5	16.5	17.5	V
UVLO(HOLD)	VDD Holdup Enter Voltage to Turn on Gate	V_{FB}=0.5V	7.9	8.5	9.1	V
UVLO(ON)	VDD Under Voltage Lockout Enter		7.1	7.7	8.3	V
VOVP	Over voltage protection voltage	FB=3V Ramp up VDD until gate clock is off	57	58.5	60	V
Feedback Input Section(FB Pin)						
V_{FB}_Open	V_{FB} Open Loop Voltage		5.5	5.9	6.3	V
Avcs	PWM input gain ΔVFB/ΔVCS			5.5		V/V
Ton_max	Max Ton time @ VDD=18V, VFB=3V,VCS=0V	DEM=2V		10.7		us
Vref_green	The threshold enter green mode			2.2		V
Vref_burst_H	The threshold exit burst mode			1.25		V
Vref_burst_L	The threshold enter burst mode			1.15		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		270		uA
Z_{FB}_IN	Input Impedance			20		KΩ
V_{TH}_Openloop	The open loop FB Threshold Voltage			4.8		V
T_D_ Openloop	The open loop protection debounce Time		50	60	70	ms
Current Sense Input(CS Pin)						
SST_CS	Soft start time of CS threshold			2.5		ms
T_blanking	Leading edge blanking time			230		ns
T_D_OC	Over Current Detection and Control Delay	From Over Current Occurs till the gate driver output starts to turn off		50		ns

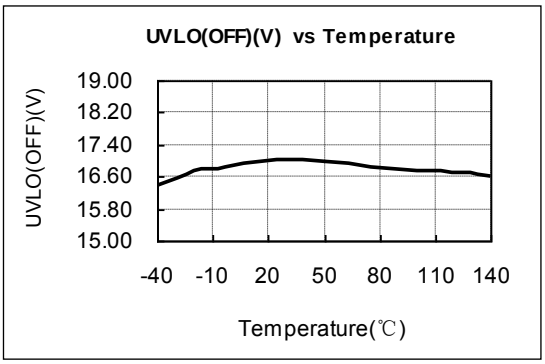
Vth_ocp	Internal Current Limiting Threshold Voltage with zero duty cycle		0.28	0.3	0.32	V
Vth_ocp_clamp	OCP CS voltage clamper		0.34	0.36	0.38	V
Oscillator						
Fosc_max_QR_L	Average max clamp oscillation frequency in QR mode	VDD=15V,FB=3V,Vac <150V	120	130	140	KHz
Fosc_max_QR_H	Average max clamp oscillation frequency in QR mode	VDD=15V,FB=3V,Vac >165V	100	110	120	KHz
∆f_OSC_max_QR	Max clamp oscillation frequency jittering			±6		%
Fosc_min_CCM_L	Min clamp oscillation frequency in CCM mode	VDD=15V,FB=3V,Vac <150V, DEM=2V		70		KHz
Fosc_min_QR_H	Min clamp oscillation frequency in QR mode	VDD=15V,FB=3V,Vac >165V, DEM=2V		25		KHz
∆f_OSC_CCM	Min clamp oscillation frequency jittering			±6		%
F_shuffling	Shuffling frequency			240		Hz
F_Burst	Burst Mode Switch Frequency			25		KHz
DEM pin						
Iref_AC_H	The detected high AC line current threshold of auxiliary windings during power MOSFET turned on			350		uA
Iref_AC_L	The detected low AC line current threshold of auxiliary windings during power MOSFET turned on			320		uA
Voutput_ovp	Voltage threshold for adjustable output OVP		2.85	3.0	3.15	V
Td_ output_ovp	Output voltage OVP debounce time			8		cycles
Vref_scp	SCP threshold			0.4		V
Td_ scp	SCP debounce time			8		cycles
Td_dis_scp	SCP detect after startup			15		ms
Tsp	Output voltage Sampling Blanking Time	FB>2.2V		2.2		us
		FB<1.5V		1.5		us
On Chip OTP						
OTP Level				140		℃
OTP exit				125		℃

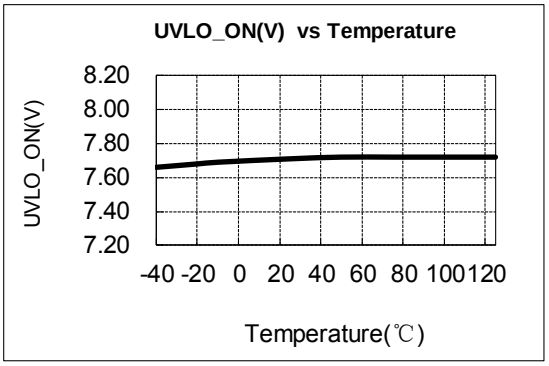
Parameter / Product	Max VDS(V) GaN FET Max Drain-Source Voltage			Rds,on(Ω) On resistance		
	Min	Typ.	Max	Min	Typ.	Max
OB2733VCTP-V			650[note]		1.0	

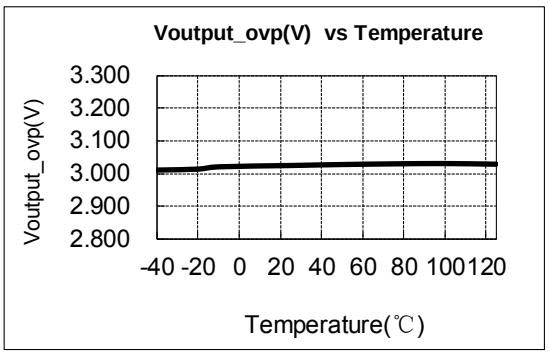
Note: The transient VDS voltage is relaxed to 800V for surge ratings during non-repetitive events that are<200us and repetitive events that are<100ns.

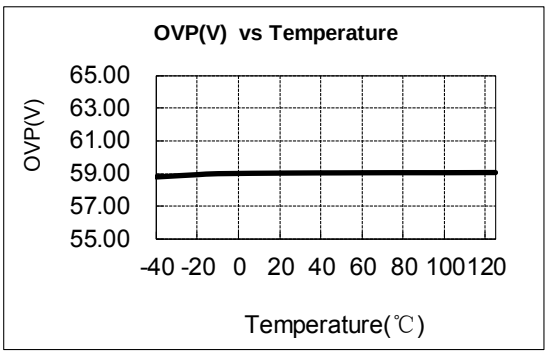
CHARACTERIZATION PLOTS

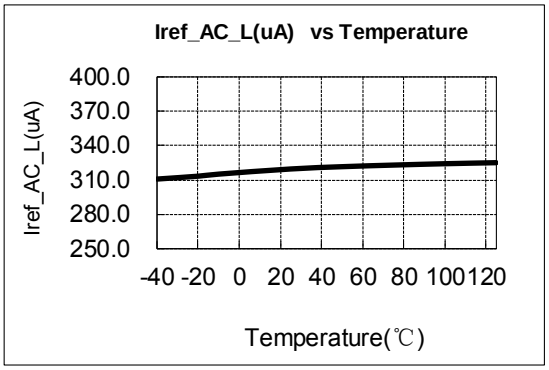
VDD = 18V, TA = 25℃ condition applies if not otherwise noted.

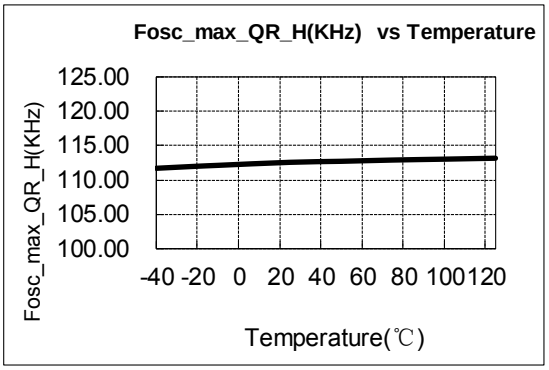


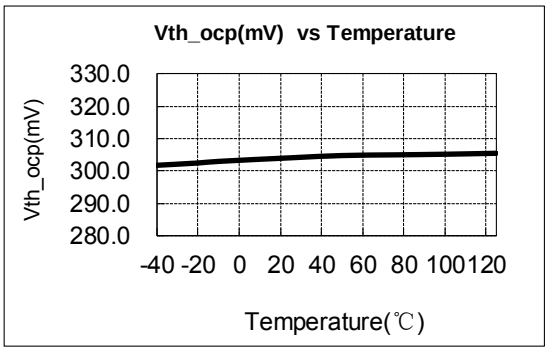












OPERATION DESCRIPTION

Quasi-Resonant (QR) converter typically features lower EMI and higher power conversion efficiency compared to conventional hard-switched converter with a fixed switching frequency. OB2733x is a highly integrated high frequency Quasi-Resonant (QR) controller with adaptive multi-mode regulation, optimized for high power density GaN FETs PD adapter solutions, together with PD secondary controller, such as OB2621. The controller is as well compatible with cost effective offline flyback converter applications covering a wide output range. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of OB2733x is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

Operating Current

The Operating current of OB2733x is low at 2.5mA (typical). Good efficiency is achieved with OB2733x low operation current together with the 'extended burst mode' control features.

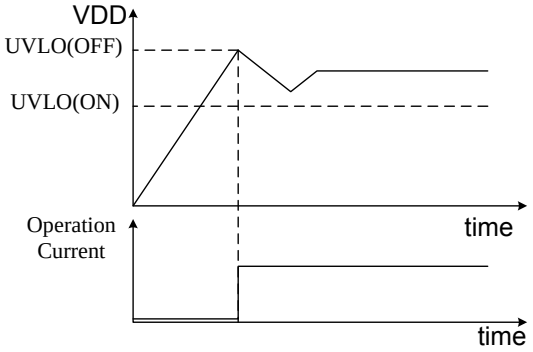


Fig.1 Startup current timing

Soft Start

OB2733x features an internal 2.5ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the CS peak voltage is gradually increased from 0 V to the maximum level. Every restart up is followed by a soft start.

Extended Burst Mode Operation

At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below Vref_burst_L (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to Vref_burst_H (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to greatest extend.

Frequency shuffling for EMI improvement

The frequency Shuffling (switching frequency modulation) is implemented in OB2733x. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Multi-Mode Operation for High Efficiency

OB2733x is a multi-mode PWM controller, integrating the QR, CCM, green and burst mode. The controller changes the operation mode according to line voltage, output voltage and load conditions. At high AC line input conditions, it operates in a forced quasi-resonance (QR) valley switching mode with On-Bright proprietary technology for excellent EMI performance.

At peak power load conditions, there are two situations: firstly, if the system input is in low line input range, the IC can operate in 70KHz fixed frequency CCM mode and the first valley switching mode. Secondly, if the system input is in high line input range, the IC operates in QR mode with a minimum 25KHz clamp frequency.

At full load conditions, the IC may operate in the valley switching QR mode both in the low line input and high line input. The frequency varies depending on the line voltage and the load conditions. In this way, by working in valley switching QR mode, high power conversion efficiency can be achieved in the universal input range when system is at full loading conditions.

At middle load conditions (Vth1<VFB<Vth2), the system operates in PFM (pulse frequency modulation) mode for high power conversion efficiency. Generally, in flyback converter, the decreasing of load results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. However, the valley switching characteristic is still preserved in PFM mode. That

is, when load decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced. In such way, a smooth frequency fold-back is realized and high power conversion efficiency is achieved.

At no load or very light load conditions (VFB<Vth1), the system operates in On-Bright's proprietary "extended burst mode". In the extended burst mode, the switching frequency at below 25KHz is minimized to avoid audio noise during operation.

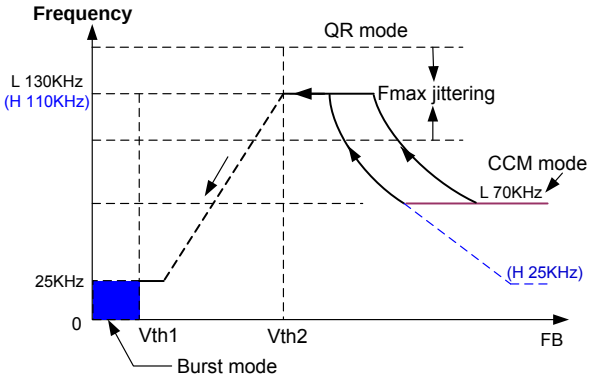


Fig. 2 Frequency vs Feedback voltage

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2733x current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense voltage and the FB voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through DEM pin. This voltage features a flyback polarity. After the on time (determined by the CS voltage and FB voltage), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_pC_d}$, where L_p is the primary self inductance of primary winding of the transformer and C_d is the capacitance on the drain node.

The typical detection level is fixed at 200mV(typical) at the DEM pin. Demagnetization is recognized by detection of a possible "valley" when the voltage at DEM is below 200mV in falling edge.

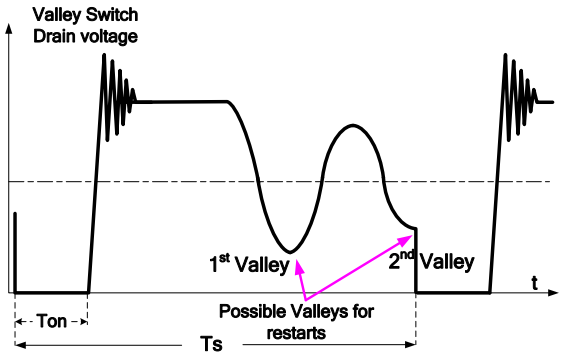


Fig. 3 Valley detection

Adaptive OCP Compensation

The variation of max output power in QR system can be rather large if no compensation is provided. The OCP threshold value is self adjusted lower at higher AC voltage. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage. In OB2733x, with On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range. A proprietary OCP compensation block is integrated and no external components are needed.

It provides an adaptive cycle-by-cycle OCP compensation method varying with gate on duty cycle in Fig4. For duty cycle less than D1, the OCP threshold changes linearly from 0.3V to 0.33V. For duty cycle larger than D2, the OCP threshold is clamped to 0.36V (typical), as shown in Figure 4.

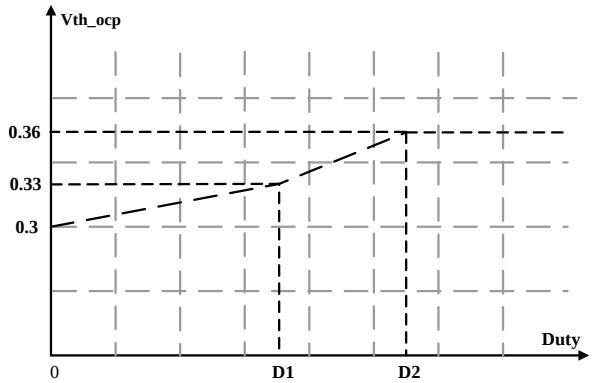
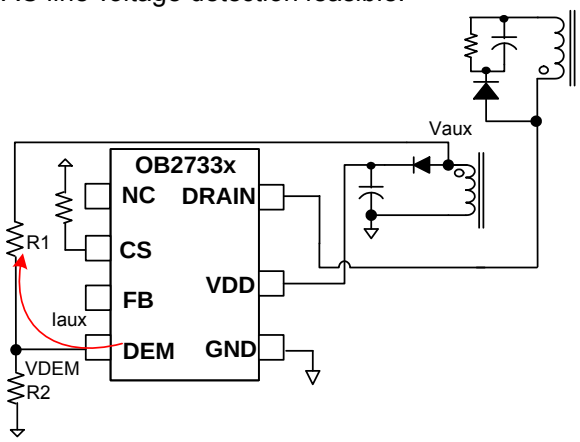


Fig4 Cycle by cycle OCP compensation

Multiple Functions of Output voltage detection and AC line voltage detection

When the power MOSFET is turn on, the voltage on auxiliary windings is negative which make our AC line voltage detection feasible.



$$I_{AUX} = \frac{0.1}{R2} + \frac{0.1 - V_{AUX}}{R1}$$

R1: The resistor connected from DEM to AUX.

R2: The resistor connected from DEM to ground.

After system starts up, if IC detects I_{aux} < Iref_AC_L, low line voltage operation mode is triggered after 40ms debounce. If IC detects I_{aux} > Iref_AC_H, high line voltage operation mode is triggered after 40ms debounce.

For output voltage OVP detection, when Gate is off, V_{DEM} is equal to V_{AUX}*R2/(R1+R2). If V_{DEM} is larger than 3V (typical), OVP auto-recovery protection is triggered after 8 Gate cycles debounce.

For output voltage SCP detection, after system start-up 15ms later, If V_{DEM} is smaller than 0.4V(typical), the internal counter starts counting subsequent SCP events more than 8 cycles, and the same time FB open>12mS & VCS>Vth_OCP, and then SCP protection is triggered with auto-recovery.

By selecting proper R1 and R2 resistance, output OVP level can be programmed.

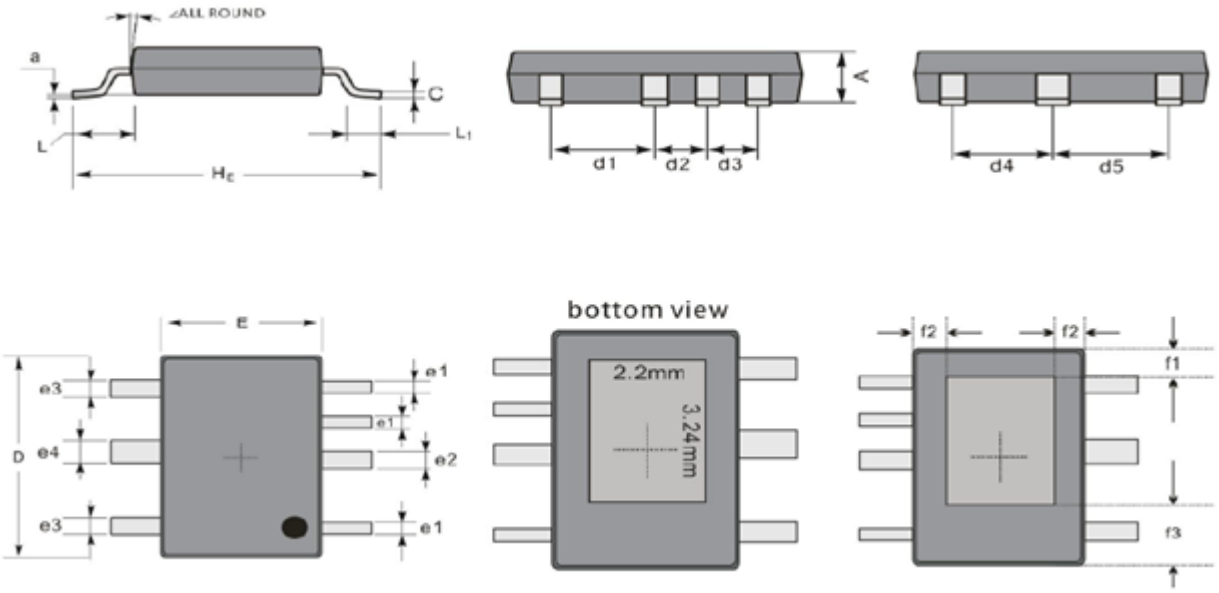
$$V_{AUX} = \frac{3*(R1+R2)}{R2}$$

Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VDD (UVLO), Internal Over Temperature Protection (OTP), VDD Over Voltage Protection (OVP), output SCP and output Over Voltage Protection (OVP).

At overload condition when FB input voltage exceeds power limit threshold value for more than Td_OLP, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.05	1.25	0.041	0.049
C	0.15	0.22	0.006	0.009
D	6.00	6.40	0.236	0.252
E	3.70	4.10	0.146	0.161
HE	5.90	6.10	0.232	0.240
d1	2.46	2.56	0.097	0.101
d2	1.28	1.38	0.050	0.054
d3	1.22	1.32	0.048	0.052
d4	2.18	2.28	0.086	0.090
d5	2.68	2.78	0.106	0.109
e1	0.35	0.45	0.014	0.018
e2	0.46	0.56	0.018	0.022
e3	0.50	0.60	0.020	0.024
e4	0.75	0.85	0.030	0.033
L	0.95	1.15	0.037	0.045
L1	0.40	0.80	0.016	0.031
a	0.20 (REF)		0.008 (REF)	
f1	0.61	0.71	0.024	0.028
f2	0.80	0.90	0.031	0.035
f3	2.25	2.35	0.089	0.093

IMPORTANT NOTICE

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