ZN65C1R070L Preliminary Datasheet

650V, 70mΩ typ., GaN FET in DFN 8x8 Package

1. General Description

The ZN65C1R070L is a 650V, 70 mΩ Gallium Nitride (GaN) FET in an 8 x 8 DFN package. It is a normally-off device that combines ZienerTech's latest high-voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

2. Features and Benefits

- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Wide gate safety margin
- Capable of reverse conduction
- Low gate charge
- RoHS compliant and Halogen-free packaging
- Achieves increased efficiency in both hard- and soft- switched circuits
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Easy to drive with commonly-used gate drivers

3. Applications

- Fast charger
- Telecom power
- Data center
- Lighting

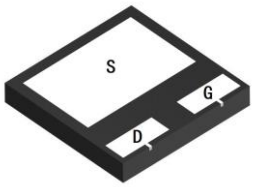
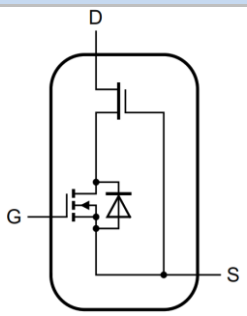
4. Key Specifications

Table 1. Key Specifications

Symbol	Parameter	Value	Unit
$V_{DS,\ max}$	Drain-source voltage	650	V
$I_{D,\ max}$	Continuous drain current @Tc = 25°C	24	A
$R_{DS(on),\ typ}$	Drain-source on-state resistance	70	mΩ
$Q_{G,\ typ}$	Total gate charge	9.5	nC
$Q_{RR,\ typ}$	Reverse recovery charge	110	nC

5. Pin Description

Table 2. Pin Description

Pin	Description	Bottom View	Graphic Symbol
G	Gate		
D	Drain		
S	Source		

6. Ordering Information

Table 3. Ordering Information

Part number	Package	Package Configuration	Marking Code
ZN65C1R070L	DFN 8*8	Source	ZN65C1R070L

7. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Parameter	Symbol	Min.	Max.	Unit.	Conditions
Drain to source voltage	V_{DSS}	-	650	V	V_{GS} = 0V
Transient drain to source voltage	$V_{DSS(TR)}$	-	800		Non-repetitive Pulse for ⩽10ms at 25℃
Gate to source voltage	V_{GSS}	-20	20		
Maximum power dissipation	P_D	-	96	W	T_C = 25°C, Fig.1
Continuous drain current	I_D	-	24	A	T_C = 25°C
		-	15	A	T_C = 100°C
Pulsed drain current	I_{DM}	-	TBD	A	Pulsed, t_p ≤ 200μs,T_C = 25°C
Operating temperature	T_J	-55	150	°C	
Storage temperature	T_S	-55	150	°C	

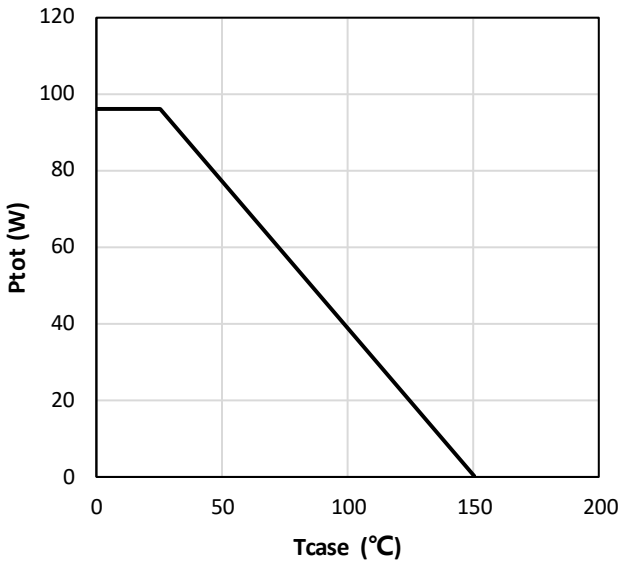


Fig. 1. Power Dissipation

TBD

Fig 2. Safe Operating Area T_C = 25°C

8. Thermal Characteristics

Table 5. Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Thermal resistance (Junction-to-case)	$R_{th(j-c)}$	-	1.3	-	°C/W	
Thermal resistance (Junction-to-ambient) [a]	$R_{th(j-a)}$	-	62	-	°C/W	
Reflow soldering temperature	T_{SOLD}	-	-	260	°C	reflow MSL3

Notes:

a. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm^2 copper area and 70µm thickness).

TBD

Fig. 3. Transient Thermal Impedance

9. Electrical Characteristics

Table 6. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Device Characteristics						
Gate threshold voltage	$V_{GS(th)}$	-	4	-	V	V_{DS} = V_{GS}, I_D = 0.7mA
Drain-source on-state resistance [a]	$R_{DS(on)}$	-	70	-	mΩ	V_{GS} = 10V, I_D = 16A, T_J = 25°C, Fig.18,Fig.19
		-	144	-		V_{GS} = 10V, I_D = 16A, T_J = 150°C, Fig.18,Fig.19
Drain-to-source leakage current	I_{DSS}	-	4	-	μA	V_{DS} = 650V,V_{GS} = 0V, T_J = 25°C
		-	10	-		V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C
Gate-to-source leakage current	I_{GSS}	-	-	100	nA	V_{GS} = 20V, V_{DS} = 0V, T_J = 25°C
		-	-	-100		V_{GS} = -20V, V_{DS} = 0V, T_J = 25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input capacitance	C_{ISS}	-	765	-	pF	V_{GS} = 0V, V_{DS} = 400V, f = 1MHz, Fig.8
Output capacitance	C_{OSS}	-	60	-		
Reverse transfer capacitance	C_{RSS}	-	1.1	-		
Output capacitance, energy related [a]	$C_{O(er)}$	-	110	-	pF	V_{GS} = 0V, V_{DS} = 0V to 400V, Fig. 9
Output capacitance, time related [b]	$C_{O(tr)}$	-	225	-		
Total gate charge	Q_G	-	9.5	-	nC	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 16A,Fig. 11
Gate-source charge	Q_{GS}	-	4.2	-		
Gate-drain charge	Q_{GD}	-	2	-		
Output charge	Q_{OSS}	-	90	-	nC	V_{GS} = 0V, V_{DS} = 0V to 400V
Turn-on delay time	$t_{D(on)}$	-	38	-	ns	V_{DS} = 400V, V_{GS} = 0V to 12V, I_D = 16A, R_{G_on} = 51Ω, R_{G_off} = 2Ω Fig.14; Fig.15
Rise time	t_R	-	17	-		
Turn-off delay time	$t_{D(off)}$	-	37	-		
Fall time	t_F	-	7	-		
Reverse Device Characteristics						
Reverse voltage [c]	V_{SD}	-	1.8	-	V	V_{GS} = 0V, I_S = 16A,T_J = 25°C, Fig. 12
		-	1.3	-		V_{GS} = 0V, I_S = 8A, T_J = 25°C, Fig. 12
Reverse recovery time	t_{RR}	-	24	-	ns	I_S = 16A,V_{DD} = 400V, di/dt = 1000A/us, Fig.16; Fig. 17
Reverse recovery charge	Q_{RR}	-	110	-	nC	V_{GS} = 0V, I_S = 16A, T_J = 25°C, Fig.16; Fig. 17

Notes:

a. Equivalent capacitance to give same stored energy from 0V to 400V

b. Equivalent capacitance to give same charging time from 0V to 400V

c. Includes dynamic $R_{DS(on)}$ effect

9.1 Electrical characteristics(curves) (T_C=25°C unless otherwise stated)

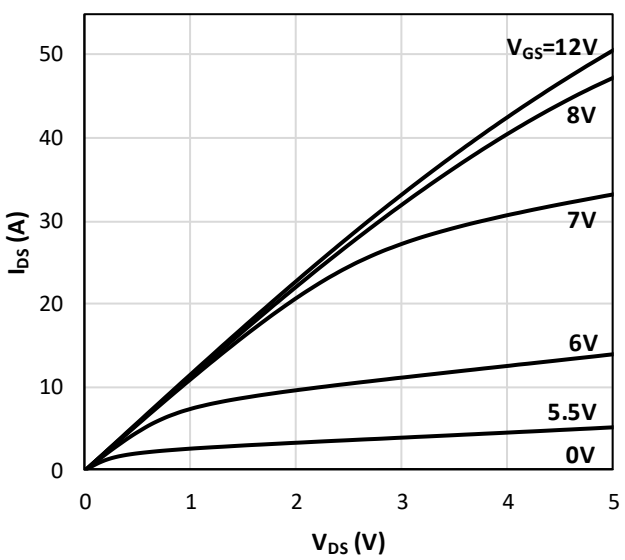


Figure 4. Typical Output Characteristics
T_J = 25°C

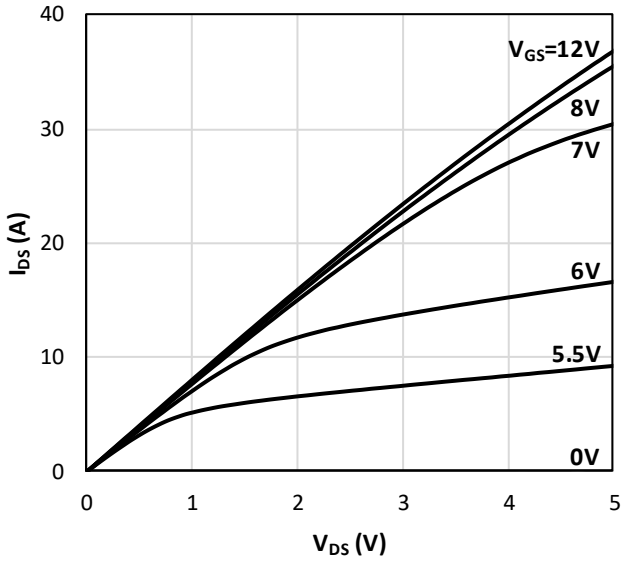


Figure 5. Typical Output Characteristics
T_J = 150°C

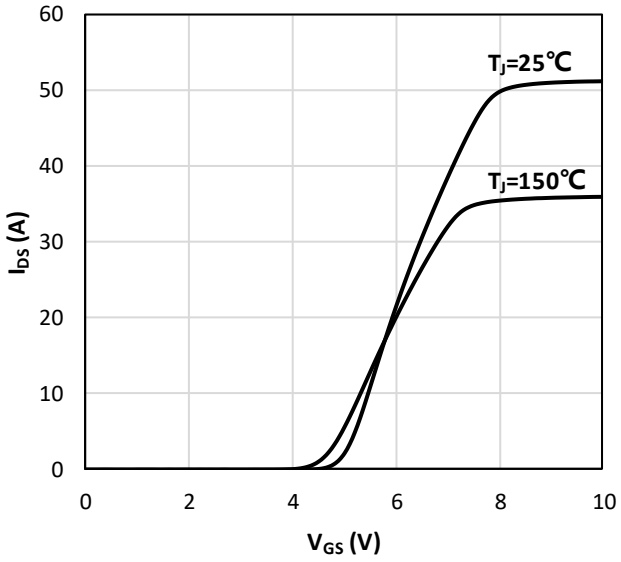


Fig. 6. Typical Transfer Characteristics
V_{DS} = 5V

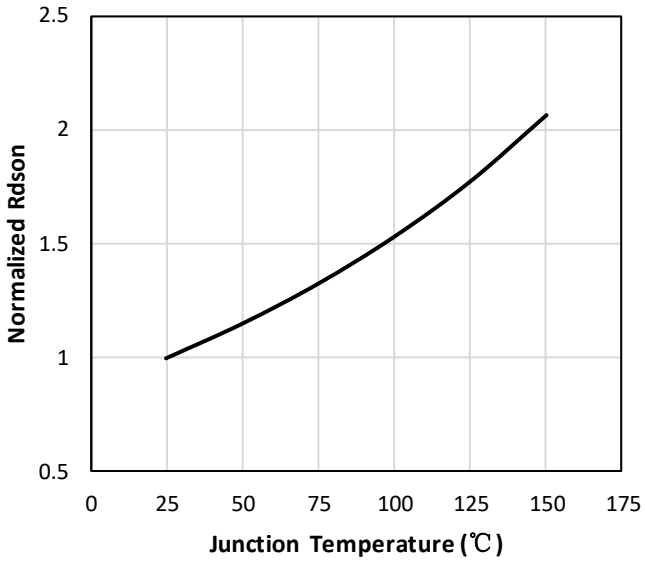


Fig. 7. Normalized On-resistance
I_D = 16A, V_{GS} = 10V

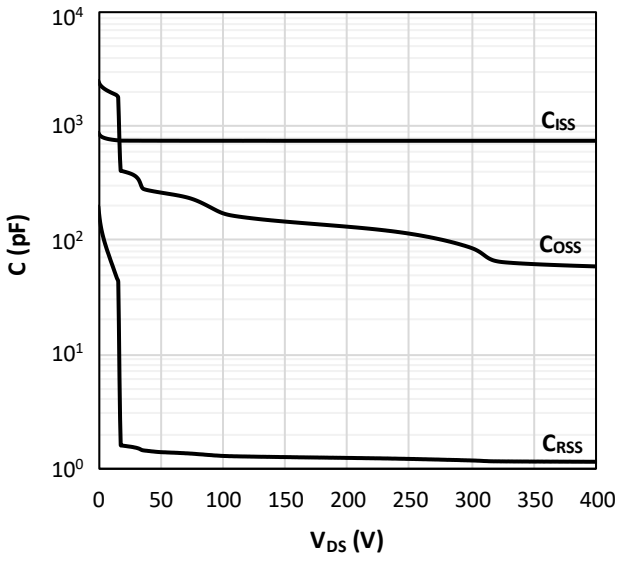


Fig. 8. Typical Capacitance

V_{GS} = 0V, f = 1MHz

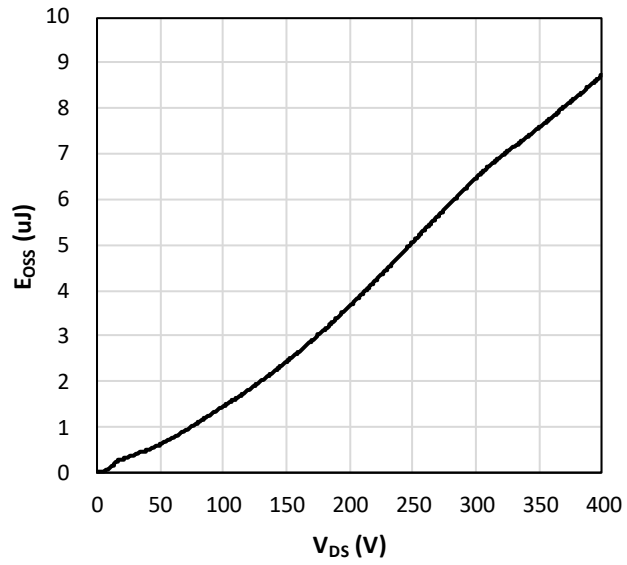


Fig. 9. Typical Coss Stored Energy

V_{GS} = 0V, f = 1MHz

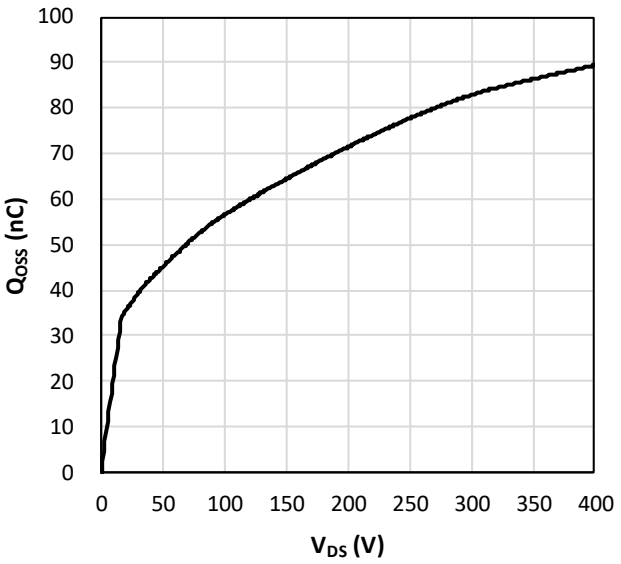


Fig. 10. Typical Q_{OSS}

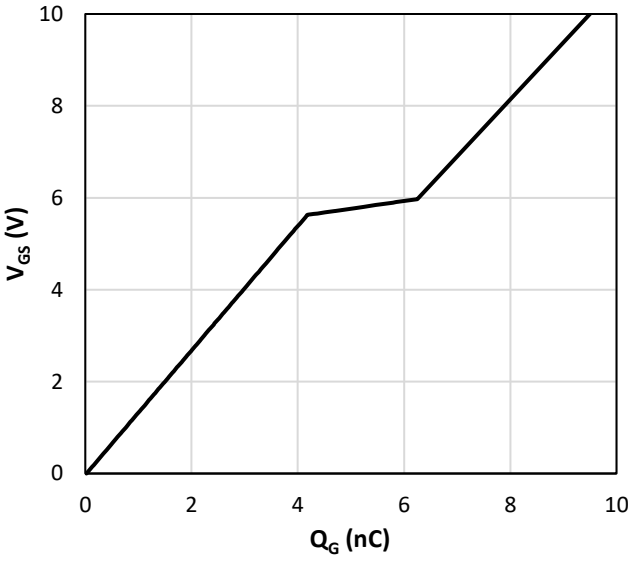


Fig. 11. Typical Gate Charge

I_{DS} = 16A, V_{DS} = 400V

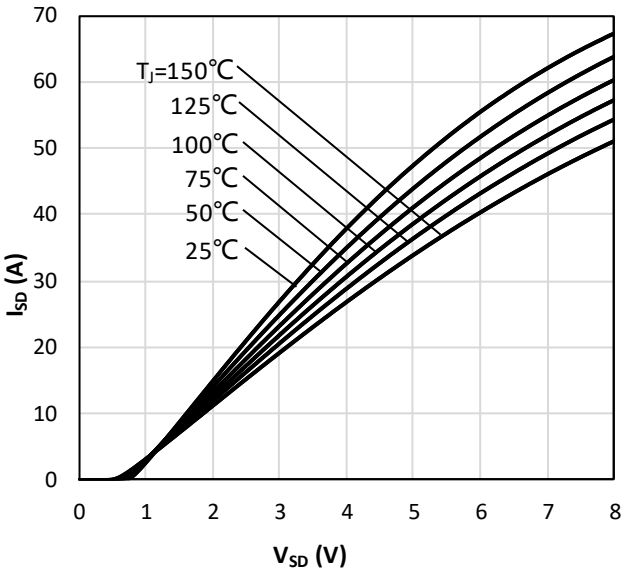


Fig. 12. Forward Characteristics of Rev. Diode
$I_{SD} = f(V_{SD})$

TBD

Fig. 13. Typical R_{DS}(on)

10. Test Circuits

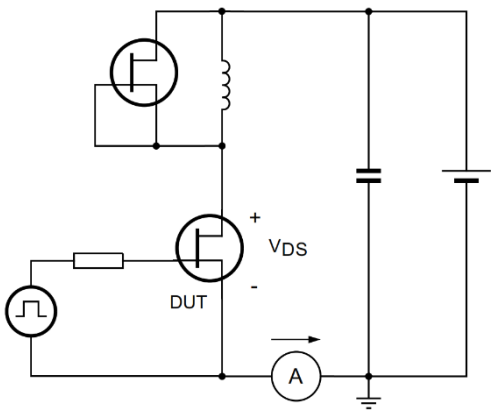


Fig. 14. Switching Time Test Circuit

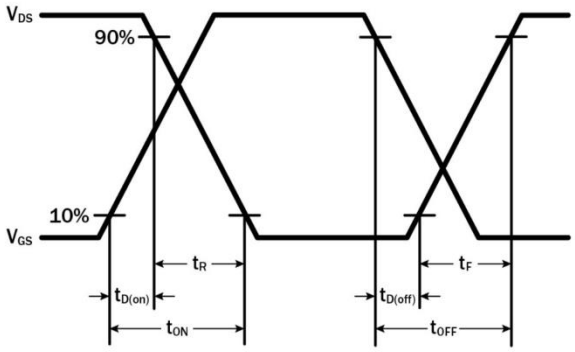


Fig. 15. Switching Time Waveform

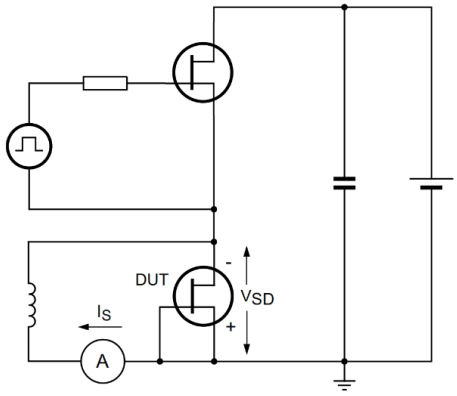


Fig. 16. Diode Characteristics Test Circuit

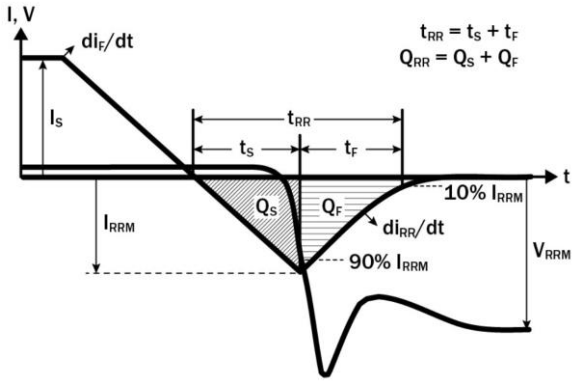


Fig. 17. Diode Recovery Waveform

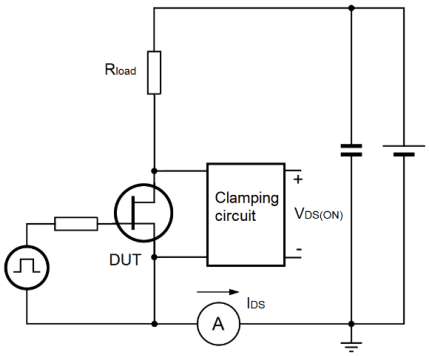


Fig. 18. Dynamic $R_{DS(on)eff}$ Test Circuit

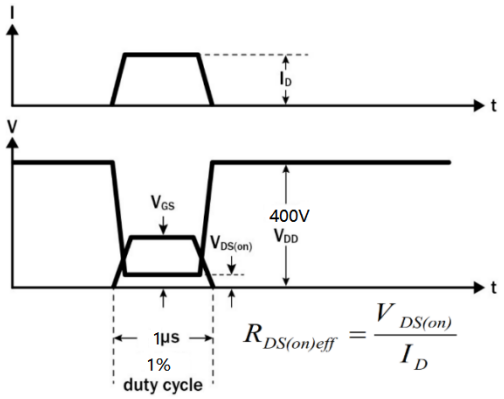


Fig. 19. Dynamic RDS(on)eff Waveform

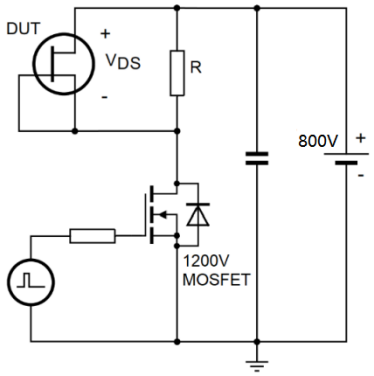


Fig. 20. Spike Voltage Test Circuit

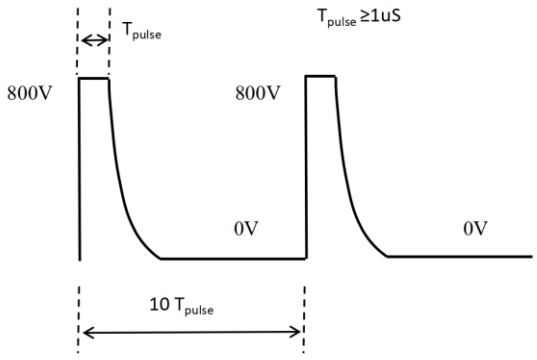


Fig. 21. Spike Voltage Waveform

11. Package Information

11.1 DFN 8x8 Package Information

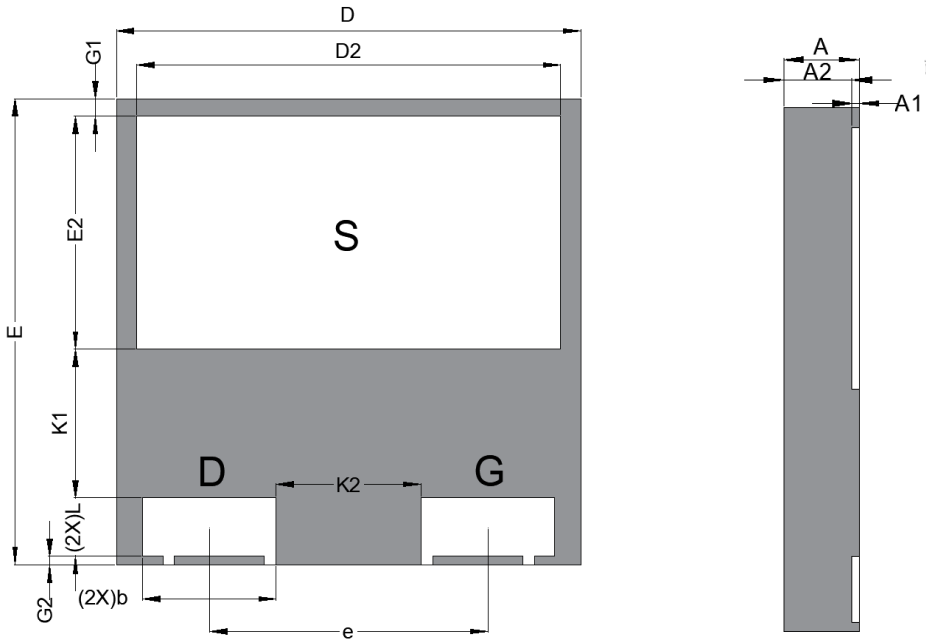


Fig. 22. DFN 8x8 Package Outline

DIM	mm			in		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.40	1.45	0.053	0.055	0.057
A1	0.007	0.012	0.017	/		
A2	1.343	1.388	1.433	/		
b	2.25	2.30	2.35	0.088	0.090	0.092
D	7.90	8.00	8.10	0.308	0.312	0.316
D2	7.25	7.30	7.35	0.283	0.285	0.287
E	7.90	8.00	8.10	0.308	0.312	0.316
E2	4.20	4.25	4.30	0.164	0.166	0.168
e	4.8BSC			0.187BSC		
K1	2.50	-	-	0.098	-	-
K2	2.50	-	-	0.098	-	-
L	0.75	0.80	0.85	0.029	0.031	0.033
G1	0.25	0.30	0.35	0.010	0.012	0.014
G2	0.10	0.15	0.20	0.004	0.006	0.008

12. Important Notice

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Revision History

Revision	Date	Changes
1.0	15/6/2023	Preliminary Datasheet