DRV8823 4-Bridge Serial Interface Motor Driver

1 Features

- PWM Motor Driver With Four H-Bridges
  - Drives Two Stepper Motors, One Stepper and Two DC Motors, or Four DC Motors
  - Up to 1.5-A Current Per Winding
  - Low On-Resistance
  - Programmable Maximum Winding Current
  - Three-Bit Winding Current Control Allows up to Eight Current Levels
  - Selectable Slow or Mixed Decay Modes
- 8- to 32-V Operating Supply Voltage Range
- Internal Charge Pump for Gate Drive
- Built-in 3.3-V Reference
- Serial Digital Control Interface
- Fully Protected Against Undervoltage, Overtemperature, and Overcurrent Events
- Thermally-Enhanced Surface Mount Package

2 Applications

- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

3 Description

The DRV8823 provides an integrated motor driver solution for printers and other office automation equipment applications.

The motor driver circuit includes four H-bridge drivers. Each of the motor driver blocks employ N-channel power MOSFETs configured as an H-bridge to drive the motor windings.

A simple serial interface allows control of all functions of the motor driver with only a few digital signals. The devices also provides a low-power sleep function.

The motor drivers provide PWM current control capability. The current is programmable, based on an externally supplied reference voltage and an external current sense resistor. In addition, eight current levels (set through the serial interface) allow microstepping with bipolar stepper motors.

Internal shutdown functions are provided for overcurrent protection (OCP), short-circuit protection, undervoltage lockout, and overtemperature.

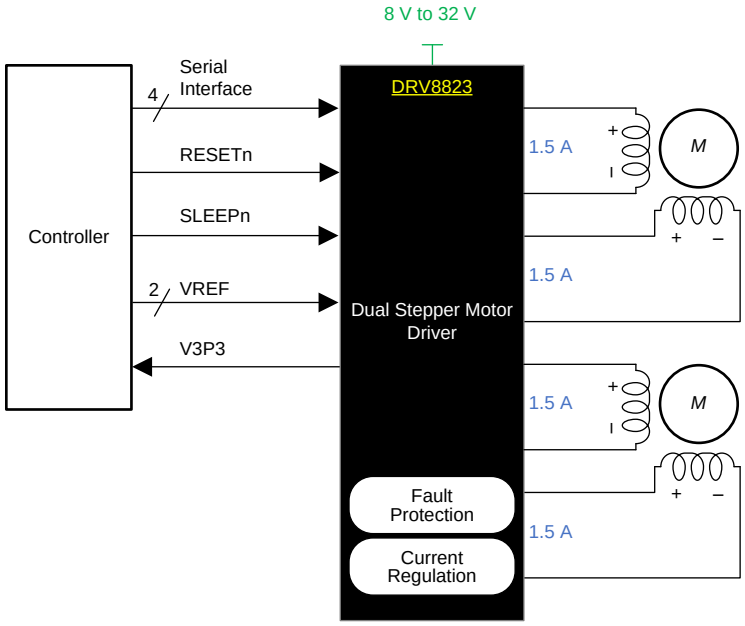
The DRV8823 is packaged in a 48-pin HTSSOP package (eco-friendly: RoHS and no Sb/Br).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8823	HTSSOP (48)	6.10 mm × 12.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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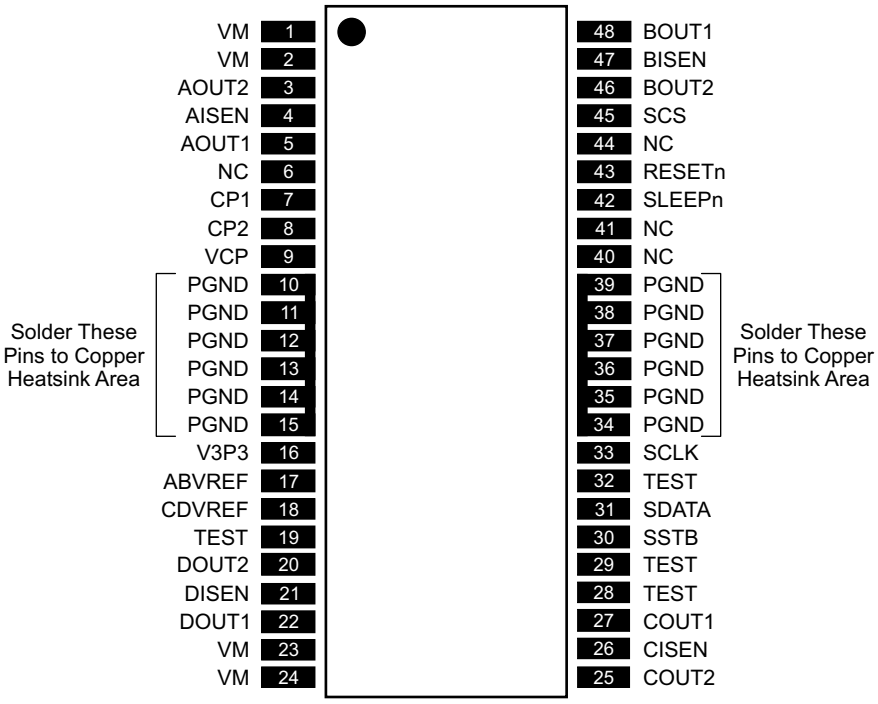
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2014) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

DCA Package
48-Pin HTSSOP
Top View



Pin Functions

PIN		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
VM	1	—	Motor supply voltage (multiple pins)	Connect all VM pins together to motor supply voltage. Bypass to GND with several 0.1-µF, 35-V ceramic capacitors.
	2			
	23			
	24			
V3P3	16	—	3.3-V regulator output	Bypass to GND with 0.47-µF, 6.3-V ceramic capacitor.
GND	10 to 15	—	Power ground (multiple pins)	Connect all PGND pins to GND and solder to copper heatsink areas.
	34 to 39			
CP1	7	I/O	Charge pump flying capacitor	Connect a 0.01-µF capacitor between CP1 and CP2
CP2	8	I/O		
VCP	9	I/O	Charge pump storage capacitor	Connect a 0.1-µF, 16-V ceramic capacitor to V_M
MOTOR DRIVERS				
ABVREF	17	I	Bridge A and B current set reference voltage	Sets current trip threshold.
AOUT1	5	O	Bridge A output 1	Connect to first coil of bipolar stepper motor 1, or DC motor winding.
AOUT2	3	O	Bridge A output 2	
ISENA	4	—	Bridge A current sense	Connect to current sense resistor for bridge A.
BOUT1	48	O	Bridge B output 1	Connect to second coil of bipolar stepper motor 1, or DC motor winding.
BOUT2	46	O	Bridge B output 2	
ISENB	47	—	Bridge B current sense	Connect to current sense resistor for bridge B.

(1) Directions: I = Input, O = Output, OZ = Tri-state output, OD = Open-drain output, I/O = Input/output, PU = Internal pullup

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
CDVREF	18	I	Bridge C and D current set reference voltage	Sets current trip threshold.
COUT1	27	O	Bridge C output 1	Connect to first coil of bipolar stepper motor 2, or DC motor winding.
COUT2	25	O	Bridge C output 2	
ISENC	26	—	Bridge C current sense	Connect to current sense resistor for bridge C.
DOUT1	22	O	Bridge D output 1	Connect to second coil of bipolar stepper motor 2, or DC motor winding.
DOUT2	20	O	Bridge D output 2	
ISEND	22	—	Bridge D current sense	Connect to current sense resistor for bridge D.
SERIAL INTERFACE				
SDATA	31	I	Serial data input	Data is clocked in on rising edge of SCLK.
SCLK	33	I	Serial input clock	Logic high enables serial data to be clocked in.
SCS	45	I	Serial chip select	Logic high latches serial data.
SSTB	30	I	Serial data strobe	Active low resets serial interface and disables outputs.
RESETn	43	I	Reset input	Active-low input disables outputs and charge pump.
SLEEPn	42	I	Sleep input	
TEST PINS				
TEST	19	I	Test inputs	Do not connect these pins (used for factory test only).
	28			
	29			
	32			

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_M	Power supply voltage	–0.3	34	V
V_I	Logic input voltage(3)	–0.5	5.75	V
$I_{O(peak)}$	Peak motor drive output current, t < 1 µs	Internally limited		
I_O	Motor drive output current(4)		1.5	A
P_D	Continuous total power dissipation	See *Dissipation Ratings*		
T_J	Operating virtual junction temperature	–40	150	°C
T_A	Operating ambient temperature	–40	85	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Input pins may be driven in this voltage range regardless of presence or absence of V_M.
(4) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range	8		32	V
I_{MOT}	Continuous motor drive output current(1)		1	1.5	A
V_{REF}	VREF input voltage(2)	1		4	V

(1) Power dissipation and thermal limits must be observed.
(2) Operational at VREF between 0 and 1 V, but accuracy is degraded.

6.4 Thermal Information

THERMAL METRIC(1)		DRV8823 DCA (HTSSOP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	V_M operating supply current	V_M = 24 V, no loads		5	8	mA
V_{UVLO}	V_M undervoltage lockout voltage	V_M rising		6.5	8	V
V_{CP}	Charge pump voltage	Relative to V_M		12		V
V_{V3P3}	V_{V3P3} output voltage		3.2	3.3	3.4	V
LOGIC-LEVEL INPUTS (INTERNAL PULLDOWNS)						
V_{IL}	Input low voltage				0.7	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis		0.3	0.45	0.6	V
I_{IN}	Input current (internal pulldown current)	V_{IN} = 3.3 V			100	µA
OVERTEMPERATURE PROTECTION						
T_{TSD}	Thermal shutdown temperature	Die temperature	150			°C
MOTOR DRIVERS						
$R_{ds(on)}$	Motor 1 FET on resistance (each individual FET)	V_M = 24 V, I_O = 0.8 A, T_J = 25°C		0.25		Ω
		V_M = 24 V, I_O = 0.8 A, T_J = 85°C		0.31	0.37	
$R_{ds(on)}$	Motor 2 FET on resistance (each individual FET)	V_M = 24 V, I_O = 0.8 A, T_J = 25°C		0.3		Ω
		V_M = 24 V, I_O = 0.8 A, T_J = 85°C		0.38	0.45	
I_{OFF}	Off-state leakage current				±12	µA
f_{PWM}	Motor PWM frequency(1)		45	50	55	kHz
t_{BLANK}	ITRIP blanking time(2)			3.75		µs
t_F	Output fall time		50		300	ns
t_R	Output rise time		50		300	ns
I_{OCP}	Overcurrent protect level		1.5	3	4.5	A
t_{OCP}	Overcurrent protect trip time		2.5			µs
t_{MD}	Mixed decay percentage	Measured from beginning of PWM cycle		75%		
CURRENT CONTROL						
I_{REF}	xVREF input current	xVREF = 3.3 V	–3		3	µA
ΔI_{CHOP}	Chopping current accuracy	xVREF = 2.5 V, derived from V3P3; 71% to 100% current	–5%		5%	
		xVREF = 2.5 V, derived from V3P3; 20% to 56% current	–10%		10%	

(1) Factory option 100 kHz.
(2) Factory options for 2.5, 5, or 6.25 µs.

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

NO.			MIN	MAX	UNIT
1	t_{CYC}	Clock cycle time	62		ns
2	t_{CLKH}	Clock high time	25		ns
3	t_{CLKL}	Clock low time	25		ns
4	$t_{SU(SDATA)}$	Setup time, SDATA to SCLK	5		ns
5	$t_{H(DATA)}$	Hold time, SDATA to SCLK	1		ns
6	$t_{SU(SCS)}$	Setup time, SCS to SCLK	5		ns
7	$t_{H(SCS)}$	Hold time, SCS to SCLK	1		ns

6.7 Dissipation Ratings

BOARD	PACKAGE	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
Low-K(1)	DCA	75.7°C/W	13.2 mW/°C	1.65 W	1.06 W	0.86 W
Low-K(2)		32°C/W	31.3 mW/°C	3.91 W	2.50 W	2.03 W
High-K(3)		30.3°C/W	33 mW/°C	4.13 W	2.48 W	2.15 W
High-K(4)		22.3°C/W	44.8 mW/°C	5.61 W	3.59 W	2.91 W

(1) The JEDEC low-K board used to derive this data was a 76-mm × 114-mm, 2-layer, 1.6-mm thick PCB with no backside copper.
(2) The JEDEC low-K board used to derive this data was a 76-mm × 114-mm, 2-layer, 1.6-mm thick PCB with 25-cm^2, 2-oz copper on back side.
(3) The JEDEC high-K board used to derive this data was a 76-mm × 114-mm, 4-layer, 1.6-mm thick PCB with no backside copper and solid 1-oz internal ground plane.
(4) The JEDEC high-K board used to derive this data was a 76-mm × 114-mm, 4-layer, 1.6-mm thick PCB with 25-cm^2, 1-oz copper on backside and solid 1-oz internal ground plane.

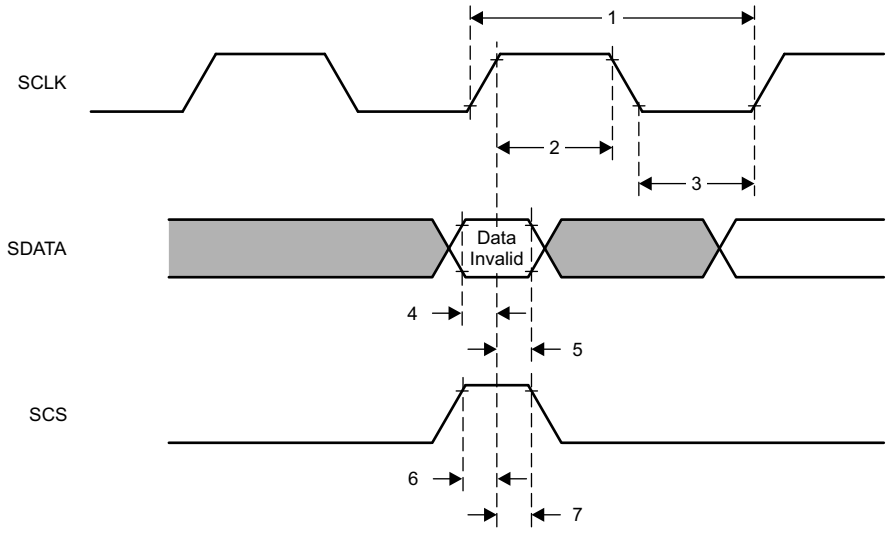


Figure 1. Timing Diagram

6.8 Typical Characteristics

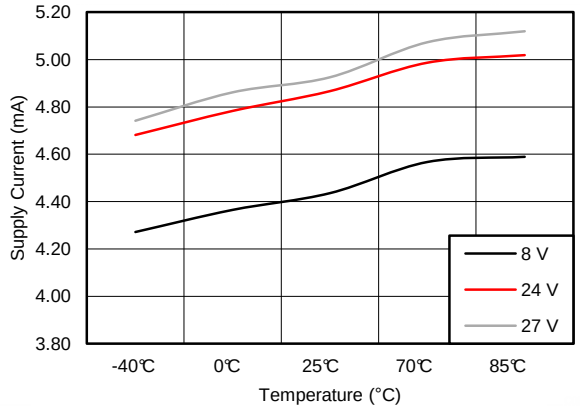


Figure 2. Supply Current vs Temperature

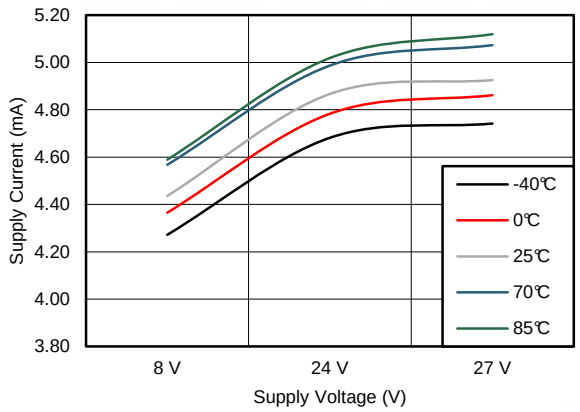


Figure 3. Supply Current vs Supply Voltage

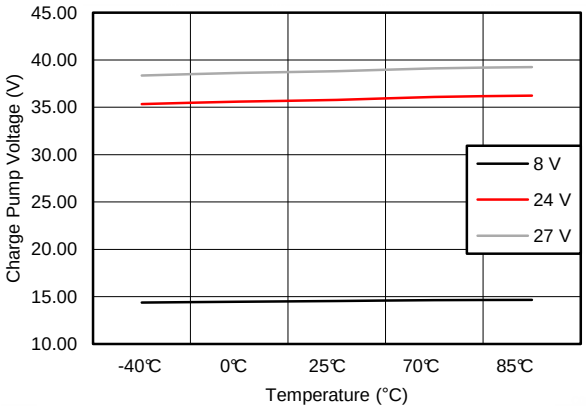


Figure 4. Charge Pump Voltage vs Temperature

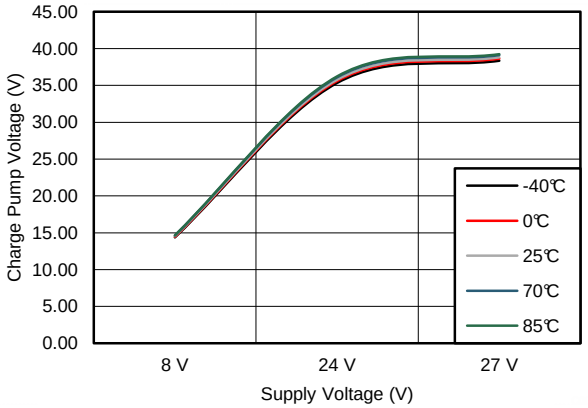


Figure 5. Charge Pump Voltage vs Supply Voltage

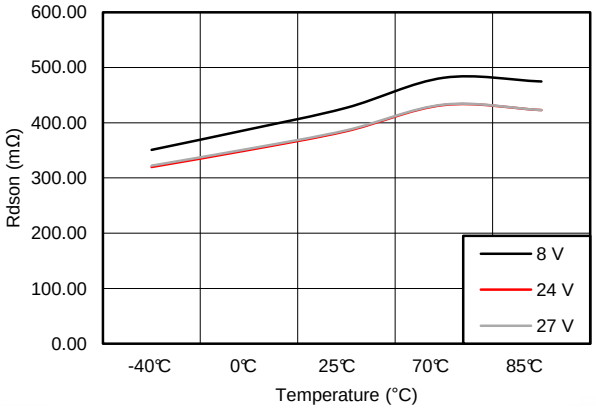


Figure 6. LS Rdson Aout2 vs Temperature

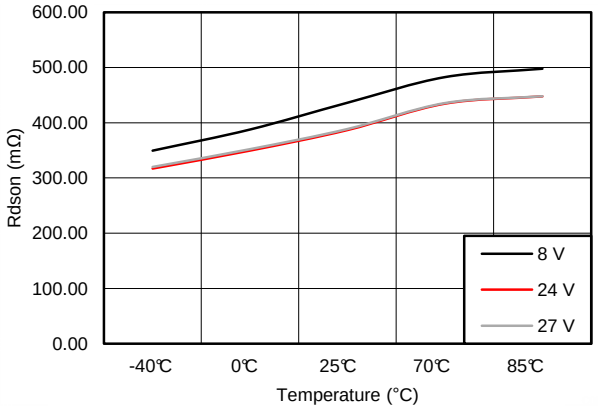


Figure 7. LS Rdson Aout1 vs Temperature

Typical Characteristics (continued)

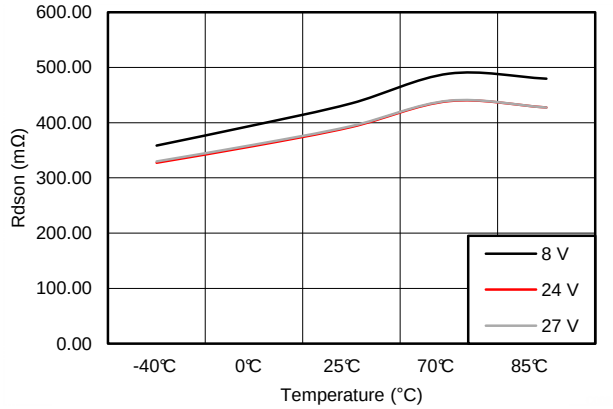


Figure 8. HS Rdson Aout2 vs Temperature

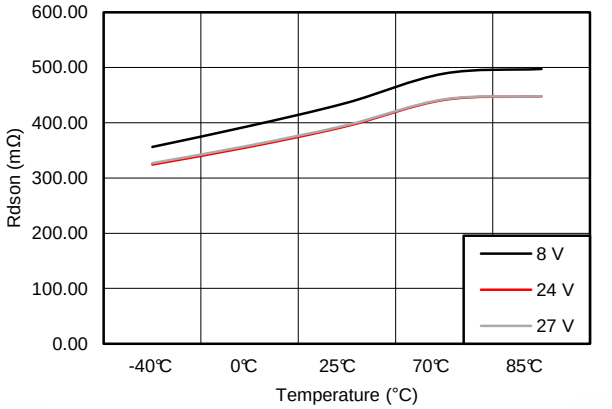


Figure 9. HS Rdson Aout1 vs Temperature

7 Detailed Description

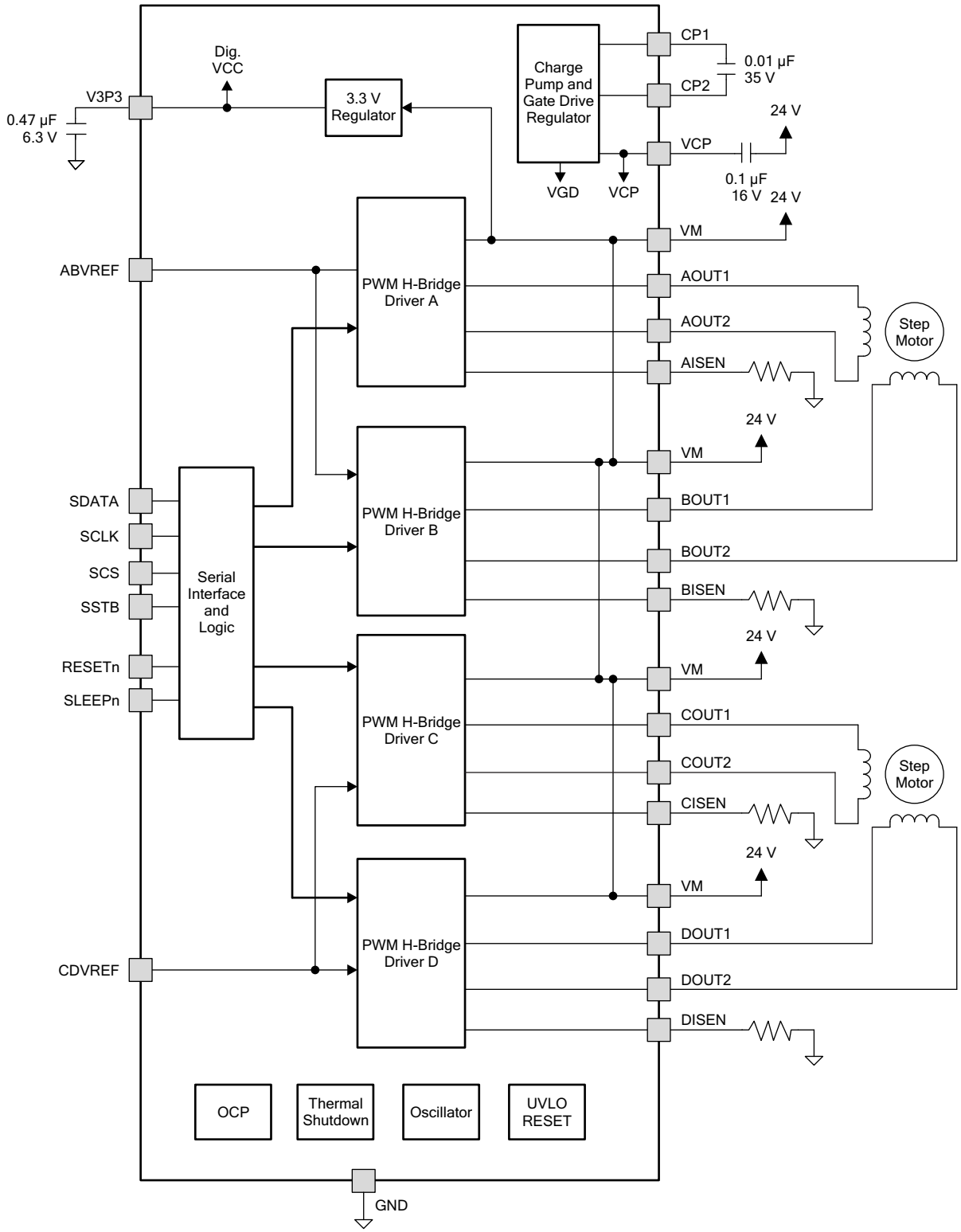
7.1 Overview

The DRV8823 is a dual stepper motor driver solution for applications that require independent control of two different motors. The device integrates four NMOS H-bridges, a microstepping indexer, and various fault protection features. The DRV8823 can be powered with a supply voltage between 8 and 32 V, and is capable of providing an output current up to 1.5 A full scale. Actual full-scale current will depend on ambient temperature, supply voltage and PCB ground size.

A serial data interface is included to control all functions of the motor driver. Current regulation through all four H-bridges is achieved using three register bits per H-bridge. The three register bits are used to scale the current in each bridge as a percentage of the full-scale current set by VREF input pin and sense resistor. The current regulation is configurable with two different decay modes, fixed slow and mixed.

The gate drive to each FET in all four H-Bridges is controlled to prevent any cross-conduction (shoot through current) during transitions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8823 contains four H-bridge motor drivers with current-control PWM circuitry. Figure 10 shows a block diagram with drivers A and B of the motor control circuitry (as typically used to drive a bipolar stepper motor). Drivers C and D are the same as A and B (though the $R_{DS(ON)}$ of the output FETs is different).

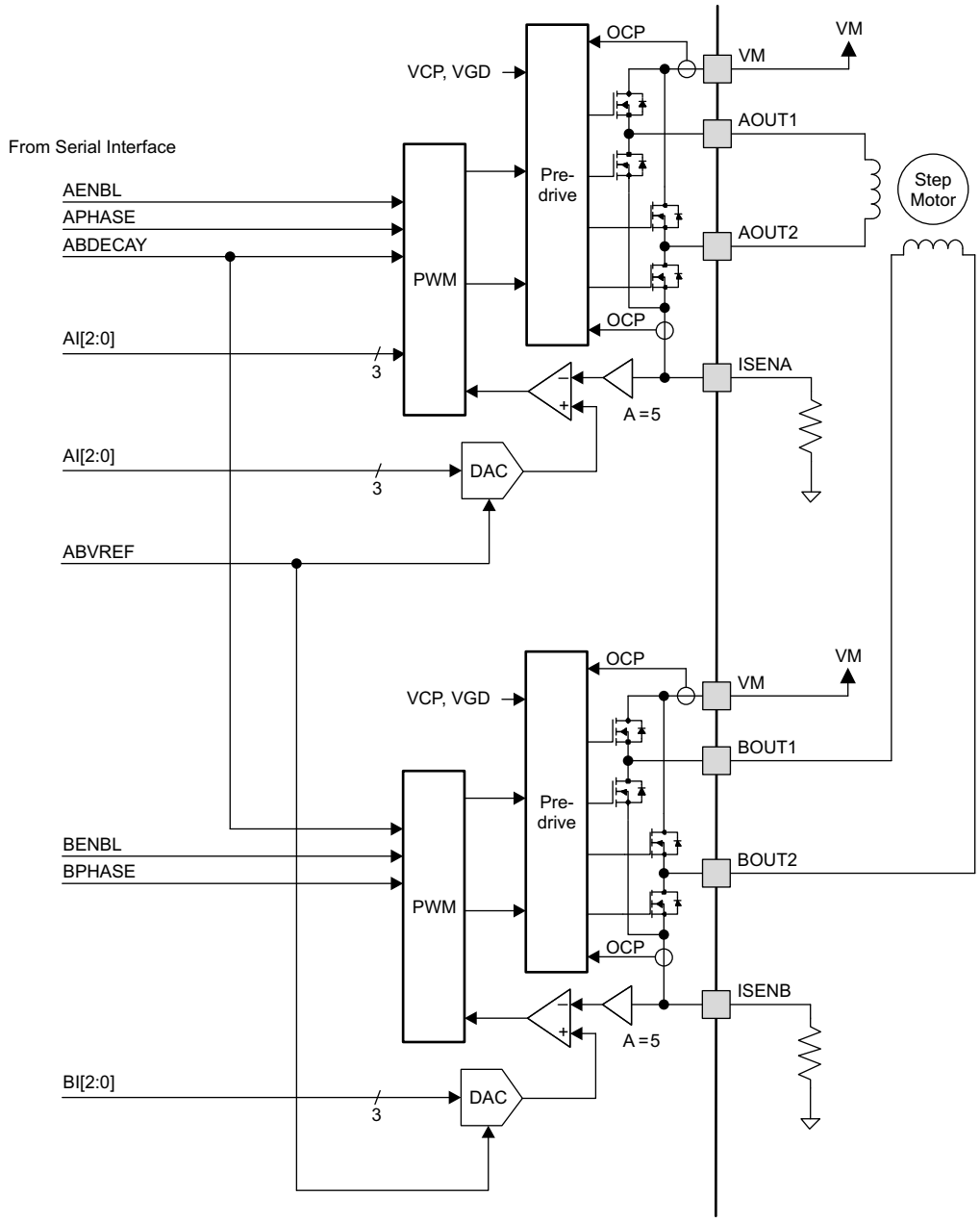


Figure 10. Block Diagram With Drivers A and B

NOTE

The device has multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

7.4 Device Functional Modes

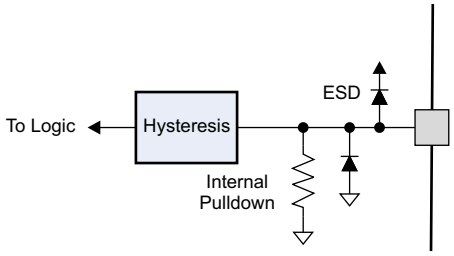


Figure 11. Logic Inputs

7.4.1 Bridge Control

The xENBL bits in the serial interface registers enable current flow in each H-bridge when set to 1.

The xPHASE bits in the serial interface registers control the direction of current flow through each H-bridge. Table 1 shows the logic.

Table 1. Bridge Control Logic

xPHASE	xOUT1	xOUT2
1	H	L
0	L	H

7.4.2 Current Regulation

The motor driver employs fixed-frequency PWM current regulation (also called current chopping). When a winding is activated, the current through it rises until it reaches a threshold, then the current is switched off until the next PWM period.

The PWM frequency is fixed at 50 kHz, but may also be set to 100 kHz by factory option.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the VREF pin.

The full-scale (100%) chopping current is calculated as follows:

$$I_{CHOP} = \frac{V_{REFX}}{5 \bullet R_{ISENSE}} \quad (1)$$

Example:

If a 0.5-Ω sense resistor is used and the VREFx pin is 2.5 V, the full-scale (100%) chopping current is 2.5 V / (5 × 0.5 Ω) = 1 A.

Three serial interface register bits per H-bridge (xI2, xI1, and xI0) are used to scale the current in each bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. Table 2 shows the function of the bits.

Table 2. Bit Functions

xI2	xI1	xI0	Relative Current (% Full-Scale Chopping Current)
0	0	0	20
0	0	1	38
0	1	0	56
0	1	1	71
1	0	0	83
1	0	1	92

Table 2. Bit Functions (continued)

xI2	xI1	xI0	Relative Current (% Full-Scale Chopping Current)
1	1	0	98
1	1	1	100

7.4.3 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. Note that the blanking time also sets the minimum on-time of the PWM.

7.4.4 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached (see case 1 in Figure 12). The current flow direction shown indicates positive current flow in Figure 12.

After the chopping current threshold is reached, the H-bridge can operate in two different states: fast decay or slow decay.

In fast-decay mode, after the PWM chopping current level is reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches 0, the bridge is disabled to prevent any reverse current flow. See case 2 in Figure 12 for fast-decay mode.

In slow-decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge (see case 3 in Figure 12).

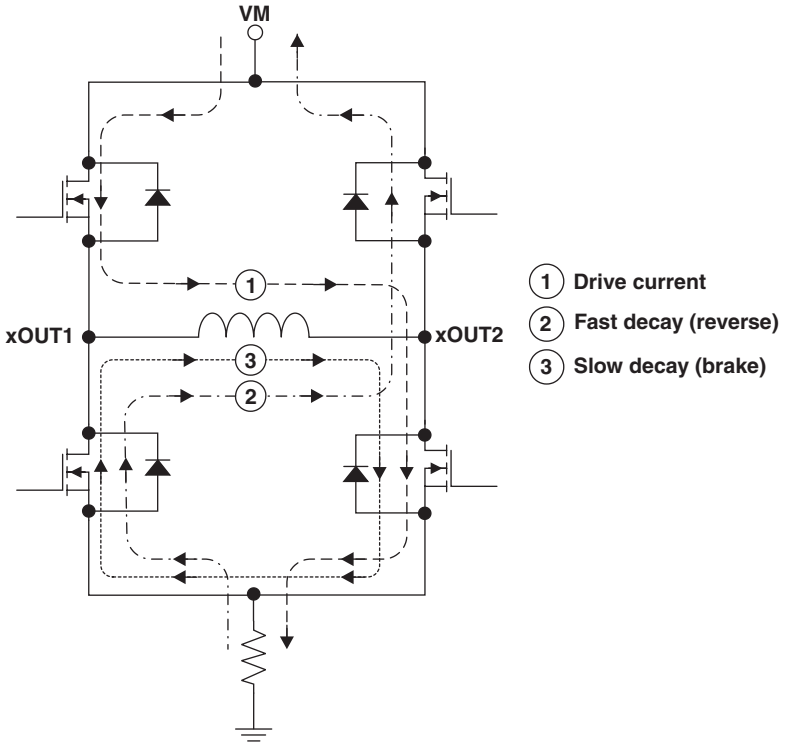


Figure 12. Decay Mode

The DRV8823 supports slow decay and also a mixed-decay mode. Mixed-decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) it switches to slow decay mode for the remainder of the fixed PWM period.

The state of the xDECAY bits in the serial interface registers selects whether the device is in slow-decay or mixed-decay mode. If the xDECAY bit is 0,the device selects slow decay. If the xDECAY bit is 1, the device selects mixed decay.

7.4.5 Protection Circuits

The DRV8823 is fully protected against undervoltage, overcurrent, and overtemperature events.

7.4.5.1 OCP

All of the drivers in DRV8823 are protected with an OCP circuit.

The OCP circuit includes an analog current limit circuit, which acts by removing the gate drive from each output FET if the current through it exceeds a preset level. This circuit limits the current to a level that is safe to prevent damage to the FET.

A digital circuit monitors the analog current limit circuits. If any analog current limit condition exists for longer than a preset period, all drivers in the device are disabled.

The device is re-enabled upon the removal and re-application of power at the VM pins.

7.4.5.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all drivers in the device are shut down.

The device remains disabled until the die temperature has fallen to a safe level. After the temperature has fallen, the device may be re-enabled upon the removal and re-application of power at the VM pin.

7.4.5.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the UVLO threshold voltage, all circuitry in the device is disabled. Operation resumes when VM rises above the UVLO threshold. The indexer logic is reset to its initial condition in the event of an UVLO.

7.4.5.4 Shoot-Through Current Prevention

The gate drive to each FET in the H-bridge is controlled to prevent any cross-conduction (shoot through current) during transitions.

7.4.6 Serial Data Transmission

Data transfers consist of sixteen bits of serial data, shifted into the SDATA pin LSB first.

On serial writes to DRV8823, additional clock edges following the final data bit continue to shift data bits into the data register; therefore, the last 16 bits presented are latched and used.

Select one of two registers by setting bits in an address field in the four upper bits in the serial data transferred (ADDR in Table 3 and Table 4). One 16-bit register is used to control motor 1 (bridges A and B), and a second 16-bit register is used to control motor 2 (bridges C and D).

Data can only be transferred into the serial interface if the SCS input pin is active high.

Data is initially clocked into a temporary holding register. This data is latched into the motor driver on the rising edge of the SSTB pin. If the SSTB pin is tied high at all times, the data is latched in after all 16 bits have been transferred.

7.5 Programming

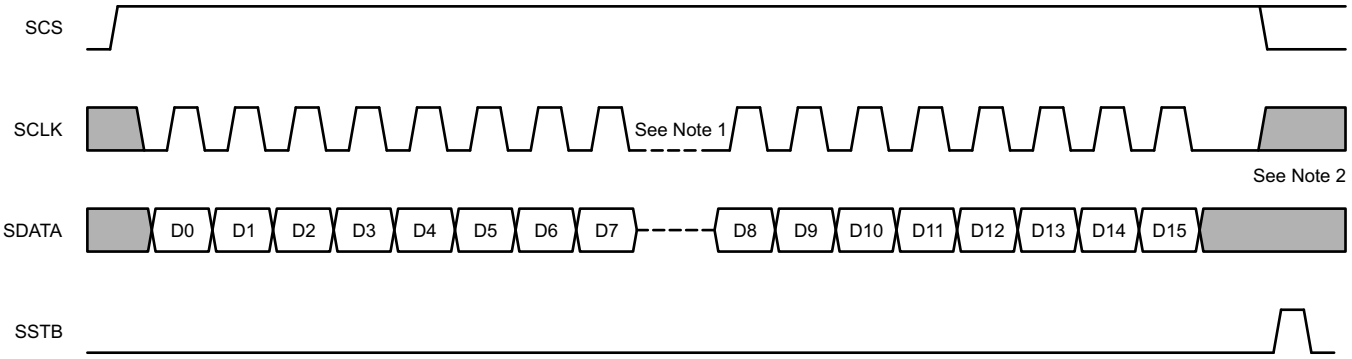
7.5.1 Data Format

Table 3. Motor 1 Command (Bridges A and B)

Bit	D15:D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ADDR (= 0000)	BDECAY	B12	B11	B10	BPHASE	BENBL	ADECAY	A12	A11	A10	APHASE	AENBL
Reset Value	x	0	0	0	0	0	0	0	0	0	0	0	0

Table 4. Motor 2 Command (Bridges C and D)

Bit	D15:D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ADDR (= 0001)	DDECAY	D12	D11	D10	DPHASE	DENBL	CDECAY	C12	C11	C10	CPHASE	CENBL
Reset Value	x	0	0	0	0	0	0	0	0	0	0	0	0



Note 1: Any amount of time is allowed between clocks, or groups of clocks, as long as SCS stays active. This allows 8- or 16-bit transfers.

Note 2: If more than 16 clock edges are presented while transferring data (while SCS is still high), data will continue to be shifted into the data register.

Figure 13. Serial Data Timing Diagram

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8823 can be used to drive two bipolar stepper motors.

8.2 Typical Application

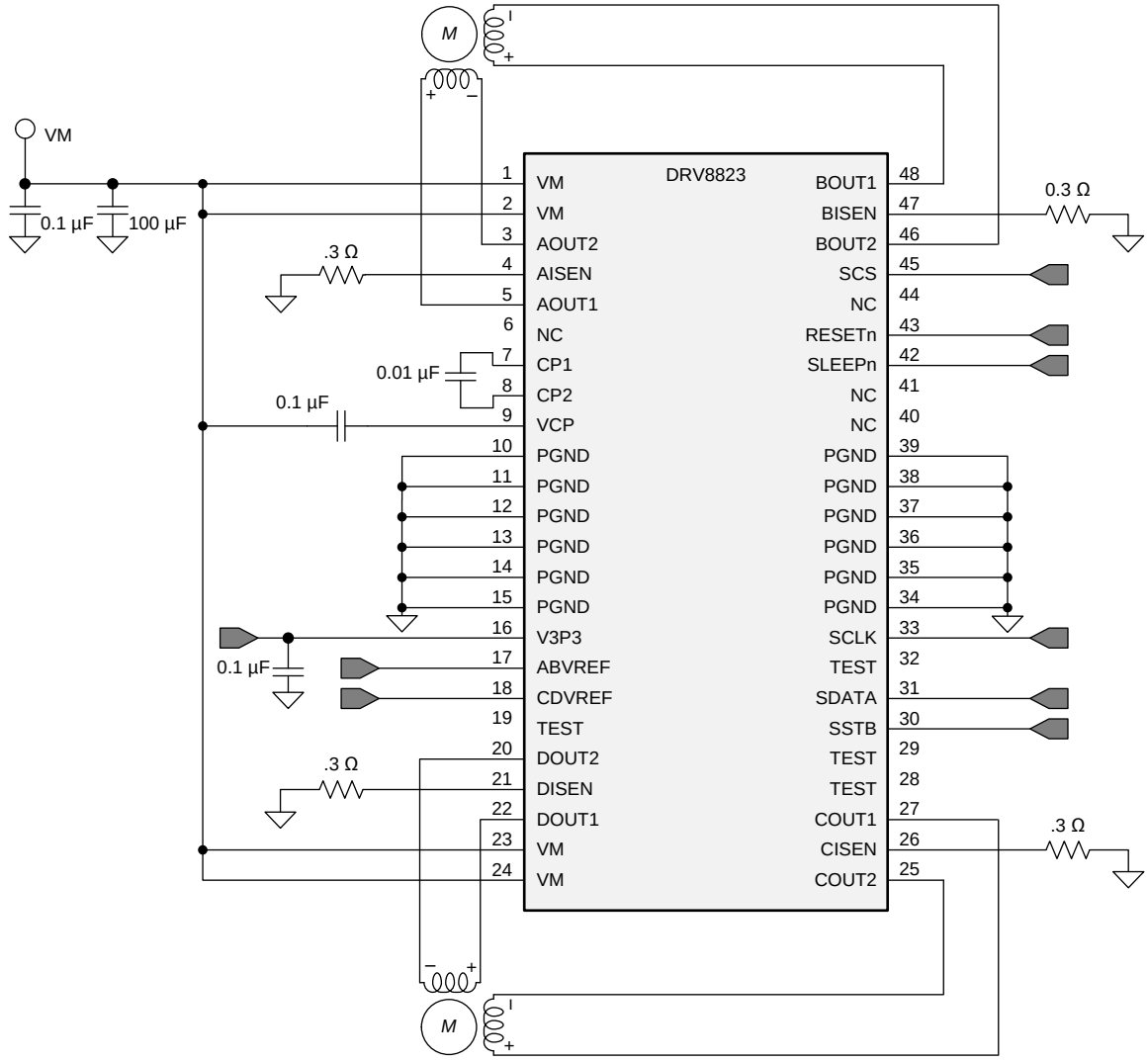


Figure 14. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 5 shows the design parameters.

Table 5. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_M	24 V
Motor winding resistance	R_L	7.4 Ω/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping angle	n_m	1/8 step
Target motor speed	V	120 rpm
Target full-scale current	I_{FS}	1 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The appropriate motor voltage will depend on the ratings of the motor selected and the desired torque. A higher voltage shortens the current rise time in the coils of the stepper motor allowing a greater average torque. Using a higher voltage also allows the motor to operate at a faster speed than a lower voltage.

8.2.3 Drive Current

The current path running to the motor starts from the supply VM, then goes through the high-side sourcing NMOS power FET, moves through the inductive winding load of the motor, then through the low-side sinking NMOS power FET, and finally going through the external sense resistor. Power dissipation losses in both NMOS power FETs inside of the DRV8823 are shown in the following equation: Equation 2.

$$P = I^2 \times (R_{DS\ (on)} \times 2) \quad (2)$$

The DRV8823 has been measured to be capable of 1.5-A continuous current with the HTSSOP package at 25°C on standard FR-4 PCBs. The max continuous current varies based on PCB design and the ambient temperature.

8.2.4 Application Curves

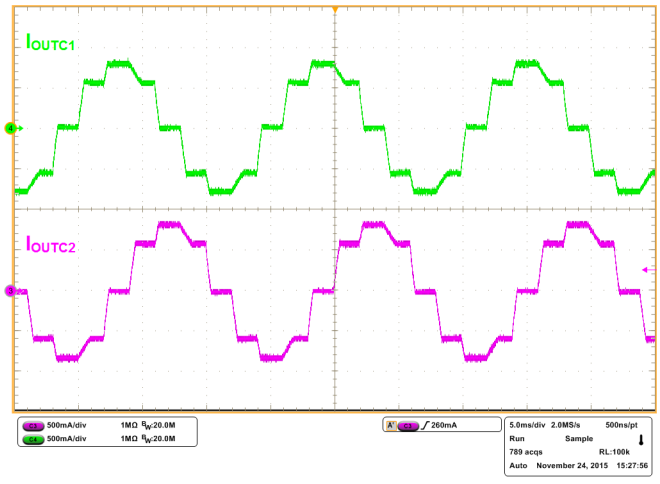


Figure 15. ½ Step Microstepping With Slow Decay

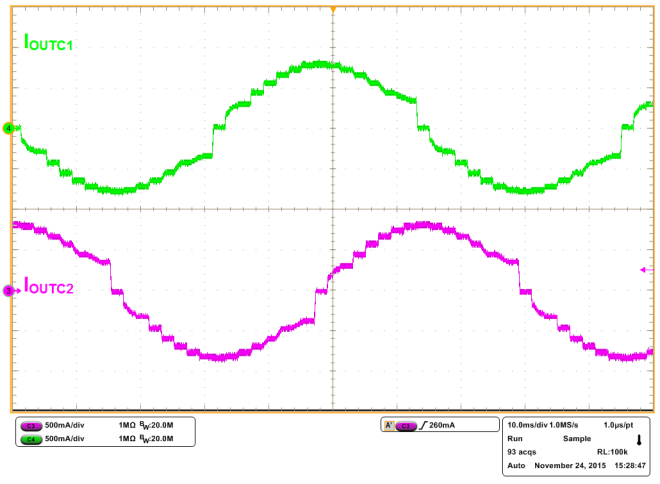


Figure 16. 1/8 Step Microstepping With Slow Decay

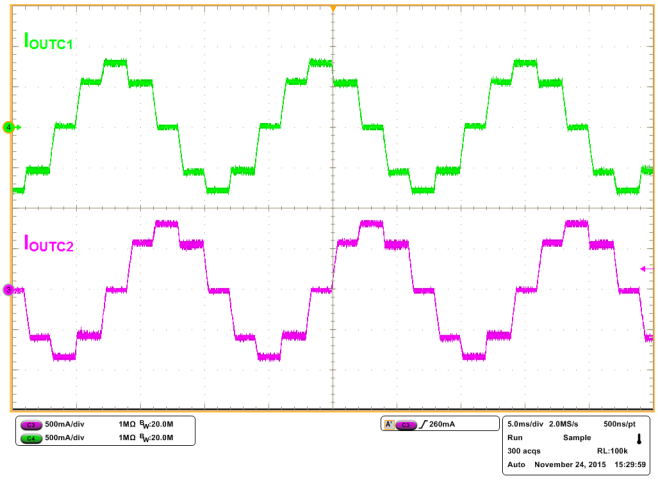


Figure 17. ½ Step Microstepping With Mixed Decay

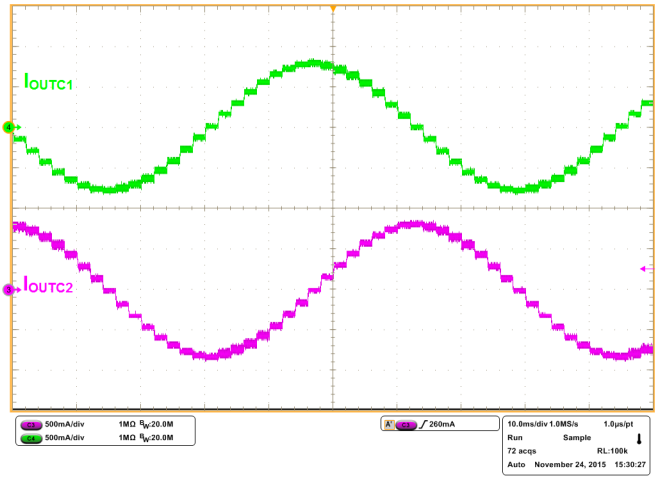


Figure 18. 1/8 Step Microstepping With Mixed Decay

9 Power Supply Recommendations

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The type of motor used (Brushed DC, Brushless DC, Stepper).

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

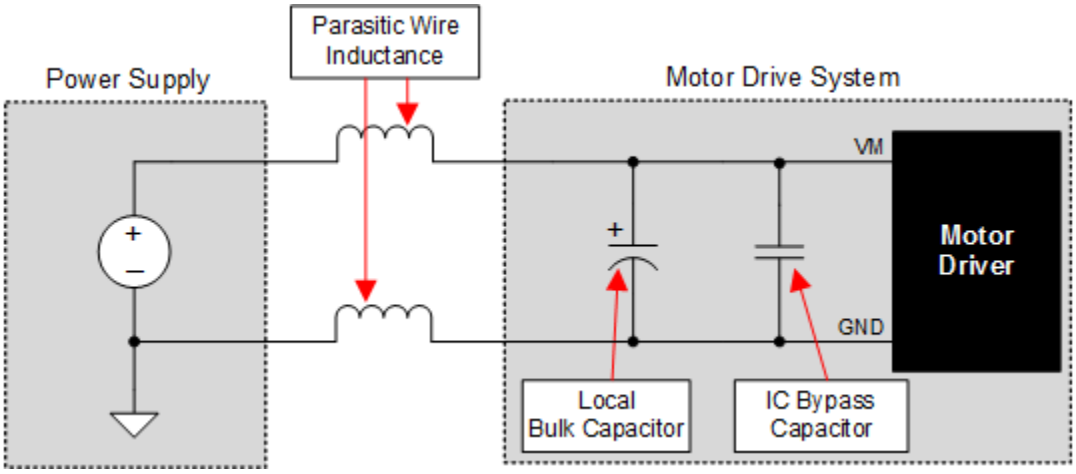


Figure 19. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

10.2 Layout Example

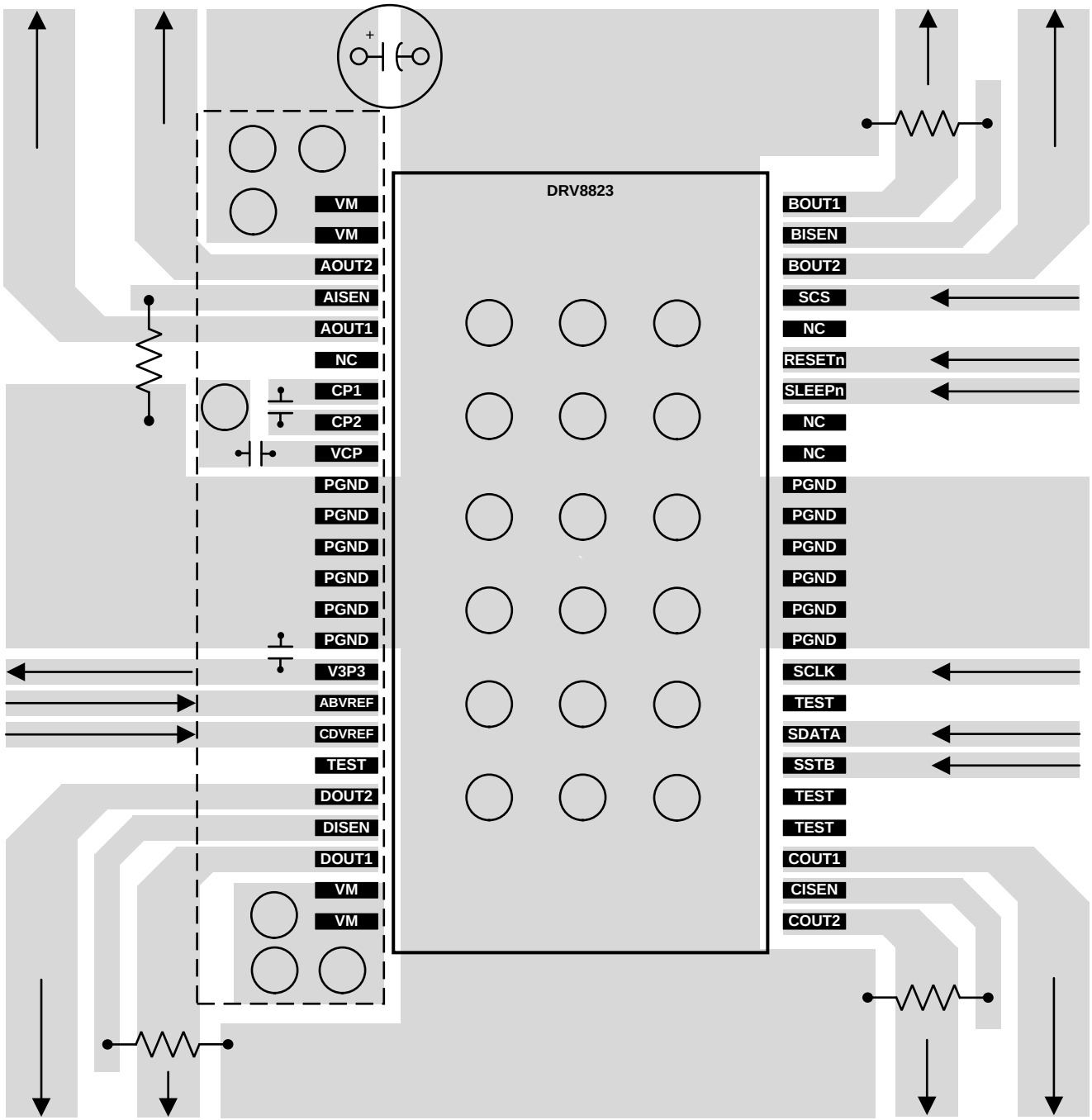


Figure 20. Typical Layout of DRV8823

10.3 Thermal Considerations

The DRV8823 has TSD as described in *Thermal Shutdown (TSD)*. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

Power dissipation in the DRV8823 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 3.

$$P_{TOT} = 4 \bullet R_{DS(ON)} \bullet (I_{OUT(RMS)})^2 \quad (3)$$

where

- P_{TOT} is the total power dissipation.
- $R_{DS(ON)}$ is the resistance of each FET.
- $I_{OUT(RMS)}$ is the RMS output current being applied to each winding.

$I_{OUT(RMS)}$ is equal to approximately 0.7x the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high side and one low side). Remember that the DRV8823 has two stepper motor drivers, so the power dissipation of each must be added together to determine the total device power dissipation.

The maximum amount of power that can be dissipated in the DRV8823 depends on ambient temperature and heatsinking. Use the thermal *Dissipation Ratings* to estimate the temperature rise for typical PCB constructions.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

10.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002) and TI application brief, *PowerPAD™ Made Easy*, (SLMA004) available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated. Figure 21 shows thermal resistance versus copper plane area for both a single-sided PCB with 2-oz copper heatsink area, and a 4-layer PCB with 1-oz copper and a solid ground plane. Both PCBs are 76 mm × 114 mm, and 1.6-mm thick. The heatsink effectiveness increases rapidly to about 20 cm^2, then levels off somewhat for larger areas.

Six pins on the center of each side of the package are also connected to the device ground. A copper area can be used on the PCB that connects to the PowerPAD as well as to all the ground pins on each side of the device. This is especially useful for single-layer PCB designs.

Thermal Considerations (continued)

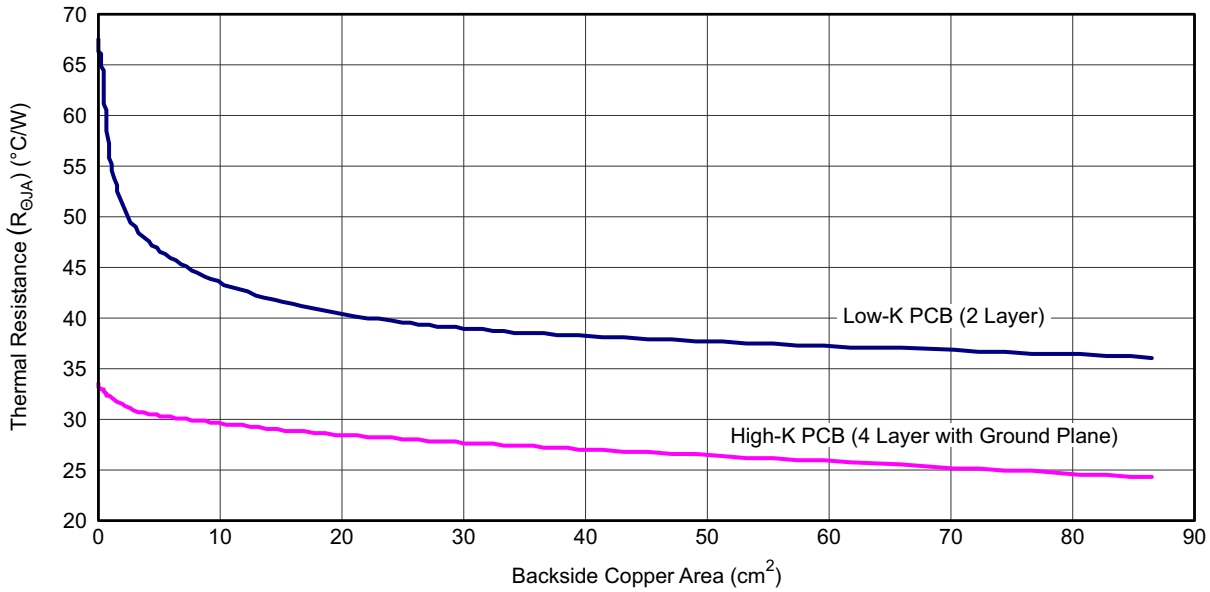


Figure 21. Thermal Resistance vs Copper Plane Area

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *PowerPAD™ Made Easy*, SLMA004
- *Current Recirculation and Decay Modes*, SLVA321
- *Calculating Motor Driver Power Dissipation*, SLVA504
- *Understanding Motor Driver Current Ratings*, SLVA505

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8823DCA	ACTIVE	HTSSOP	DCA	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8823	Samples
DRV8823DCAR	ACTIVE	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8823	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

OTHER QUALIFIED VERSIONS OF DRV8823 :

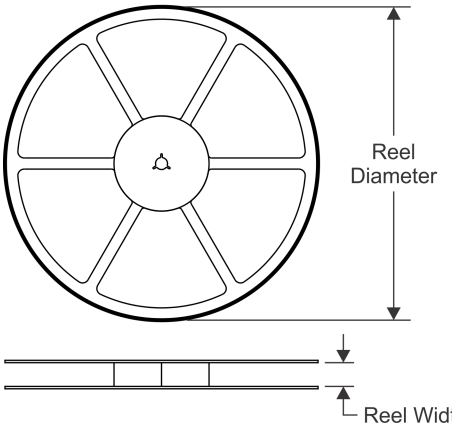
- Automotive: DRV8823-Q1

NOTE: Qualified Version Definitions:

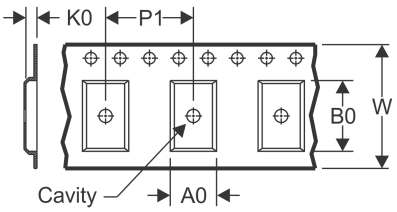
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

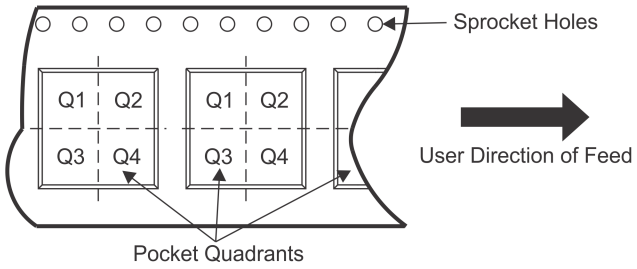


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

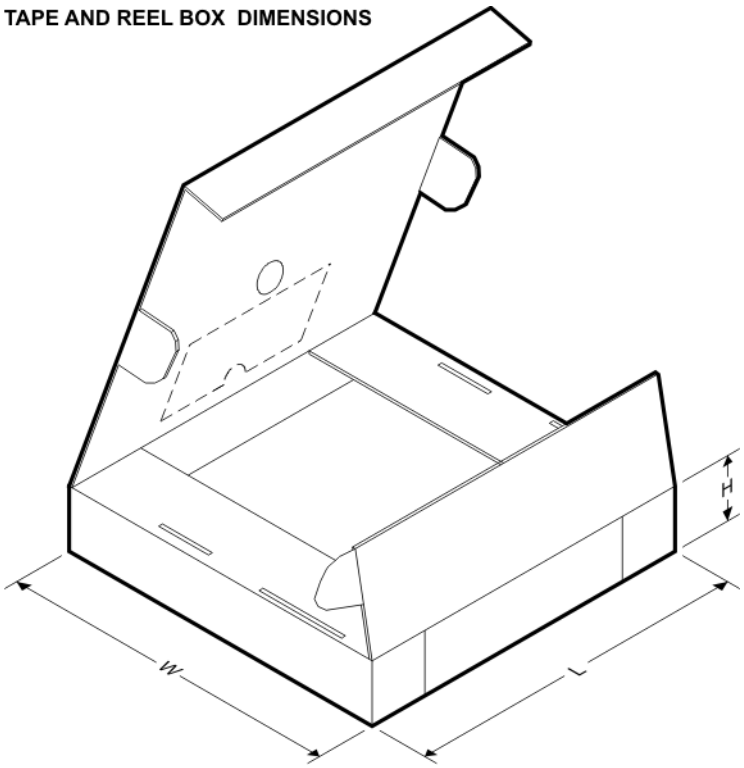
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8823DCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

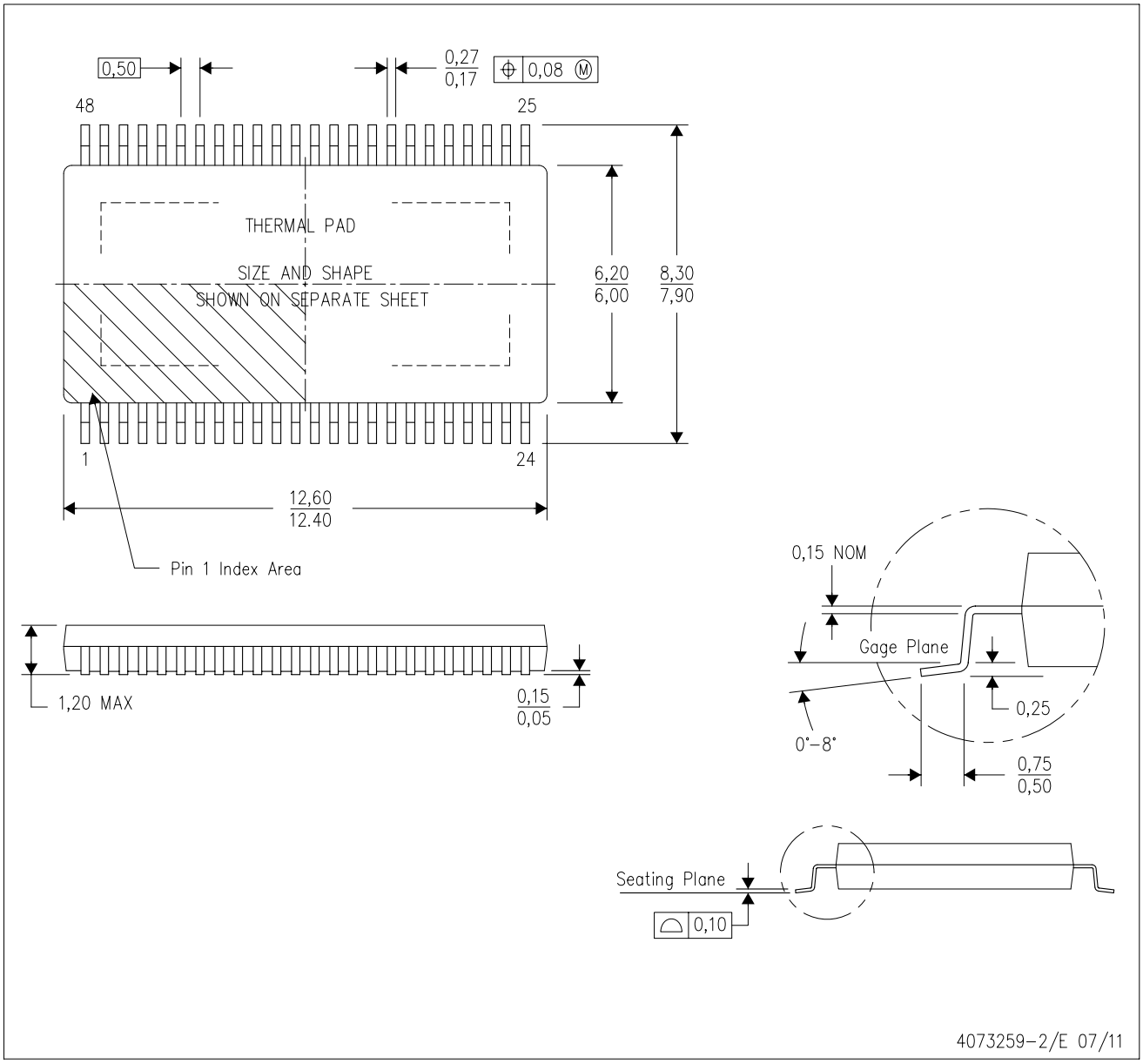
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8823DCAR	HTSSOP	DCA	48	2000	350.0	350.0	43.0

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

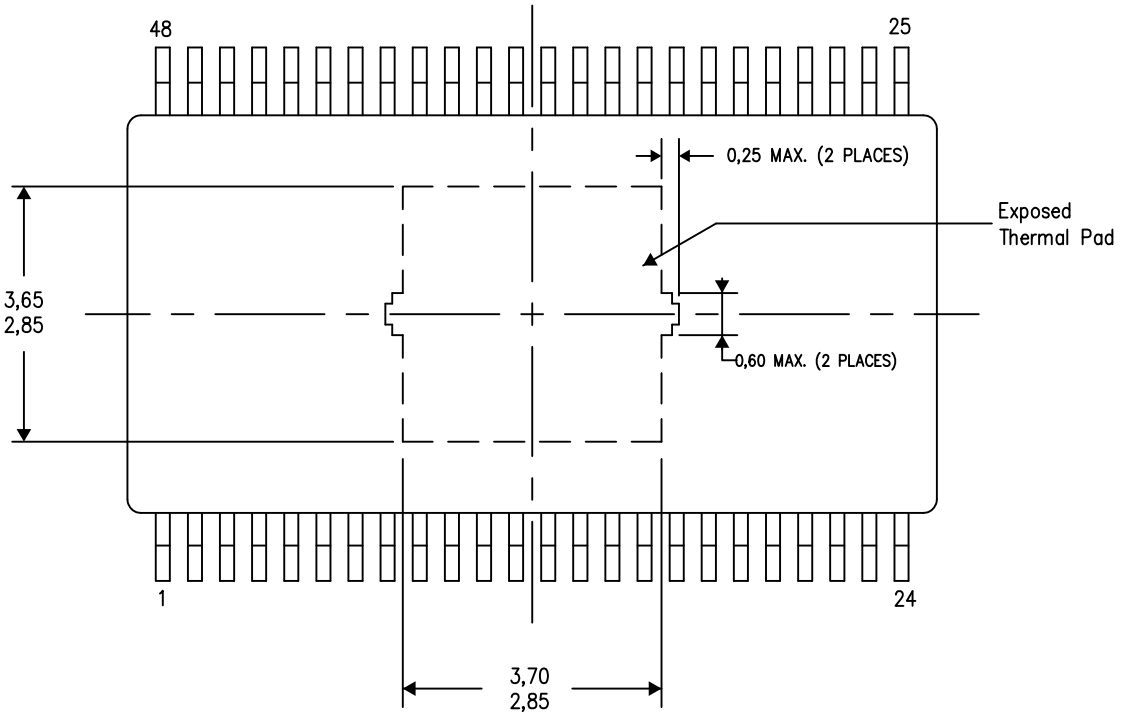
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

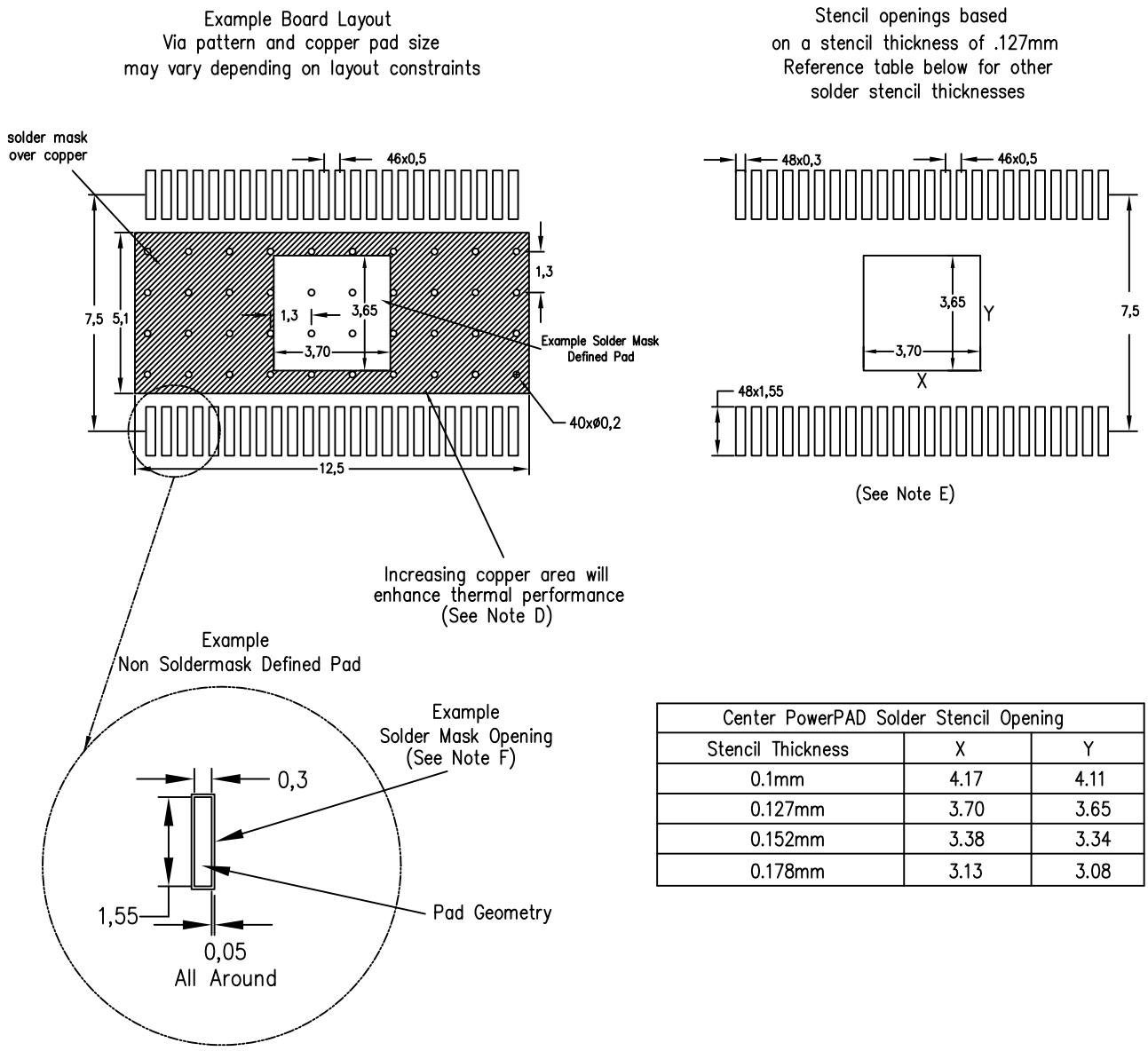
Exposed Thermal Pad Dimensions

4206320–6/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.17	4.11
0.127mm	3.70	3.65
0.152mm	3.38	3.34
0.178mm	3.13	3.08

4208546–5/H 11/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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