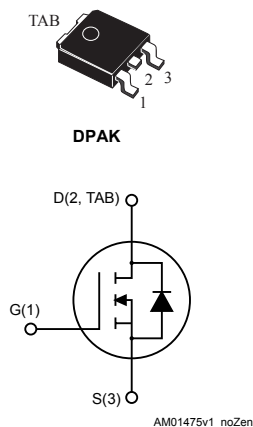


## N-channel 60 V, 6.8 mΩ typ., 40 A STripFET™ F7 Power MOSFET in a DPAK package



### Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------|--------------------------|----------------|
| STD80N6F7  | 60 V            | 8.0 mΩ                   | 40 A           |

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent FoM (figure of merit)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

| Product status  |               |
|-----------------|---------------|
| STD80N6F7       |               |
| Product summary |               |
| Order code      | STD80N6F7     |
| Marking         | 80N6F7        |
| Package         | DPAK          |
| Packing         | Tape and reel |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol            | Parameter                                                       | Value      | Unit             |
|-------------------|-----------------------------------------------------------------|------------|------------------|
| $V_{DS}$          | Drain-source voltage                                            | 60         | V                |
| $V_{GS}$          | Gate-source voltage                                             | $\pm 20$   | V                |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$  | 40         | A                |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 40         | A                |
| $I_{DM}^{(2)(1)}$ | Drain current (pulsed)                                          | 160        | A                |
| $P_{TOT}$         | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$           | 100        | W                |
| $E_{AS}^{(3)}$    | Single pulse avalanche energy                                   | 60         | mJ               |
| $dv/dt^{(4)}$     | Peak diode recovery                                             | 4.3        | V/ns             |
| $T_j$             | Operating junction temperature range                            | -55 to 175 | $^\circ\text{C}$ |
| $T_{stg}$         | Storage temperature range                                       |            |                  |

1. This value is limited by package
2. Pulse width limited by safe operating area
3. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_{AS} = 20\text{ A}$ ,  $V_{DD} = 40\text{ V}$ .
4.  $I_{SD} = 20\text{ A}$ ,  $di/dt = 700\text{ A}/\mu\text{s}$ ,  $V_{DD} = 48\text{ V}$ .

**Table 2. Thermal data**

| Symbol              | Parameter                        | Value | Unit                      |
|---------------------|----------------------------------|-------|---------------------------|
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 50    | $^\circ\text{C}/\text{W}$ |
| $R_{thj-case}$      | Thermal resistance junction-case | 1.5   | $^\circ\text{C}/\text{W}$ |

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$

## 2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

**Table 3. On/off-state**

| Symbol        | Parameter                         | Test conditions                                    | Min. | Typ. | Max. | Unit          |
|---------------|-----------------------------------|----------------------------------------------------|------|------|------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$        | 60   |      |      | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 60\text{ V}$     |      |      | 1    | $\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current         | $V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$     |      |      | 100  | nA            |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DD} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$ | 2    |      | 4    | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$       |      | 6.8  | 8.0  | m $\Omega$    |

**Table 4. Dynamic**

| Symbol    | Parameter                    | Test conditions                                                     | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|---------------------------------------------------------------------|------|------|------|------|
| $C_{iss}$ | Input capacitance            | $V_{DS} = 30\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$ | -    | 1600 | -    | pF   |
| $C_{oss}$ | Output capacitance           |                                                                     | -    | 800  | -    | pF   |
| $C_{rss}$ | Reverse transfer capacitance |                                                                     | -    | 50   | -    | pF   |
| $Q_g$     | Total gate charge            | $V_{DD} = 30\text{ V}$ , $I_D = 20\text{ A}$ ,                      | -    | 25   | -    | nC   |
| $Q_{gs}$  | Gate-source charge           | $V_{GS} = 0\text{ to }10\text{ V}$                                  | -    | 7.2  | -    | nC   |
| $Q_{gd}$  | Gate-drain charge            | (see Figure 13. Test circuit for gate charge behavior)              | -    | 8    | -    | nC   |

**Table 5. Switching times**

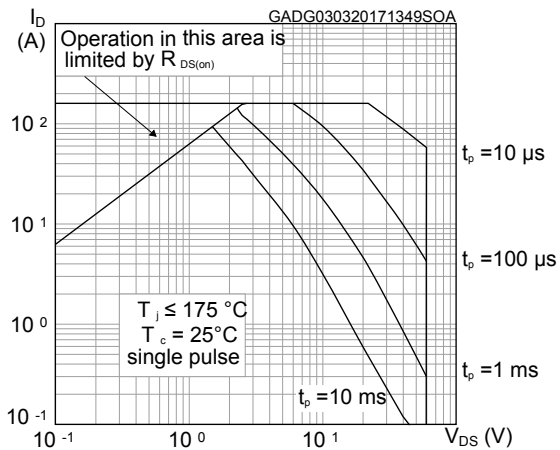
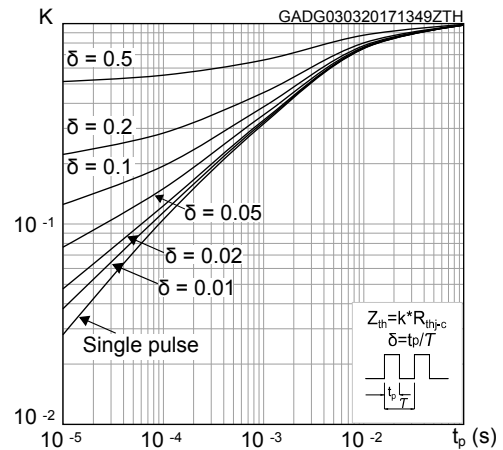
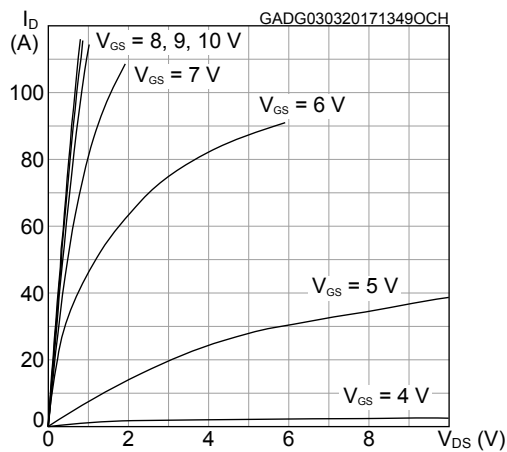
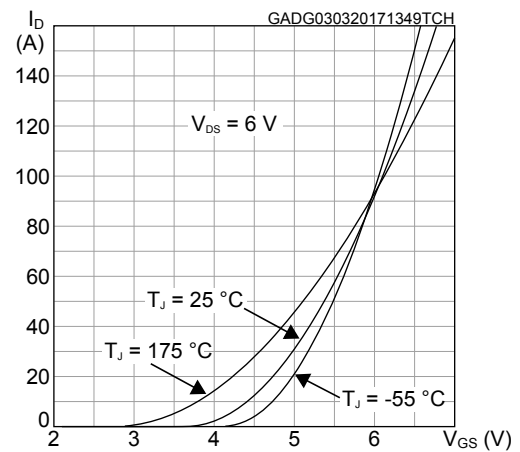
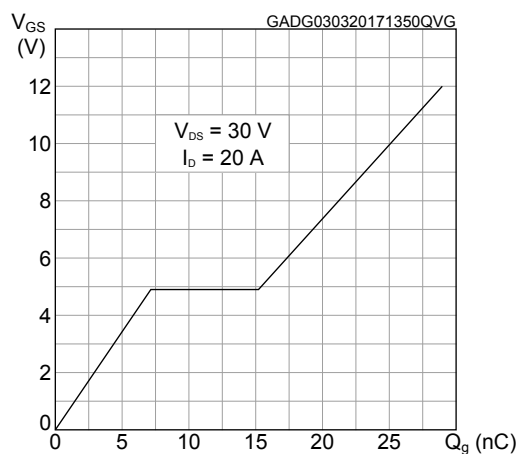
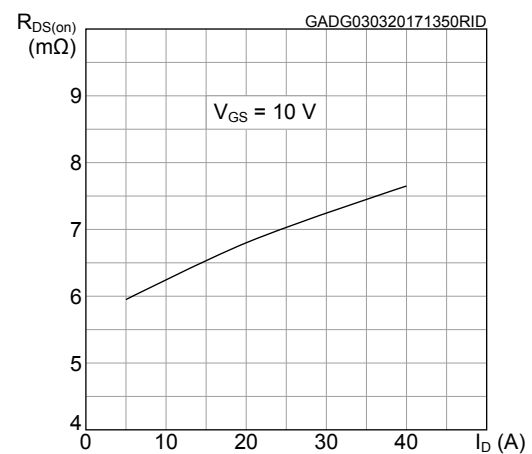
| Symbol       | Parameter           | Test conditions                                                                                                                                                                                              | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 30\text{ V}$ , $I_D = 20\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform) | -    | 15   | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                              | -    | 17.6 | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                              | -    | 24.4 | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                              | -    | 7.8  | -    | ns   |

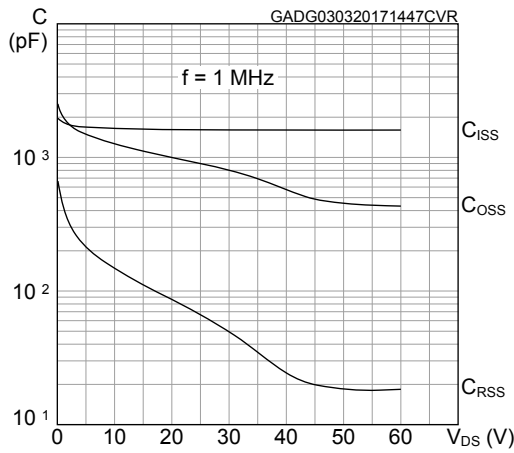
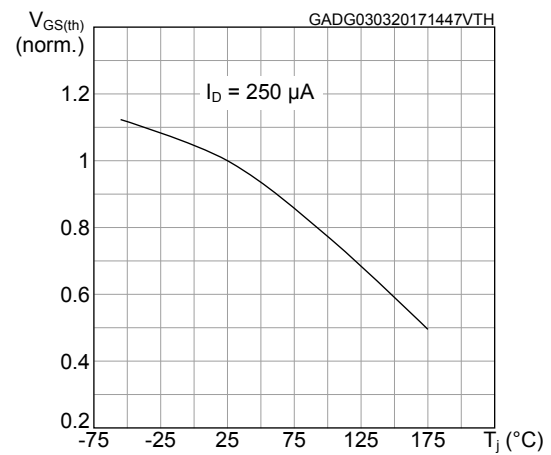
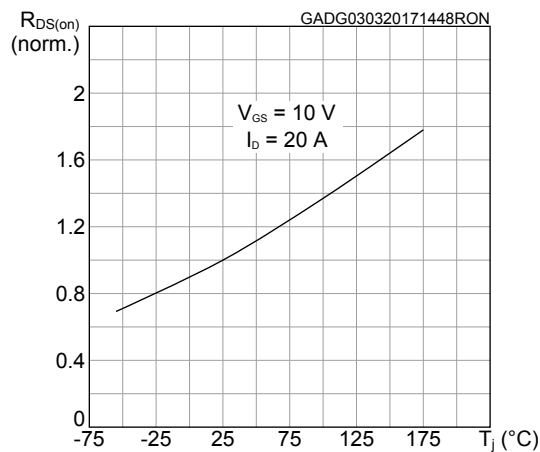
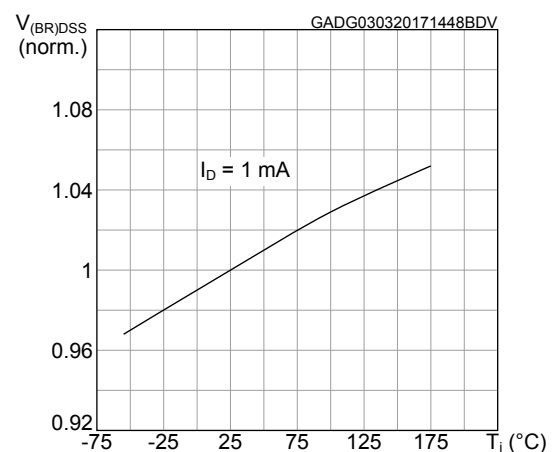
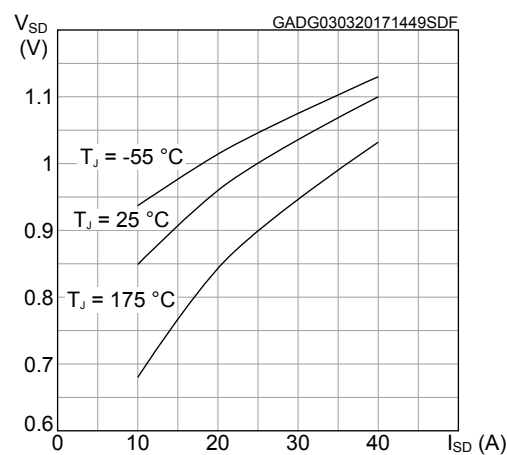
**Table 6. Source-drain diode**

| Symbol         | Parameter                | Test conditions                                                                     | Min. | Typ. | Max. | Unit |
|----------------|--------------------------|-------------------------------------------------------------------------------------|------|------|------|------|
| $V_{SD}^{(1)}$ | Forward on voltage       | $I_{SD} = 40\text{ A}$ , $V_{DD} = 0\text{ V}$                                      | -    |      | 1.2  | V    |
| $t_{rr}$       | Reverse recovery time    | $I_D = 40\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 48\text{ V}$   | -    | 39.6 |      | ns   |
| $Q_{rr}$       | Reverse recovery charge  | (see Figure 14. Test circuit for inductive load switching and diode recovery times) | -    | 36   |      | nC   |
| $I_{RRM}$      | Reverse recovery current |                                                                                     | -    | 1.8  |      | A    |

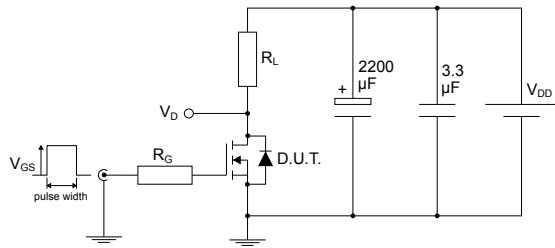
1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

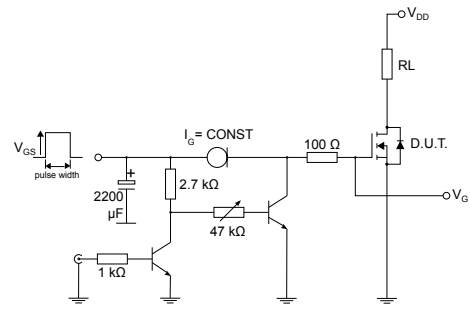
**Figure 1. Safe operating area**

**Figure 2. Normalized thermal impedance**

**Figure 3. Output characteristics**

**Figure 4. Transfer characteristics**

**Figure 5. Gate charge vs gate-source voltage**

**Figure 6. Static drain-source on-resistance**


**Figure 7. Capacitance variations**

**Figure 8. Normalized  $V_{GS(th)}$  vs temperature**

**Figure 9. Normalized on-resistance vs temperature**

**Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature**

**Figure 11. Source-drain diode forward characteristics**


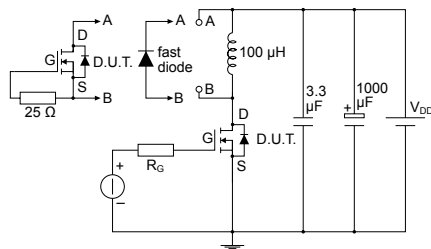
### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


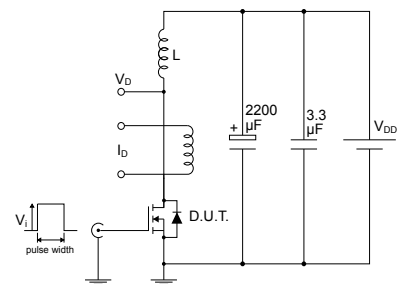
AM01468v1

**Figure 13. Test circuit for gate charge behavior**


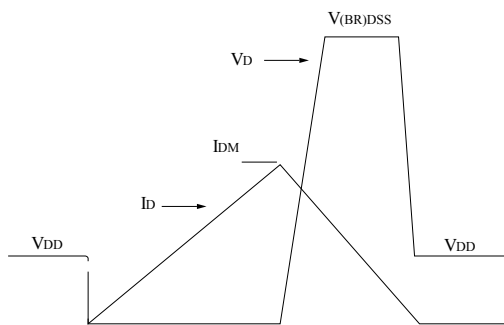
AM01469v10

**Figure 14. Test circuit for inductive load switching and diode recovery times**


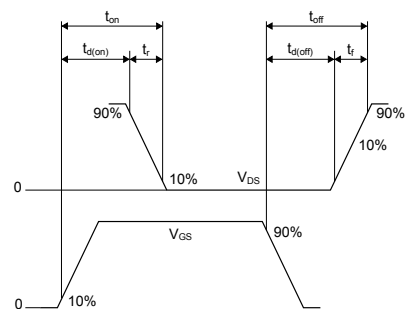
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**Figure 15. Unclamped inductive load test circuit**


AM01471v1

**Figure 16. Unclamped inductive waveform**


AM01472v1

**Figure 17. Switching time waveform**


AM01473v1

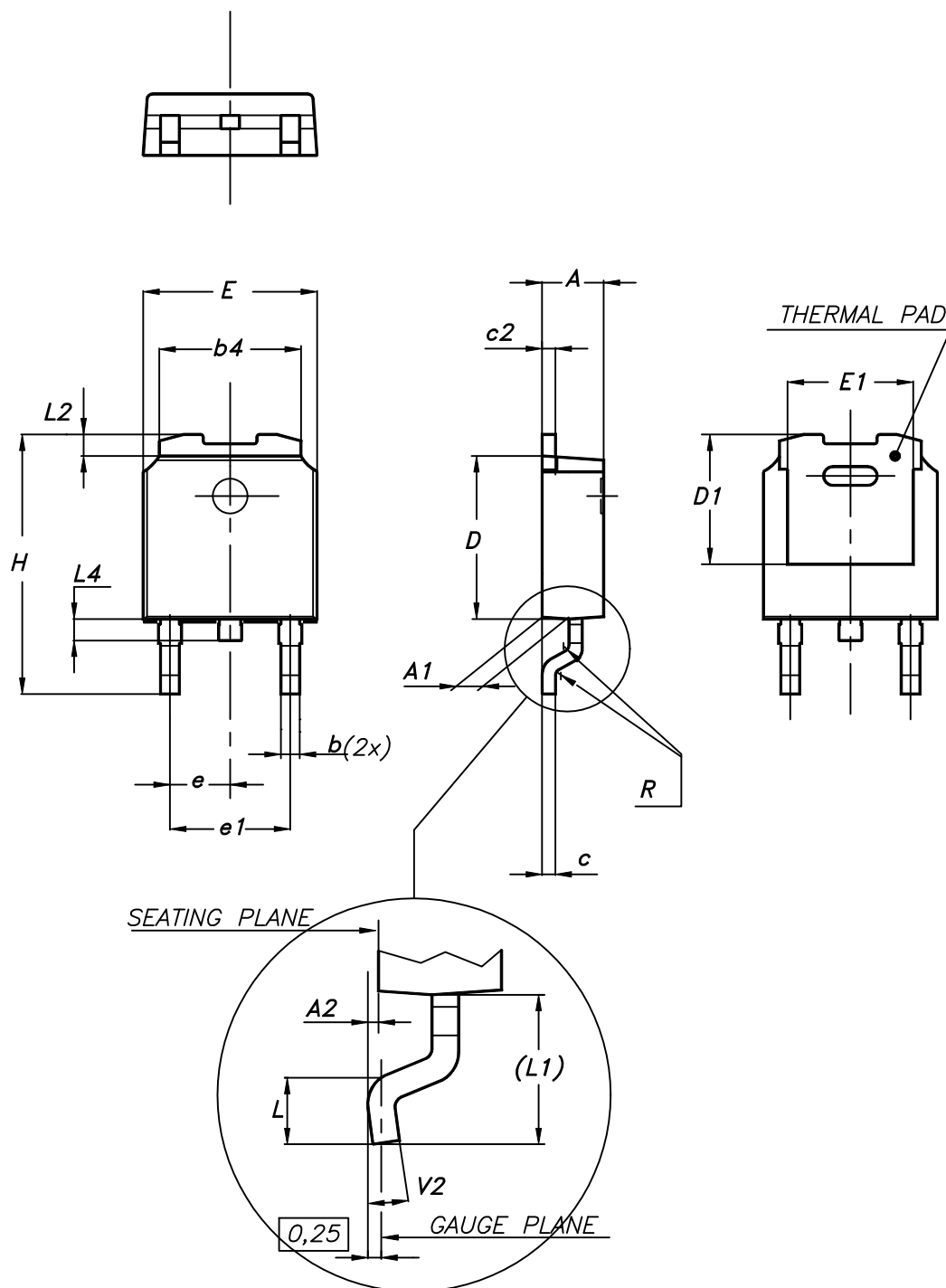
## **4 Package information**

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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

## 4.1 DPAK (TO-252) type A2 package information

Figure 18. DPAK (TO-252) type A2 package outline



0068772\_type-A2\_rev24

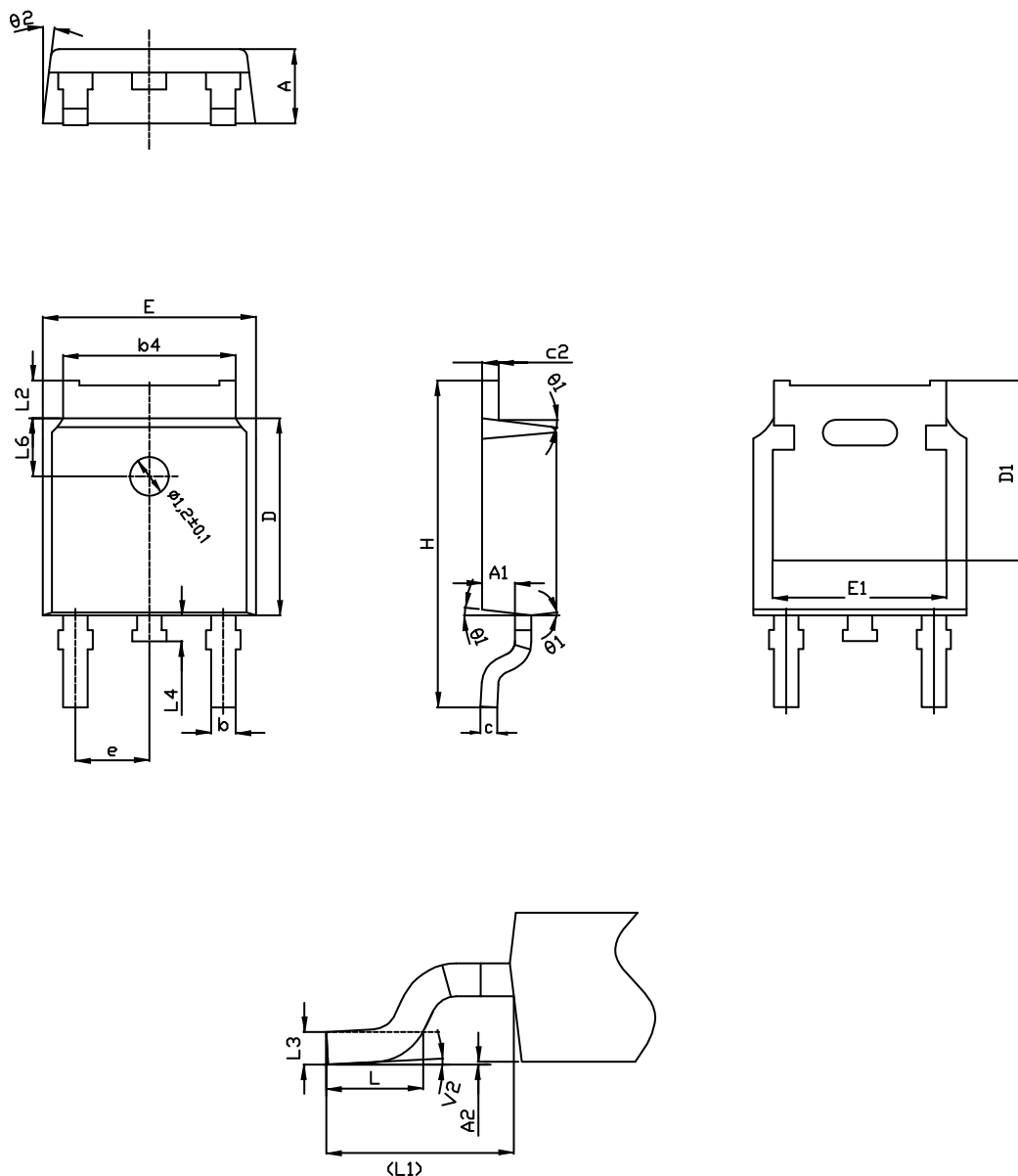


**Table 7. DPAK (TO-252) type A2 mechanical data**

| Dim. | mm   |      |       |
|------|------|------|-------|
|      | Min. | Typ. | Max.  |
| A    | 2.20 |      | 2.40  |
| A1   | 0.90 |      | 1.10  |
| A2   | 0.03 |      | 0.23  |
| b    | 0.64 |      | 0.90  |
| b4   | 5.20 |      | 5.40  |
| c    | 0.45 |      | 0.60  |
| c2   | 0.48 |      | 0.60  |
| D    | 6.00 |      | 6.20  |
| D1   | 4.95 | 5.10 | 5.25  |
| E    | 6.40 |      | 6.60  |
| E1   | 5.10 | 5.20 | 5.30  |
| e    | 2.16 | 2.28 | 2.40  |
| e1   | 4.40 |      | 4.60  |
| H    | 9.35 |      | 10.10 |
| L    | 1.00 |      | 1.50  |
| L1   | 2.60 | 2.80 | 3.00  |
| L2   | 0.65 | 0.80 | 0.95  |
| L4   | 0.60 |      | 1.00  |
| R    |      | 0.20 |       |
| V2   | 0°   |      | 8°    |

## 4.2 DPAK (TO-252) type C2 package information

Figure 19. DPAK (TO-252) type C2 package outline



0068772\_C2\_24

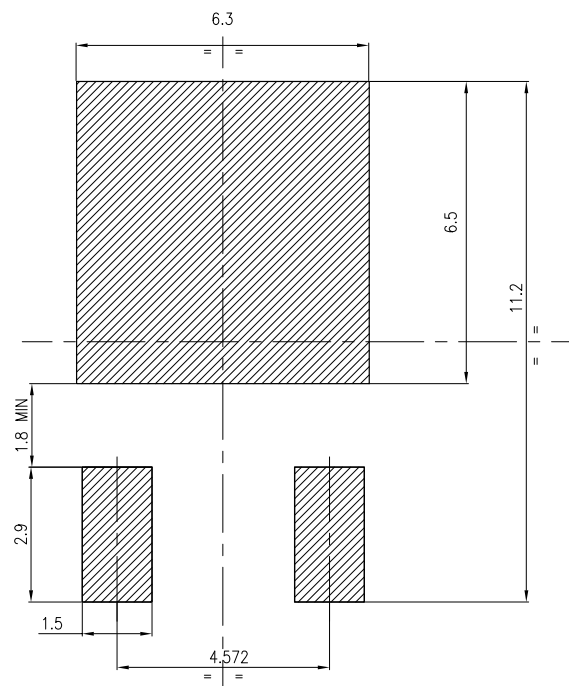
Table 8. DPAK (TO-252) type C2 mechanical data

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 2.20 | 2.30 | 2.38 |
| A1   | 0.90 | 1.01 | 1.10 |
| A2   | 0.00 |      | 0.10 |
| b    | 0.72 |      | 0.85 |
| b4   | 5.13 | 5.33 | 5.46 |

| Dim. | mm       |       |       |
|------|----------|-------|-------|
|      | Min.     | Typ.  | Max.  |
| c    | 0.47     |       | 0.60  |
| c2   | 0.47     |       | 0.60  |
| D    | 6.00     | 6.10  | 6.20  |
| D1   | 5.10     |       | 5.60  |
| E    | 6.50     | 6.60  | 6.70  |
| E1   | 5.20     |       | 5.50  |
| e    | 2.186    | 2.286 | 2.386 |
| H    | 9.80     | 10.10 | 10.40 |
| L    | 1.40     | 1.50  | 1.70  |
| L1   | 2.90 REF |       |       |
| L2   | 0.90     |       | 1.25  |
| L3   | 0.51 BSC |       |       |
| L4   | 0.60     | 0.80  | 1.00  |
| L6   | 1.80 BSC |       |       |
| θ1   | 5°       | 7°    | 9°    |
| θ2   | 5°       | 7°    | 9°    |
| V2   | 0°       |       | 8°    |

### 4.3 DPAK (TO-252) footprint information

**Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)**



FP\_0068772\_24

## Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                         |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 03-Nov-2016 | 1        | First release                                                                                                                                                                   |
| 03-Mar-2017 | 2        | Updated <i>Table 2: "Absolute maximum ratings"</i> and <i>Table 5: "Dynamic"</i> .<br>Added Section 2.1: " <i>Electrical characteristics (curves)</i> ".<br>Minor text changes. |
| 02-May-2017 | 3        | Updated <i>Table 2: "Absolute maximum ratings"</i> .                                                                                                                            |
| 01-Feb-2018 | 4        | Added DPAK (TO-252) type C package information.<br>Removed maturity status indication from cover page.                                                                          |
| 12-Feb-2018 | 5        | Modified <a href="#">Section 4 Package information</a> .<br>Minor text changes.                                                                                                 |

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