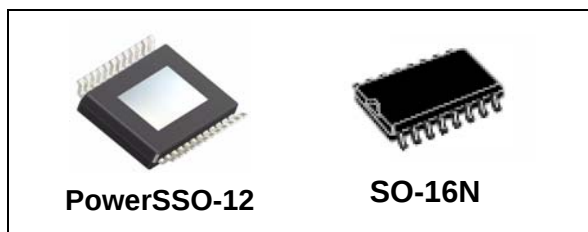


Double channel high-side driver with analog current sense for 24 V automotive applications

Datasheet - production data



Features

Max transient supply voltage	V_{CC}	58 V
Operating voltage range	V_{CC}	8 to 36 V
Typ on-state resistance (per ch.)	R_{ON}	100 m Ω
Current limitation (typ)	I_{LIM}	22 A
Off-state supply current	I_S	2 μ A ⁽¹⁾

1. Typical value with all loads connected.

- AEC-Q100 qualified
- General
 - Very low standby current
 - 3.0 V CMOS compatible input
 - Optimized electromagnetic emission
 - Very low electromagnetic susceptibility
 - Compliant with European directive 2002/95/EC
 - Fault reset standby pin (FR_Stby)
 - Optimized for LED application
- Diagnostic functions
 - Proportional load current sense
 - High current sense precision for wide range currents
 - Off-state open-load detection
 - Output short to V_{CC} detection
 - Overload and short to ground latch-off
 - Thermal shutdown latch-off
 - Very low current sense leakage



- Protection
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients
 - Protection against loss of ground and loss of V_{CC}
 - Thermal shutdown
 - Electrostatic discharge protection

Application

All types of resistive, inductive and capacitive loads

Description

The VND5T100LAJ-E and VND5T100LAS-E are monolithic devices made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the devices against low energy spikes.

These devices integrate an analog current sense which delivers a current proportional to the load current.

Fault conditions such as overload, overtemperature or short to V_{CC} are reported via the current sense pin.

Output current limitation protects the devices in overload condition. The devices latch off in case of overload or thermal shutdown.

The devices are reset by a low level pass on the fault reset standby pin.

A permanent low level on the inputs and fault reset standby pin disables all outputs and sets the devices in standby mode.

Contents

1	Block diagram and pin description	5
2	Electrical specifications	7
2.1	Absolute maximum ratings	7
2.2	Thermal data	8
2.3	Electrical characteristics	9
2.4	Electrical characteristics curves	19
3	Application information	21
3.1	GND protection network against reverse battery	21
3.1.1	Solution 1: resistor in the ground line (RGND only)	21
3.1.2	Solution 2: diode (DGND) in the ground line	22
3.2	Load dump protection	22
3.3	MCU I/Os protection	22
3.4	Maximum demagnetization energy ($V_{CC} = 24\text{ V}$)	23
4	Package and PCB thermal data	24
4.1	PowerSSO-12 thermal data	24
4.2	SO-16N thermal data	27
5	Package and packing information	30
5.1	ECOPACK®	30
5.2	PowerSSO-12 mechanical data	30
5.3	SO-16N package information	32
6	Packing information	34
6.1	PowerSSO-12 packing information	34
6.2	SO-16N packing information	35
7	Order code	36
8	Revision history	37

List of tables

Table 1.	Pin function	5
Table 2.	Suggested connections for unused and not connected pins	6
Table 3.	Absolute maximum ratings	7
Table 4.	Thermal data.	8
Table 5.	Power section	9
Table 6.	Switching ($V_{CC} = 24\text{ V}$; $T_j = 25\text{ °C}$)	9
Table 7.	Logic inputs.	9
Table 8.	Protections and diagnostics	11
Table 9.	Current sense ($8\text{ V} < V_{CC} < 36\text{ V}$)	12
Table 10.	Open-load detection	13
Table 11.	Truth table.	17
Table 12.	Electrical transient requirements (part 1)	18
Table 13.	Electrical transient requirements (part 2)	18
Table 14.	Electrical transient requirements (part 3)	18
Table 15.	Thermal parameters	26
Table 16.	Thermal parameters	29
Table 17.	PowerSSO-12 mechanical data	31
Table 18.	SO-16N mechanical data	33
Table 19.	Device summary	36
Table 20.	Document revision history	37

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram PowerSSO-12 (top view)	6
Figure 3.	Configuration diagram SO-16N (top view)	6
Figure 4.	Current and voltage conventions	7
Figure 5.	T_{standby} definition	10
Figure 6.	T_{reset} definition	11
Figure 7.	Current sense delay characteristics	13
Figure 8.	Open-load off-state delay timing	14
Figure 9.	Switching characteristics	14
Figure 10.	Output stuck to V_{CC} detection delay time at FR_{STBY} activation	15
Figure 11.	Delay response time between rising edge of FR_{STBY} current and rising edge of current sense	15
Figure 12.	Output voltage drop limitation	16
Figure 13.	Device behavior in overload condition	16
Figure 14.	Off-state output current	19
Figure 15.	High level input current	19
Figure 16.	Input clamp voltage	19
Figure 17.	Input high level voltage	19
Figure 18.	Input low level voltage	19
Figure 19.	Input hysteresis voltage	19
Figure 20.	On-state resistance vs T_{case}	20
Figure 21.	On-state resistance vs V_{CC}	20
Figure 22.	I_{LIMH} vs T_{case}	20
Figure 23.	Turn-on voltage slope	20
Figure 24.	Turn-off voltage slope	20
Figure 25.	Application schematic	21
Figure 26.	Maximum turn-off current versus inductance	23
Figure 27.	PowerSSO-12 PC board	24
Figure 28.	$R_{\text{thj-amb}}$ vs PCB copper area in open box free air condition (one channel ON)	24
Figure 29.	PowerSSO-12 thermal impedance junction ambient single pulse (one channel ON)	25
Figure 30.	Thermal fitting model of a double channel HSD in PowerSSO-12	25
Figure 31.	SO-16N PC board	27
Figure 32.	$R_{\text{thj-amb}}$ vs PCB copper area in open box free air condition (one channel ON)	27
Figure 33.	SO-16N thermal impedance junction ambient single pulse (one channel on)	28
Figure 34.	Thermal fitting model of a double channel HSD in SO-16N	28
Figure 35.	PowerSSO-12 package dimensions	30
Figure 36.	SO-16N package dimensions	32
Figure 37.	PowerSSO-12 tube shipment (no suffix)	34
Figure 38.	PowerSSO-12 tape and reel shipment (suffix "TR")	34
Figure 39.	SO-16N tube shipment (no suffix)	35
Figure 40.	SO-16N tape and reel shipment (suffix "TR")	35

1 Block diagram and pin description

Figure 1. Block diagram

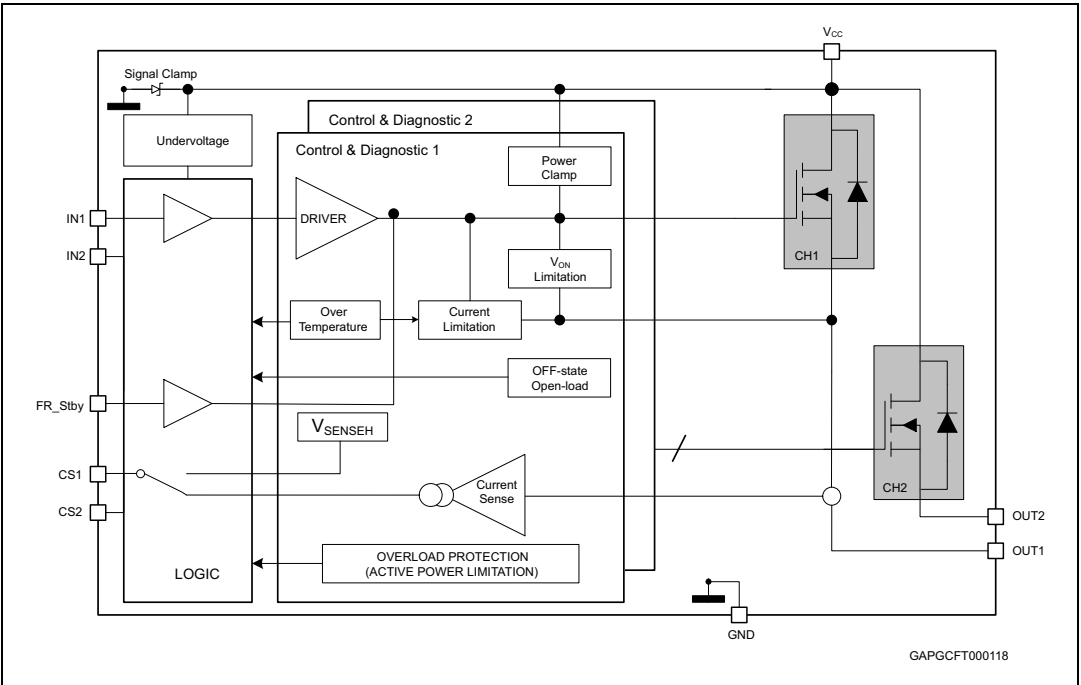


Table 1. Pin function

Name	Function
V _{CC}	Battery connection
OUTn	Power output
GND	Ground connection
INn	Voltage controlled input pin with hysteresis, CMOS compatible. It controls output switch state
CSn	Analog current sense pin, it delivers a current proportional to the load current
FR_Stby	In case of latch-off for overtemperature/overcurrent condition, a low pulse on the FR_Stby pin is needed to reset the channel. The device enters in standby mode if all inputs and the FR_Stby pin are low.

Figure 2. Configuration diagram PowerSSO-12 (top view)

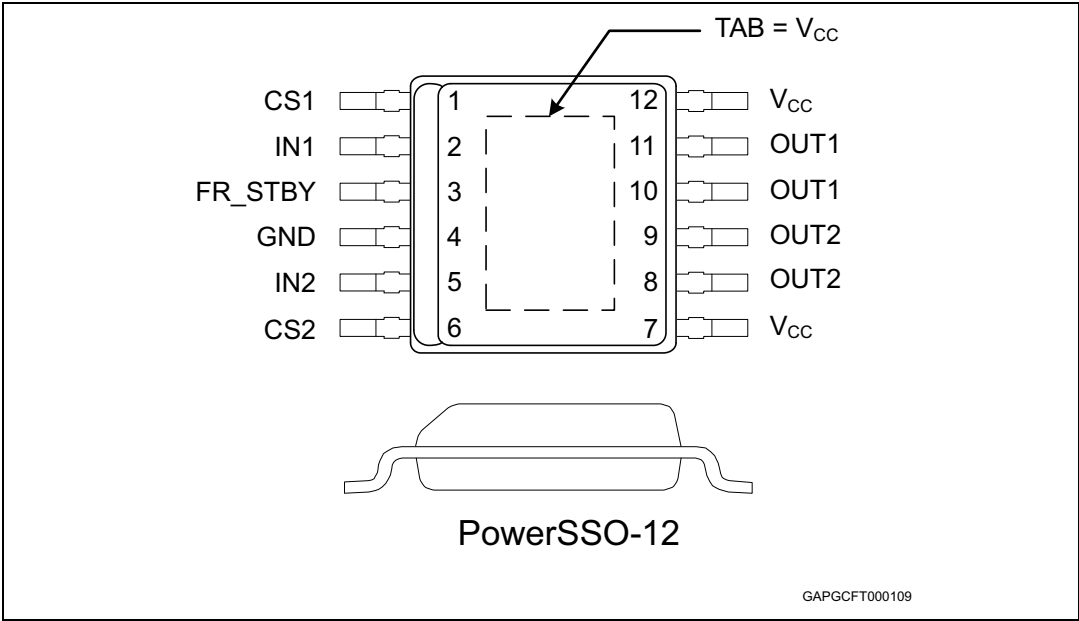


Figure 3. Configuration diagram SO-16N (top view)

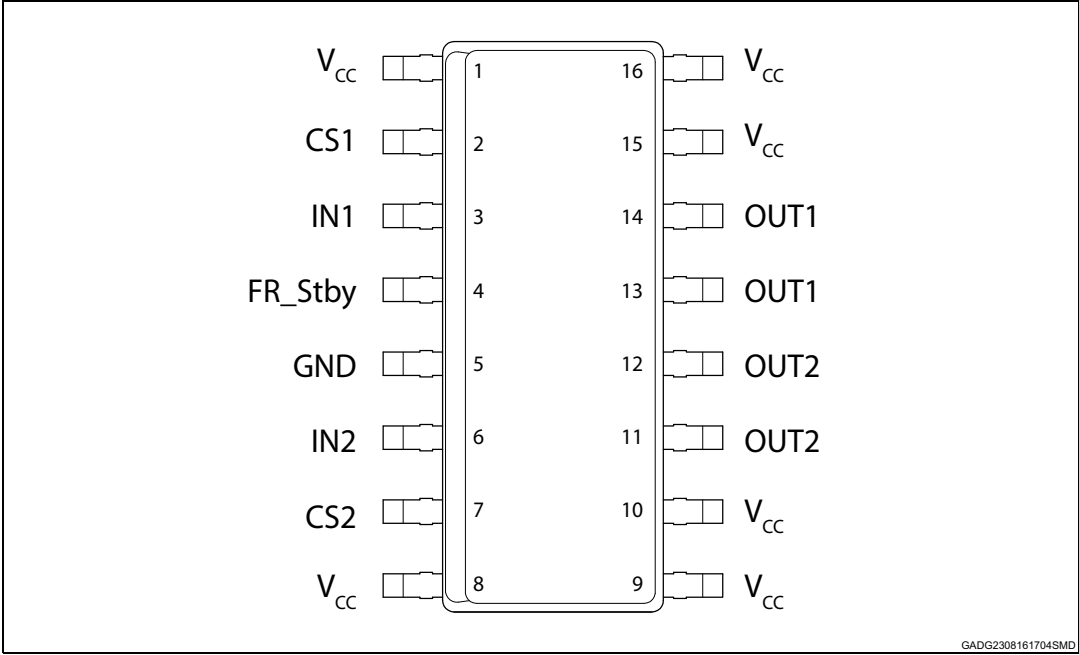


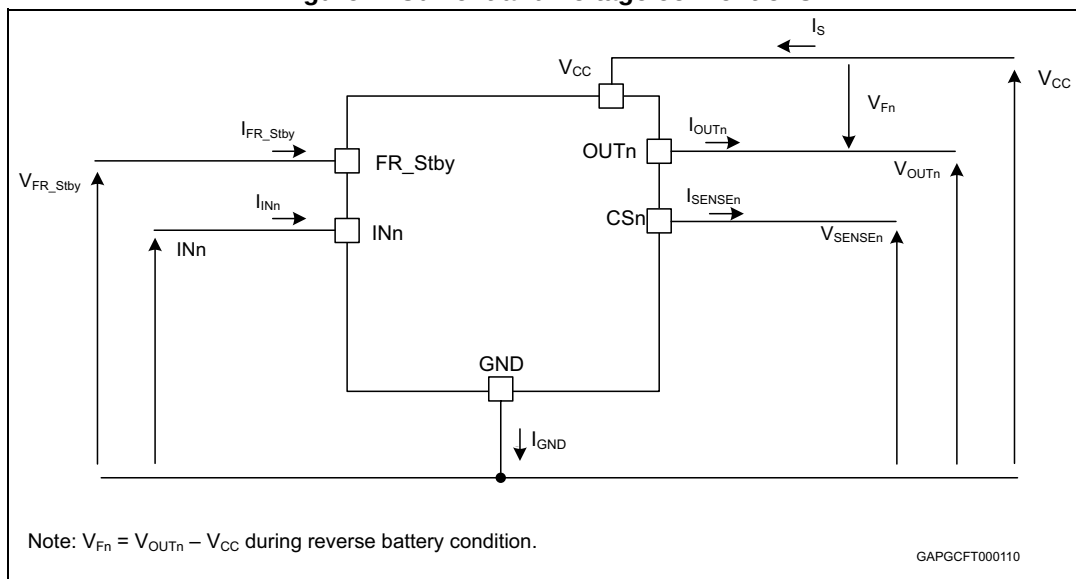
Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	FR_Stby
Floating	Not allowed	X ⁽¹⁾	X	X	X
To ground	Through 10 KΩ resistor	X	Not allowed	Through 10 KΩ resistor	Through 10 KΩ resistor

1. X: do not care.

2 Electrical specifications

Figure 4. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the ratings listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	58	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	20	A
I_{IN}	DC input current	-1 to 10	mA
I_{FR_Stby}	Fault reset standby DC input current	-1 to 1.5	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC} - 58$ to $+V_{CC}$	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy ($L = 1.9 \text{ mH}$; $V_{bat} = 32 \text{ V}$; $T_{jstart} = 150^\circ\text{C}$; $I_{OUT} = I_{limL} \text{ (Typ)}$)	70	mJ
V_{ESD}	Electrostatic discharge (Human Body Model: $R = 1.5 \text{ K}\Omega$; $C = 100 \text{ pF}$)		
	– INPUT	4000	V
	– CURRENT SENSE	2000	V
	– FR_STBY	4000	V
	– OUTPUT	5000	V
	– V_{CC}	5000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
L_{Smax}	Maximum stray inductance in short circuit $R_L = 300 \text{ m}\Omega$, $V_{bat} = 32 \text{ V}$, $T_{jstart} = 150^\circ\text{C}$, $I_{OUT} = I_{limHmax}$	40	μH

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Maximum value		Unit
		PowerSSO-12	SO-16N	
$R_{thj-case}$	Thermal resistance junction-case (with one channel ON)	6	—	$^\circ\text{C/W}$
$R_{thj-pin}$	Thermal resistance junction-pin (with one channel ON)	—	26	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	See Figure 28	See Figure 32	$^\circ\text{C/W}$

2.3 Electrical characteristics

8 V < V_{CC} < 36 V; -40°C < T_j < 150°C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		8	24	36	V
V_{USD}	Undervoltage shutdown			3.5	5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance ⁽¹⁾	$I_{OUT} = 1.5\text{ A}; T_j = 25^\circ\text{C}$		100		mΩ
		$I_{OUT} = 1.5\text{ A}; T_j = 150^\circ\text{C}$			200	
V_{clamp}	Clamp voltage	$I_S = 20\text{ mA}$	58	64	70	V
I_S	Supply current	Off-state: $V_{CC} = 24\text{ V}; T_j = 25^\circ\text{C}; V_{IN} = V_{OUT} = V_{SENSE} = 0\text{ V}$		2 ⁽²⁾	5 ⁽²⁾	μA
		On-state: $V_{CC} = 24\text{ V}; V_{IN} = 5\text{ V}; I_{OUT} = 0\text{ A}$		4.2	6	mA
$I_{L(off)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}; V_{CC} = 24\text{ V}; T_j = 25^\circ\text{C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}; V_{CC} = 24\text{ V}; T_j = 125^\circ\text{C}$	0		5	
V_F	Output - V_{CC} diode voltage	$-I_{OUT} = 1.5\text{ A}; T_j = 150^\circ\text{C}$			0.7	V

1. For each channel.

2. PowerMos leakage included

Table 6. Switching ($V_{CC} = 24\text{ V}; T_j = 25^\circ\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 16\ \Omega$		27		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 16\ \Omega$		38		μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 16\ \Omega$		1		V/μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 16\ \Omega$		0.65		V/μs
W_{ON}	Switching energy losses during t_{won}	$R_L = 16\ \Omega$		0.23		mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 16\ \Omega$		0.26		mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	Input high level voltage		2.1			V

Table 7. Logic inputs (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{IH}	High level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		V
$V_{FR_Stby_L}$	Fault_reset_standby low level voltage				0.9	V
$I_{FR_Stby_L}$	Low level fault_reset_standby current	$V_{FR_Stby} = 0.9\text{ V}$	1			μA
$V_{FR_Stby_H}$	Fault_reset_standby high level voltage		2.1			V
$I_{FR_Stby_H}$	High level fault_reset_standby current	$V_{FR_Stby} = 2.1\text{ V}$			10	μA
$V_{FR_Stby(hyst)}$	Fault_reset_standby hysteresis voltage		0.25			V
$V_{FR_Stby_CL}$	Fault_reset_standby clamp voltage	$I_{FR_Stby} = 15\text{ mA}$ ($t < 10\text{ ms}$)	11		15	V
		$I_{FR_Stby} = -1\text{ mA}$		-0.7		V
t_{reset}	Overload latch-off reset time	See Figure 5	2		24	μs
t_{stby}	Standby delay	See Figure 6	120		1200	μs

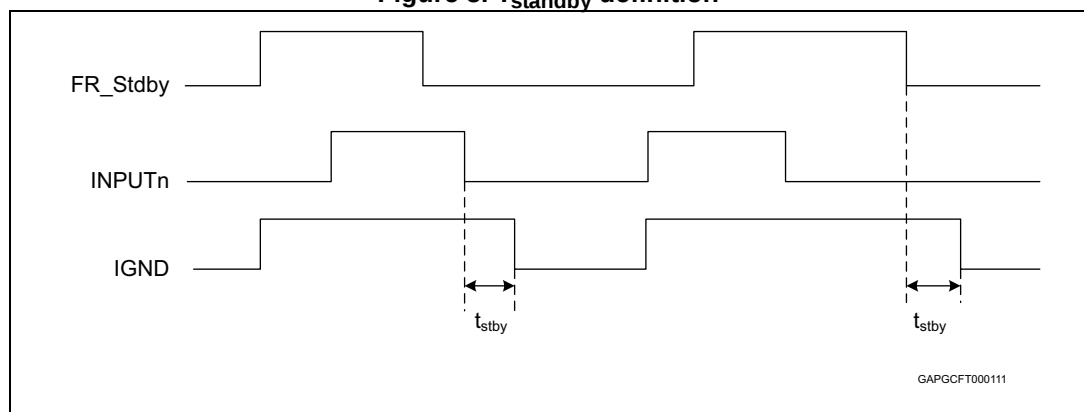
Figure 5. $T_{standby}$ definition

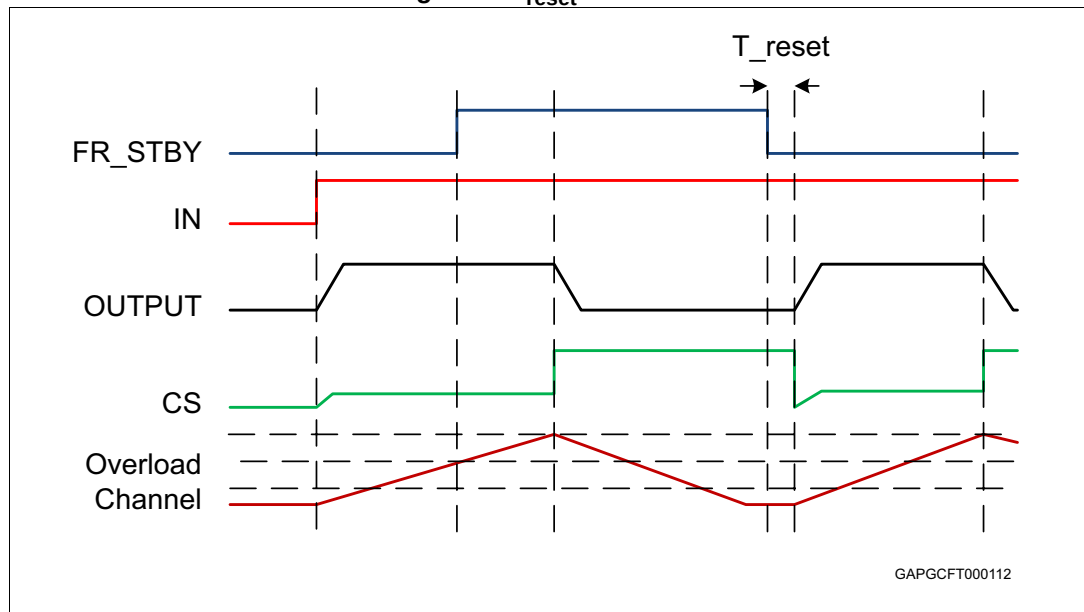
Figure 6. T_{reset} definition

Table 8. Protections and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	$V_{\text{CC}} = 24 \text{ V}$	16	22	30	A
		$5 \text{ V} < V_{\text{CC}} < 36 \text{ V}$			30	A
I_{limL}	Short circuit current during thermal cycling	$V_{\text{CC}} = 24 \text{ V};$ $T_{\text{R}} < T_{\text{j}} < T_{\text{TSD}}$		6		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_{R}	Reset temperature		$T_{\text{RS}} + 1$	$T_{\text{RS}} + 5$		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis ($T_{\text{TSD}} - T_{\text{R}}$)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	$I_{\text{OUT}} = 1.5 \text{ A}; V_{\text{IN}} = 0;$ $L = 6 \text{ mH}$	$V_{\text{CC}} - 58$	$V_{\text{CC}} - 64$	$V_{\text{CC}} - 70$	V
V_{ON}	Output voltage drop limitation	$I_{\text{OUT}} = 50 \text{ mA};$ $T_{\text{j}} = -40^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$		25		mV

Table 9. Current sense (8 V < V_{CC} < 36 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K _{OL}	I _{OUT} /I _{SENSE}	I _{OUT} = 12 mA; V _{SENSE} = 0.5 V; T _j = -40°C to 150°C	833			
K _{LED}	I _{OUT} /I _{SENSE}	I _{OUT} = 50 mA; V _{SENSE} = 0.5 V; T _j = -40°C to 150°C	1328	2190	3332	
dK _{LED} /K _{LED(TOT)} ⁽¹⁾	Current sense ratio drift	I _{OUT} = 12 mA to 25 mA; I _{CAL} = 18 mA; V _{SENSE} = 0.5 V; T _j = -40°C to 150°C	-30		30	%
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} = 100 mA; V _{SENSE} = 0.5 V; T _j = -40°C to 150°C	1170	1950	2730	
dK ₀ /K ₀ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 100 mA; V _{SENSE} = 0.5 V; T _j = -40°C to 150°C	-18		18	%
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 0.4 A; V _{SENSE} = 1 V; T _j = -40°C to 150°C	1259	1740	2191	
dK ₁ /K ₁ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 0.4 A; V _{SENSE} = 1 V; T _j = -40°C to 150°C	-15		15	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 0.8 A; V _{SENSE} = 2 V; T _j = -40°C to 150°C	1372	1730	2058	
dK ₂ /K ₂ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 0.8 A; V _{SENSE} = 2 V; T _j = -40°C to 150°C	-12		12	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 1.6 A; V _{SENSE} = 2 V; T _j = -40°C to 150°C	1509	1720	1921	
dK ₃ /K ₃ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 1.6 A; V _{SENSE} = 2 V; T _j = -40°C to 150°C	-8		8	%
K ₄	I _{OUT} /I _{SENSE}	I _{OUT} = 6 A; V _{SENSE} = 4 V; T _j = -40°C to 150°C	1646	1720	1784	
dK ₄ /K ₄ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 6 A; V _{SENSE} = 4 V; T _j = -40°C to 150°C	-4		4	%
I _{SENSE0}	Analog sense leakage current	I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{IN} = 0 V; T _j = -40 °C to 150 °C	0		1	μA
		I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{IN} = 5 V; T _j = -40 °C to 150 °C	0		2	μA
V _{SENSE}	Max analog sense output voltage	I _{OUT} = 6 A; R _{SENSE} = 3.9 KΩ	5			V
V _{SENSEH}	Analog sense output voltage in fault condition ⁽²⁾	V _{CC} = 24 V; R _{SENSE} = 3.9 KΩ	7.5	8.5	9.5	V
I _{SENSEH}	Analog sense output current in fault condition ⁽²⁾	V _{CC} = 24 V; V _{SENSE} = 5 V	4.9	9	12	mA
t _{DSENSE2H}	Delay response time from rising edge of INPUT pin	V _{SENSE} < 4 V; 0.07 A < I _{OUT} < 6 A; I _{SENSE} = 90 % of I _{SENSE max} (see Figure 7)		100	200	μs

Table 9. Current sense (8 V < V_{CC} < 36 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\Delta t_{\text{DSSENSE2H}}$	Delay response time between rising edge of output current and rising edge of current sense	$V_{\text{SENSE}} < 4 \text{ V}$; $I_{\text{SENSE}} = 90 \% \text{ of } I_{\text{SENSEMAX}}$; $I_{\text{OUT}} = 90 \% \text{ of } I_{\text{OUTMAX}}$; $I_{\text{OUTMAX}} = 1.5 \text{ A}$ (see Figure 12)			150	μs
$t_{\text{DSSENSE2L}}$	Delay response time from falling edge of INPUT pin	$V_{\text{SENSE}} < 4 \text{ V}$; $0.07 \text{ A} < I_{\text{OUT}} < 6 \text{ A}$; $I_{\text{SENSE}} = 10 \% \text{ of } I_{\text{SENSE max}}$ (see Figure 7)		5	20	μs

- Parameter guaranteed by design; it is not tested.
- Fault condition includes: power limitation, overtemperature and open-load in OFF-state condition.

Table 10. Open-load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load off-state voltage detection threshold	$V_{\text{IN}} = 0 \text{ V}$; $8 \text{ V} < V_{\text{CC}} < 36 \text{ V}$; $F_{\text{R_STBY}} = 5 \text{ V}$	2	—	4	V
t_{DSTKON}	Output short circuit to V _{CC} detection delay at turn off	See Figure 7 ; $F_{\text{R_STBY}} = 5 \text{ V}$	180	—	1800	μs
$t_{\text{DFRSTK_ON}}$	Output short circuit to V _{CC} detection delay at FRSTBY activation	See Figure 10 ; Input _{1,2} = low		—	50	μs
$I_{\text{L(off2)}}$	Off-state output current at V _{OUT} = 4V	$V_{\text{IN}} = 0 \text{ V}$; $V_{\text{SENSE}} = 0 \text{ V}$; V_{OUT} rising from 0 V to 4 V; $F_{\text{R_STBY}} = 5 \text{ V}$	-120	—	0	μA
$t_{\text{d_vol}}$	Delay response from output rising edge to V _{SENSE} rising edge in open-load	$V_{\text{OUT}} = 4 \text{ V}$; $V_{\text{IN}} = 0 \text{ V}$; $V_{\text{SENSE}} = 90 \% \text{ of } V_{\text{SENSEH}}$; $R_{\text{SENSE}} = 3.9 \text{ K}\Omega$; $F_{\text{R_STBY}} = 5 \text{ V}$		—	20	μs

Figure 7. Current sense delay characteristics

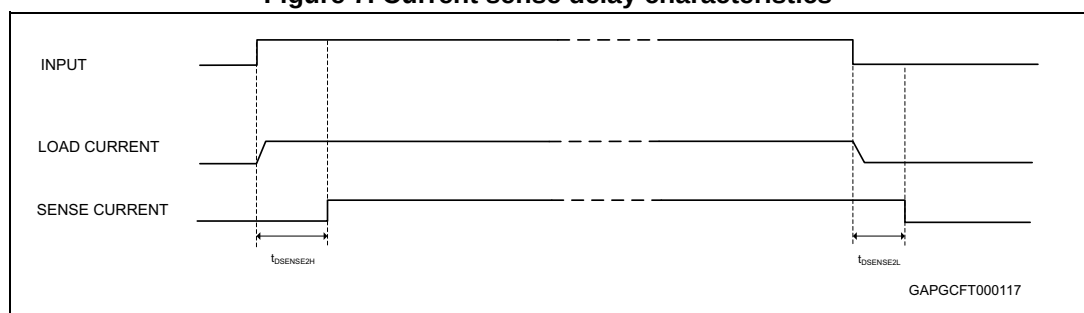


Figure 8. Open-load off-state delay timing

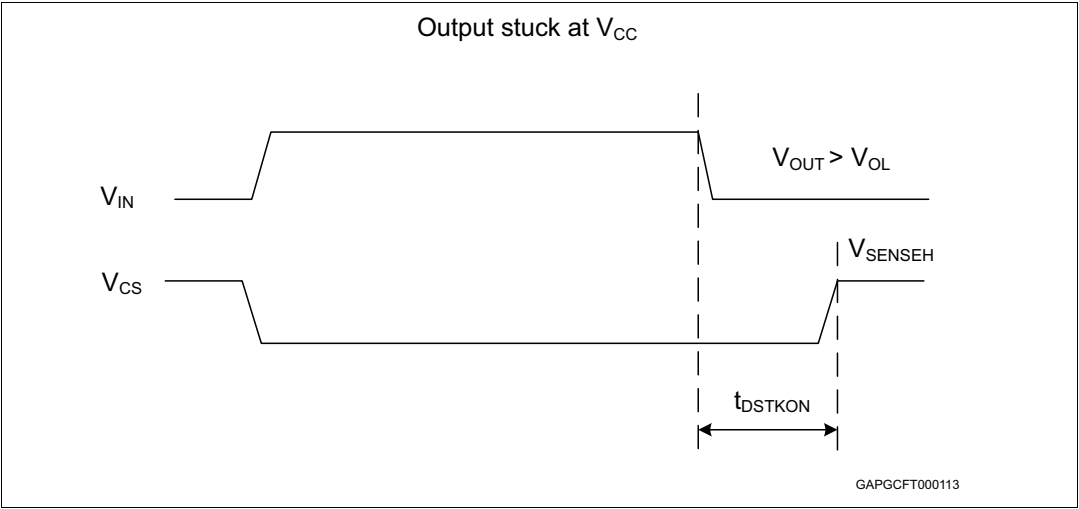


Figure 9. Switching characteristics

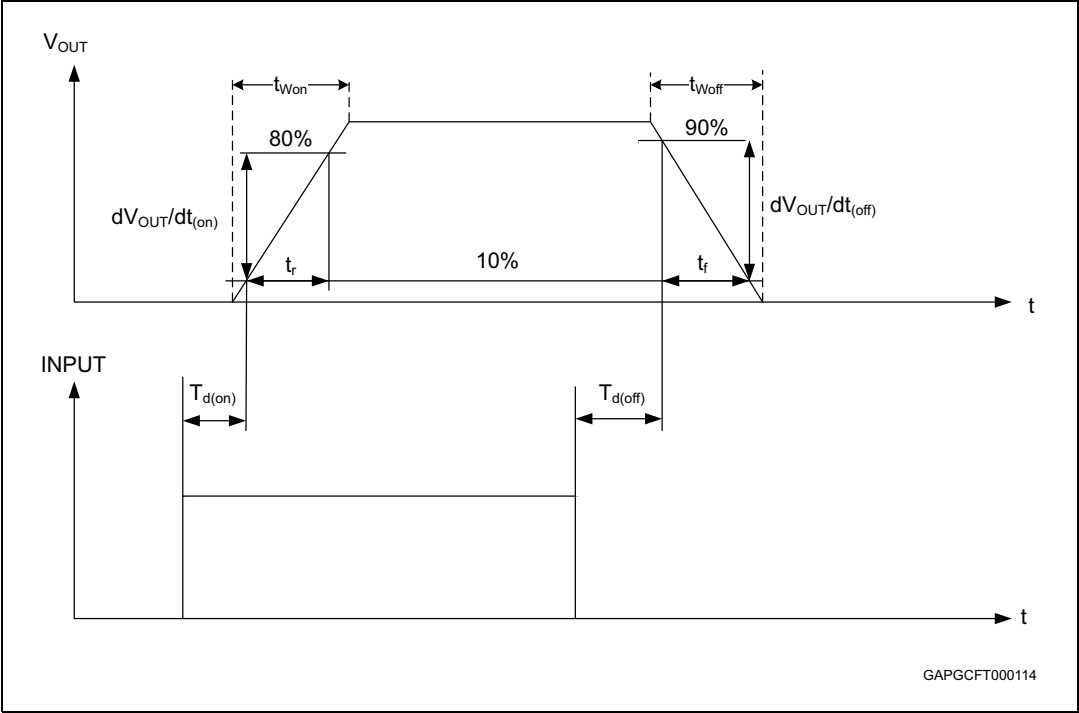


Figure 10. Output stuck to V_{CC} detection delay time at FR_{STBY} activation

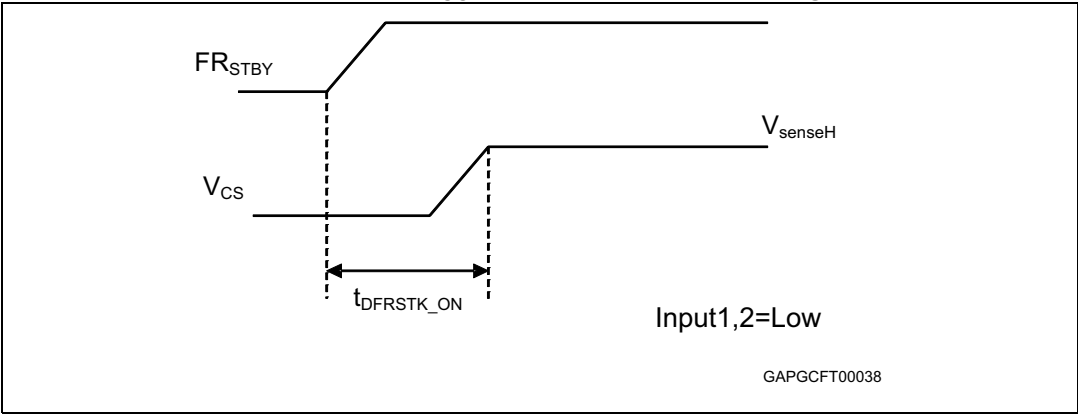


Figure 11. Delay response time between rising edge of output current and rising edge of current sense

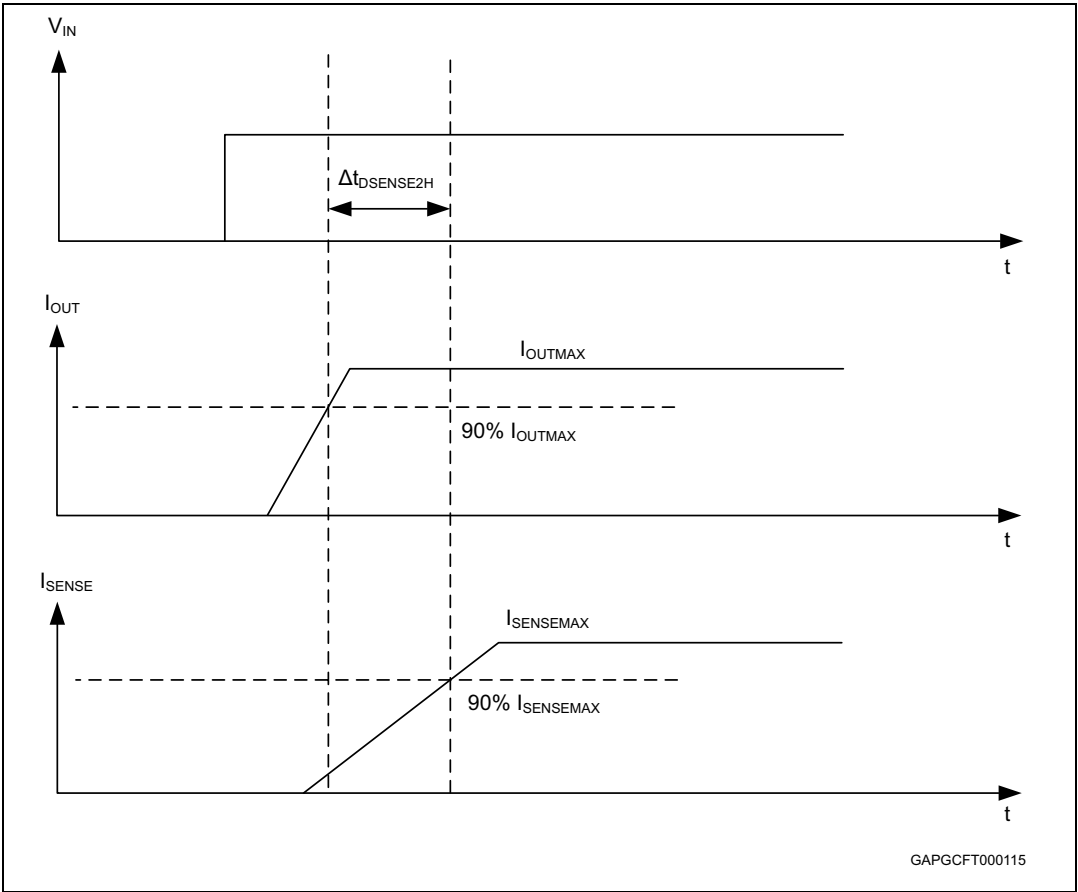


Figure 12. Output voltage drop limitation

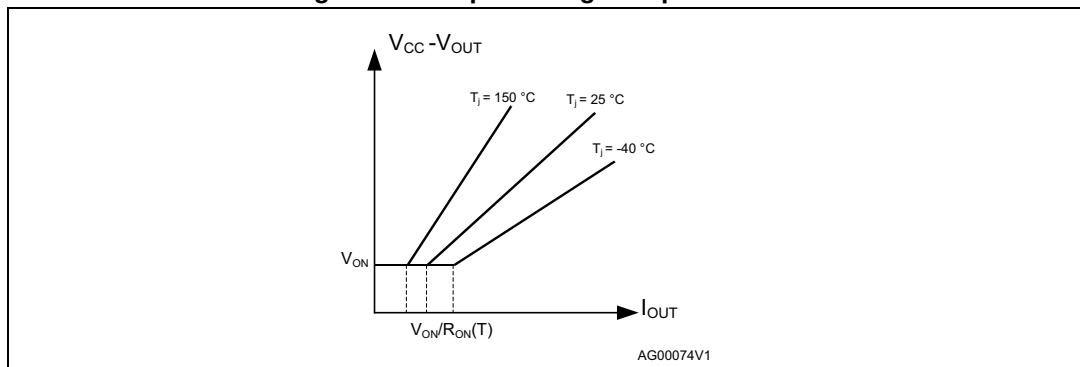
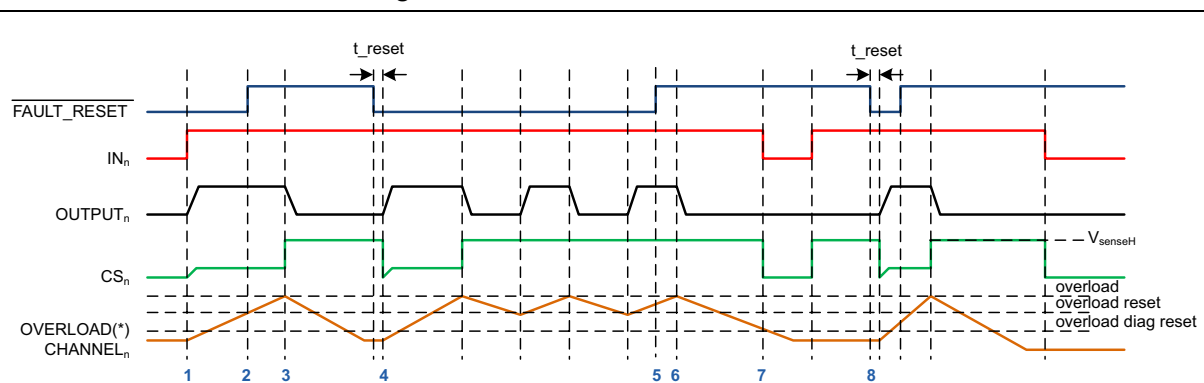


Figure 13. Device behavior in overload condition



- 1: $OUTPUT_n$ and CS_n controlled by IN_n
- 2: $FAULT_RESET$ from '0' to '1' → no action on CS_n pin
- 3: overload latch-off. IN_n high → CS_n high
- 4: $FAULT_RESET$ low AND Temp channeln < overload_reset → overload latch reset after t_{reset}
- 4 to 5: $FAULT_RESET$ low AND IN_n high → thermal cycling, CS_n high
- 5: $FAULT_RESET$ high → latch-off reset disabled
- 6 to 7: overload event and $FAULT_RESET$ high → latch-off, no thermal cycling
- 7 to 8: overload diagnostic disabled/enabled by the input
- 8: overload latch-off reset by $FAULT_RESET$

(*) OVERLOAD = thermal shutdown OR power limitation

GAPGCF000116

Table 11. Truth table

Conditions	Fault reset standby	Input	Output	Sense
Standby	L	L	L	0
Normal operation	X	L	L	0
	X	H	H	Nominal
Overload	X	L	L	0
	X	H	H	> Nominal
Overtemperature / short to ground	X	L	L	0
	L	H	Cycling	V_{SENSEH}
	H	H	Latched	V_{SENSEH}
Undervoltage	X	X	L	0
Short to V_{BAT}	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	< Nominal
Open-load off-state (with pull-up)	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	0
Negative output voltage clamp	X	L	Negative	0

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	- 450 V	- 600 V	5000 pulses	0.5 s	5 s	1 ms, 50 Ω
2a	+ 37 V	+ 50 V	5000 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	- 150 V	- 200 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	+ 150 V	+ 200 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4	- 12 V	- 16 V	1 pulse			100 ms, 0.01 Ω
5b ⁽²⁾	+ 123 V	+ 174 V	1 pulse			350 ms, 1 Ω

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b ⁽¹⁾	E	E
3b ⁽²⁾	C	C
4	C	C
5b ⁽³⁾	C	C

1. Without capacitor between V_{CC} and GND.

2. With 10 nF between V_{CC} and GND.

3. External load dump clamp, 58 V maximum, referred to ground.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the

2.4 Electrical characteristics curves

Figure 14. Off-state output current

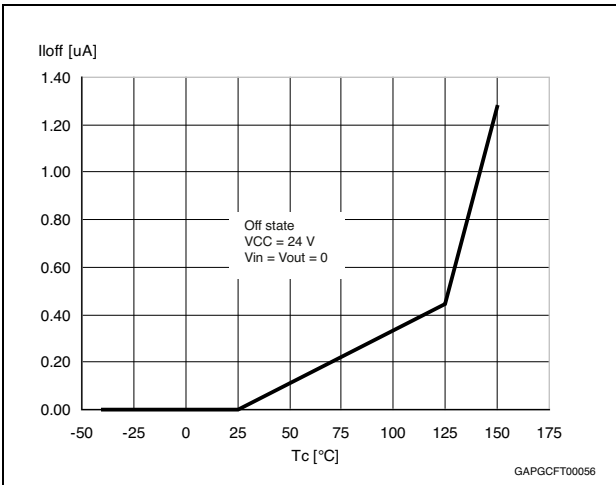


Figure 15. High level input current

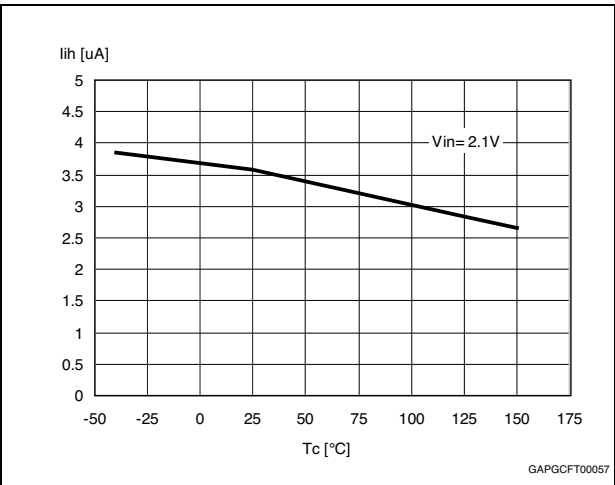


Figure 16. Input clamp voltage

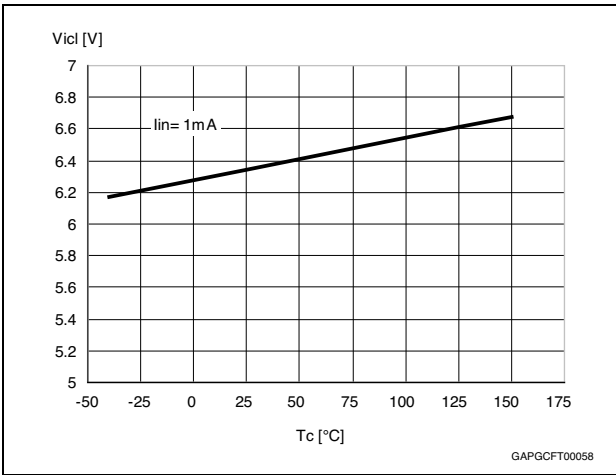


Figure 17. Input high level voltage

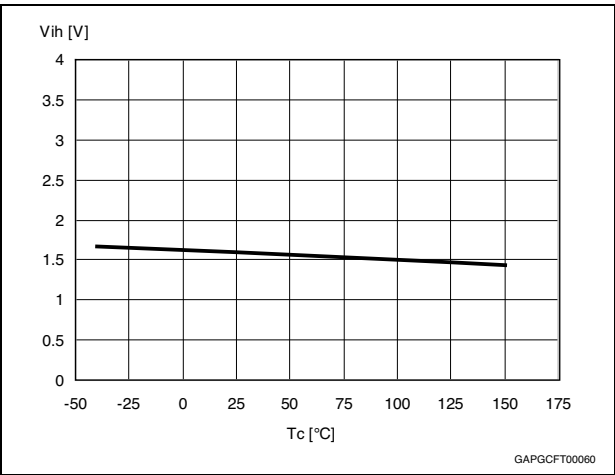


Figure 18. Input low level voltage

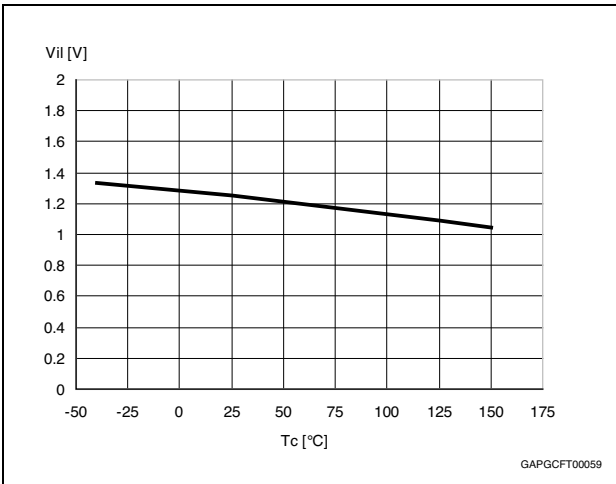


Figure 19. Input hysteresis voltage

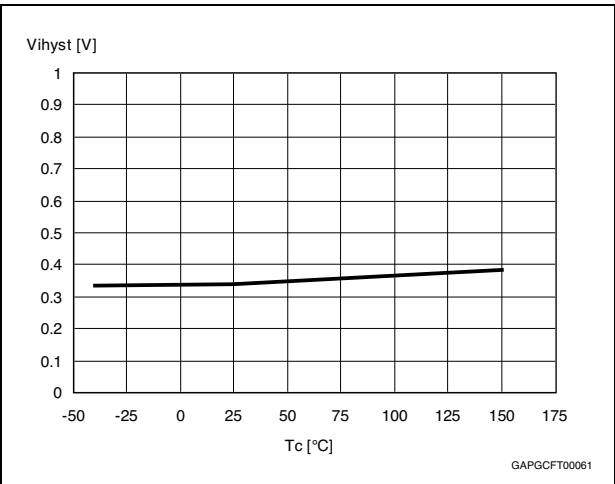


Figure 20. On-state resistance vs T_{case}

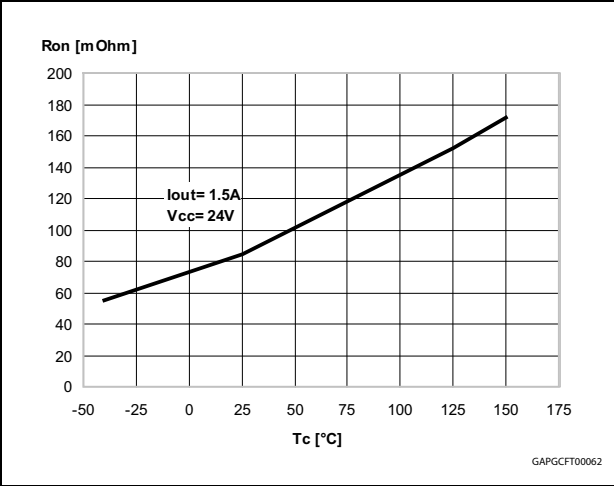


Figure 21. On-state resistance vs V_{CC}

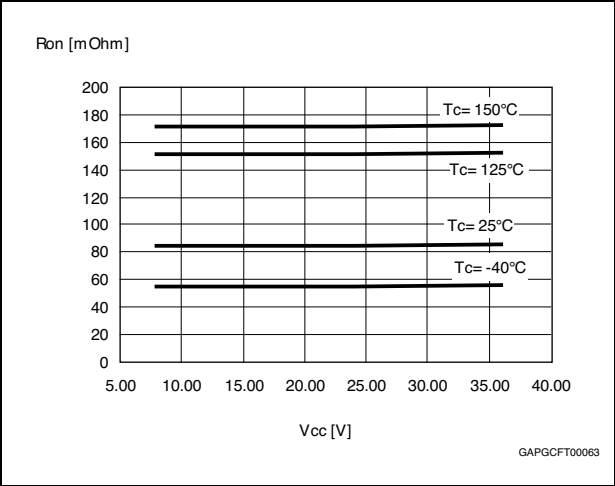


Figure 22. I_{limH} vs T_{case}

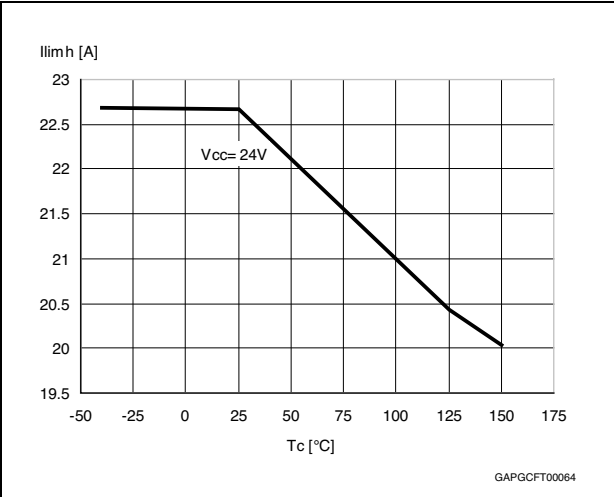


Figure 23. Turn-on voltage slope

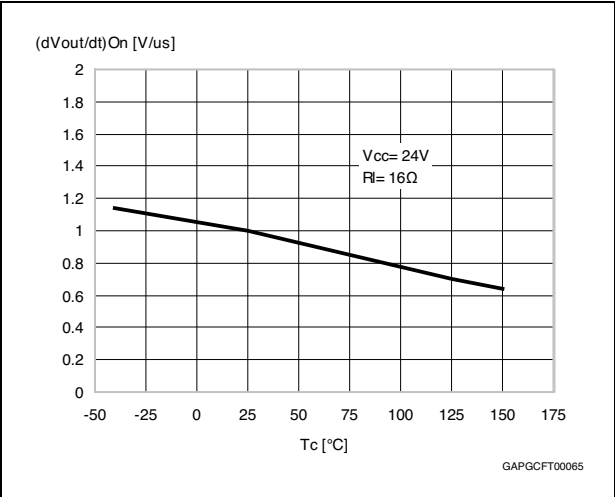
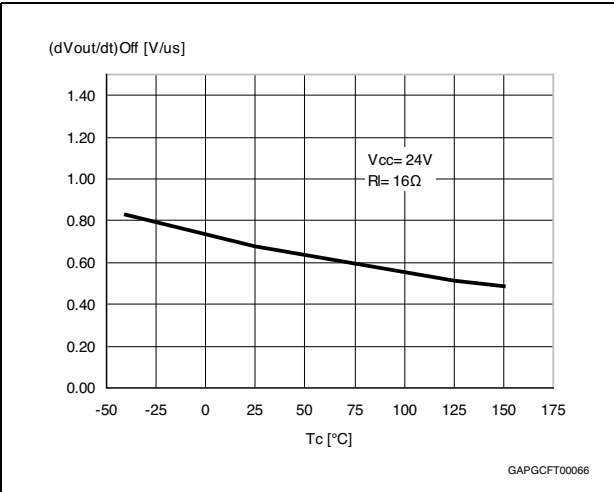
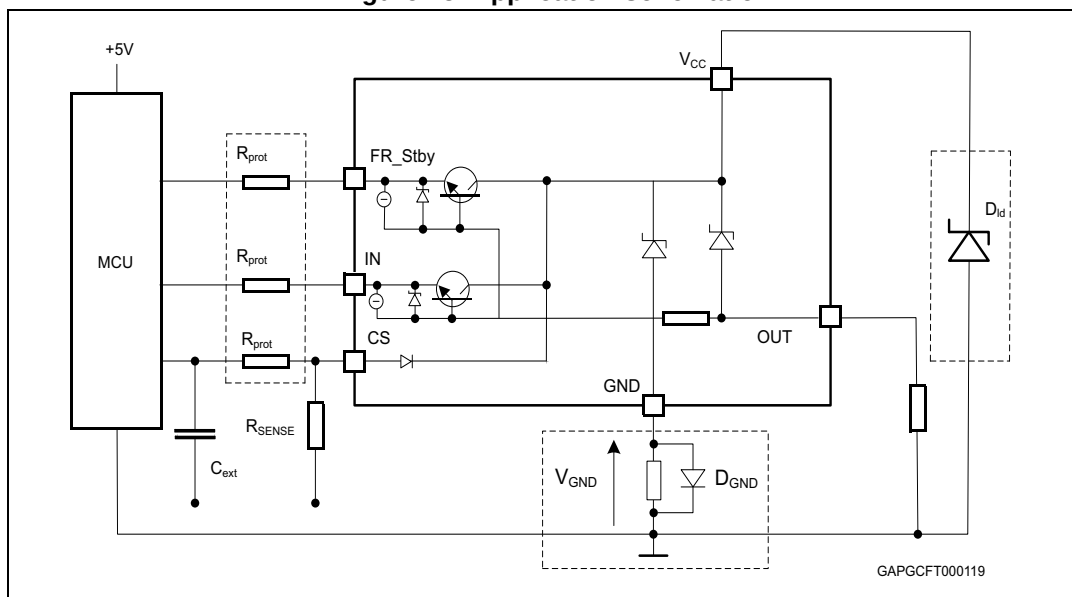


Figure 24. Turn-off voltage slope



3 Application information

Figure 25. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This solution can be used with any type of load.

The following is an indication on how to select the R_{GND} resistor.

1. $R_{GND} \leq 600 \text{ mV} / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{\text{GND}}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests Solution 2 is used (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 4.7 \text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600 \text{ mV}$) in the input threshold and in the status output values, if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds to V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/2 table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins are pulled negative. ST suggests that a resistor (R_{prot}) be inserted in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

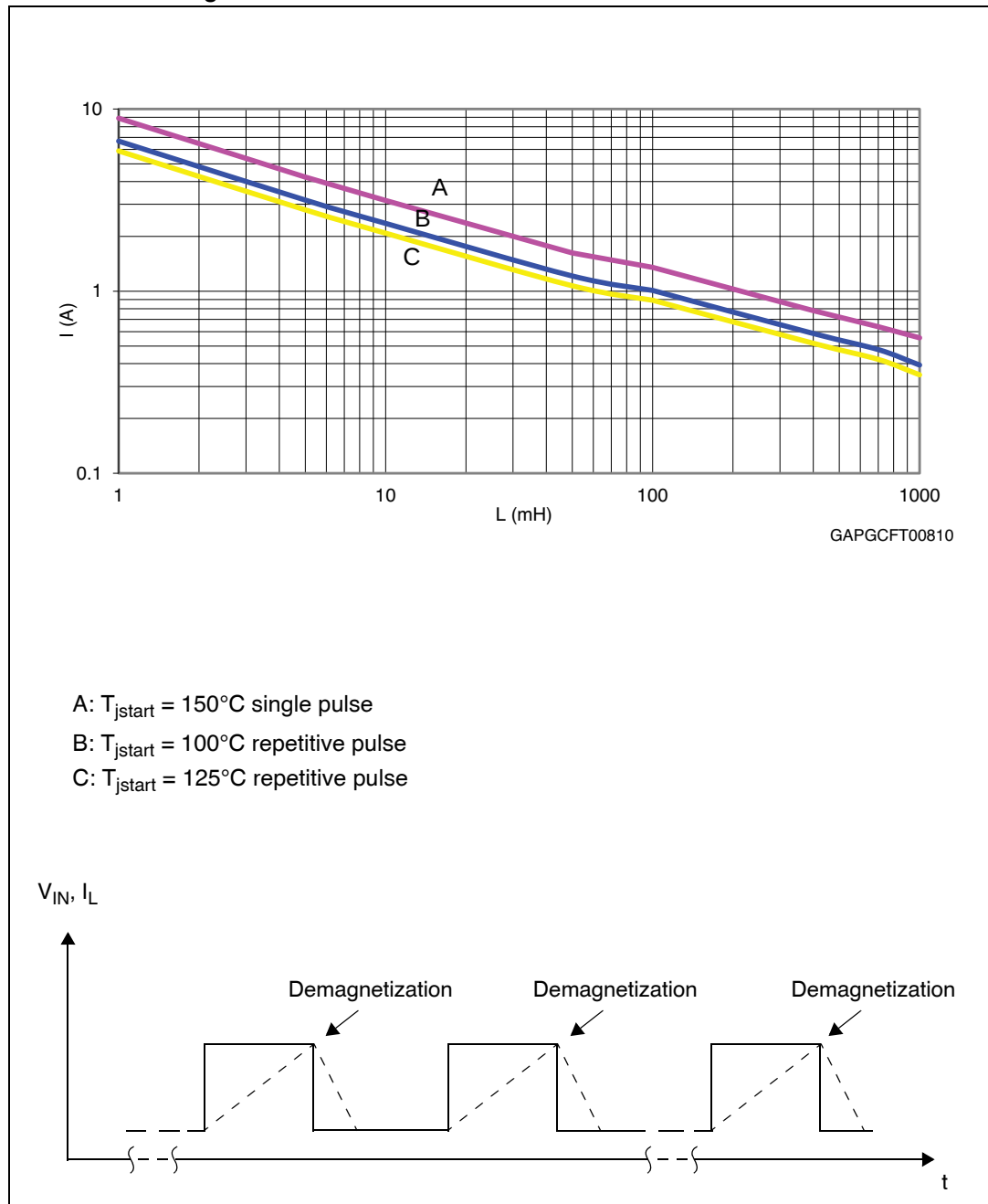
For $V_{CCpeak} = -600 \text{ V}$ and $I_{latchup} \geq 20 \text{ mA}$; $V_{OH\mu C} \geq 4.5 \text{ V}$

$$30 \text{ k}\Omega \leq R_{prot} \leq 180 \text{ k}\Omega.$$

Recommended R_{prot} value is $60 \text{ k}\Omega$.

3.4 Maximum demagnetization energy ($V_{CC} = 24\text{ V}$)

Figure 26. Maximum turn-off current versus inductance

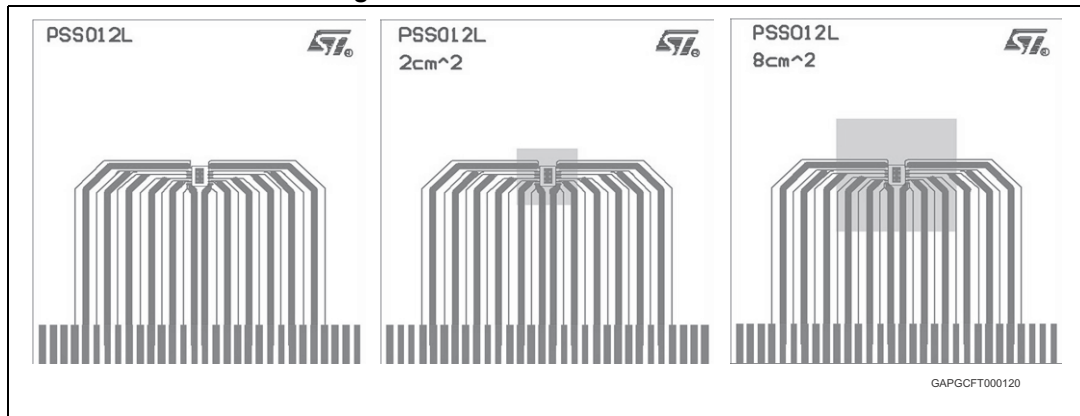


1. Values are generated with $R_L = 0\ \Omega$.
 In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-12 thermal data

Figure 27. PowerSSO-12 PC board



1. Layout condition of R_{th} and Z_{th} measurements (Board finish thickness 1.6 mm $\pm$ 10 %; Board double layer; Board dimension 77 mm x 86 mm; Board Material FR4; Cu thickness 0.070 mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm $\pm$ 0.08 mm; Cu thickness on vias 0.025 mm; Footprint dimension 4.1 mm x 6.5 mm)

Figure 28. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

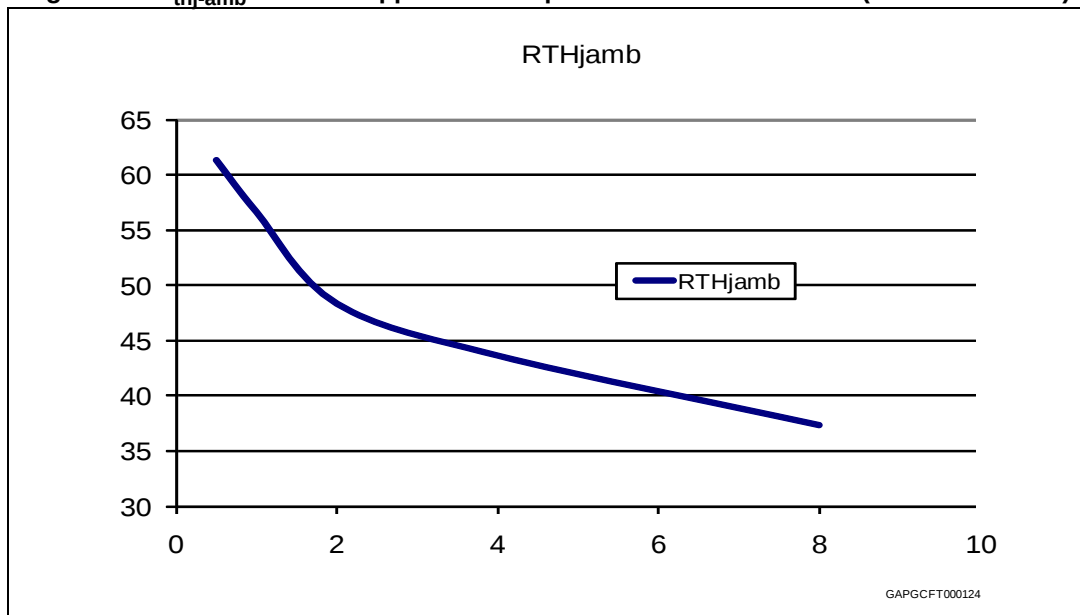


Figure 29. PowerSSO-12 thermal impedance junction ambient single pulse (one channel ON)

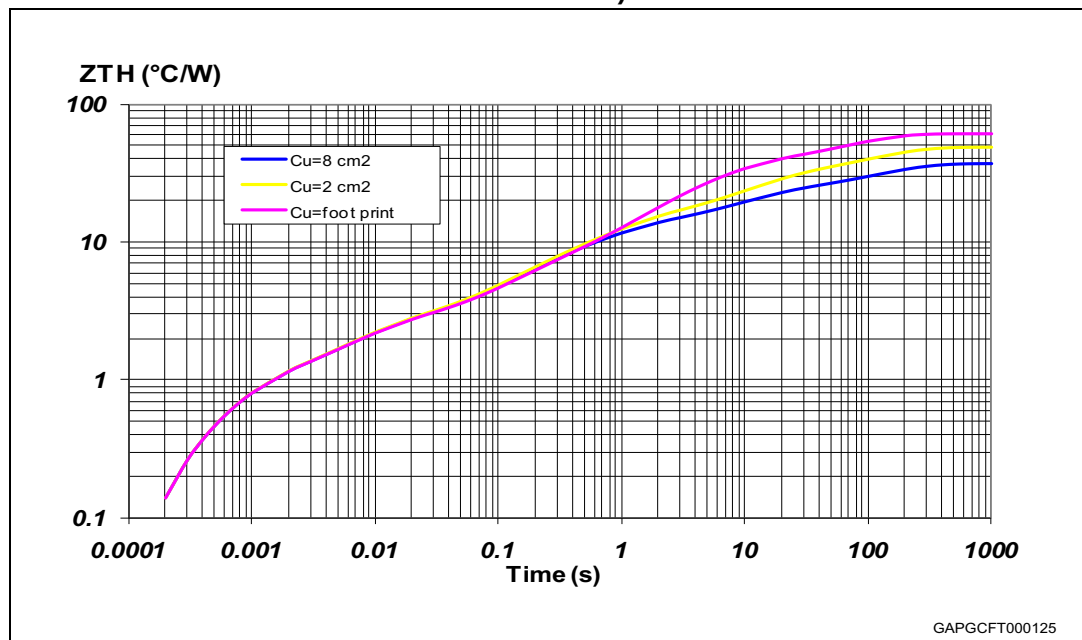
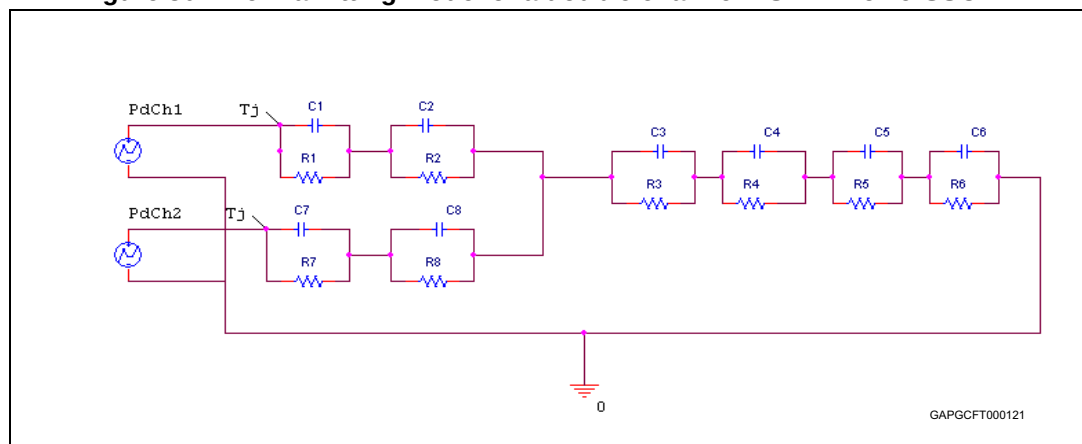


Figure 30. Thermal fitting model of a double channel HSD in PowerSSO-12



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

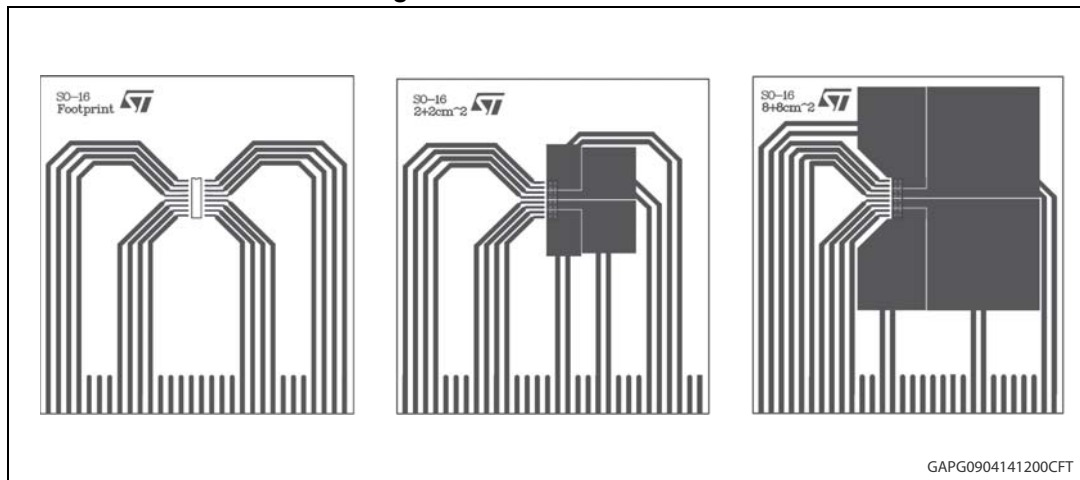
$$\text{where } \delta = t_p / T$$

Table 15. Thermal parameters

Area/island (cm ²)	Footprint	2	8
R1 = R7 (°C/W)	0.8		
R2 = R8 (°C/W)	1.5		
R3 (°C/W)	3		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 = C7 (W.s/°C)	0.0008		
C2 = C8 (W.s/°C)	0.005		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

4.2 SO-16N thermal data

Figure 31. SO-16N PC board



1. Layout condition of R_{th} and Z_{th} measurements (Board finish thickness 1.6 mm $\pm$ 10%; Board double layer; Board dimension 129 x 60; Board Material FR4; Cu thickness 0.070mm (front and back side), Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm $\pm$ 0.08 mm; Cu thickness on vias 0.025 mm).

Figure 32. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

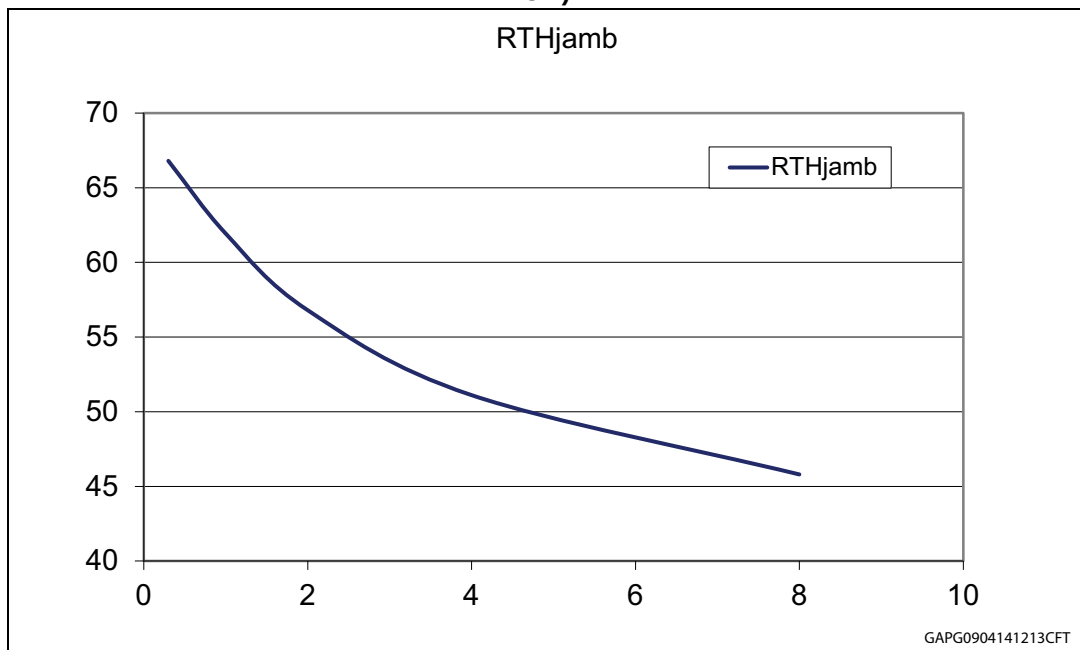


Figure 33. SO-16N thermal impedance junction ambient single pulse (one channel on)

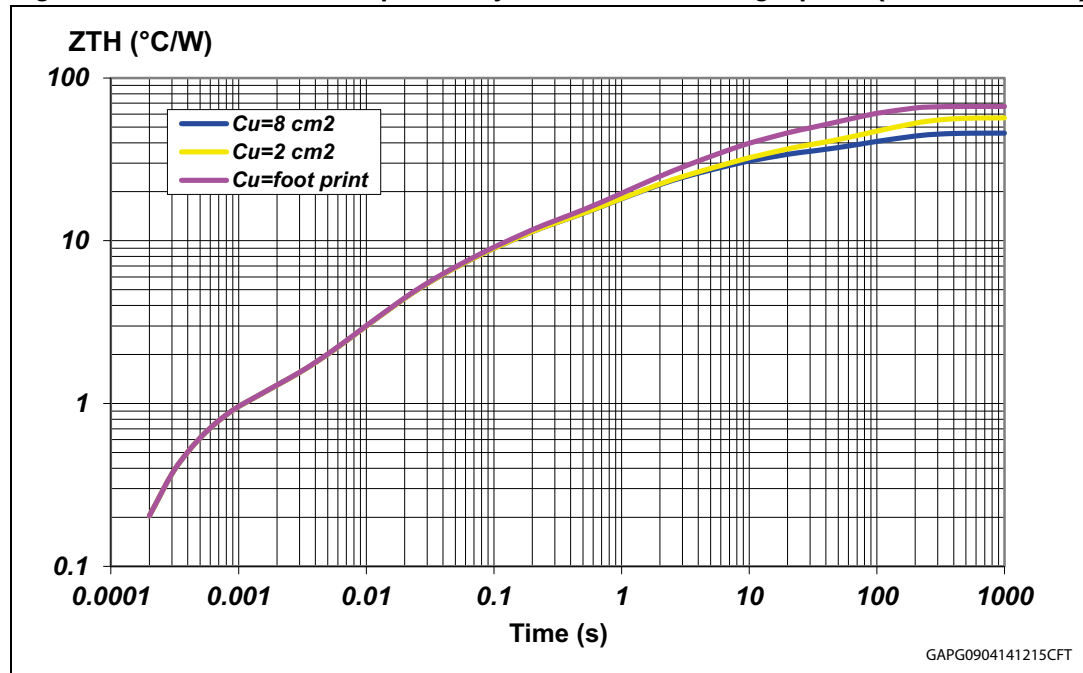
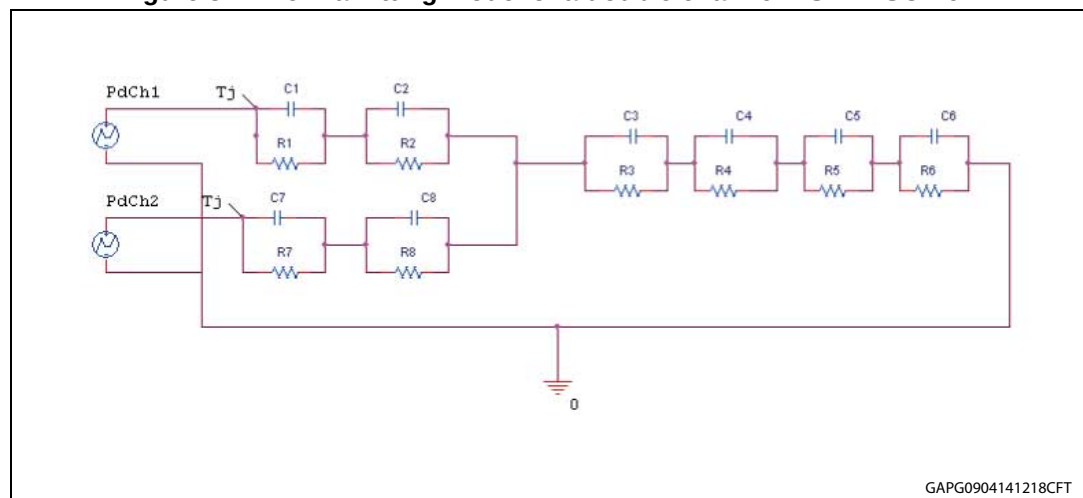


Figure 34. Thermal fitting model of a double channel HSD in SO-16N

**Equation 2: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

Table 16. Thermal parameters

Area/island (cm ²)	Footprint	2	8
R1 = R7 (°C/W)	0.8		
R2 = R8 (°C/W)	3		
R3 (°C/W)	6		
R4 (°C/W)	10		
R5 (°C/W)	20	14	12
R6 (°C/W)	27	23	14
C1 = C7 (W.s/°C)	0.0005		
C2 = C8 (W.s/°C)	0.005		
C3 (W.s/°C)	0.015		
C4 (W.s/°C)	0.1		
C5 (W.s/°C)	0.3	0.5	0.5
C6 (W.s/°C)	2.5	5	7

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 PowerSSO-12 mechanical data

Figure 35. PowerSSO-12 package dimensions

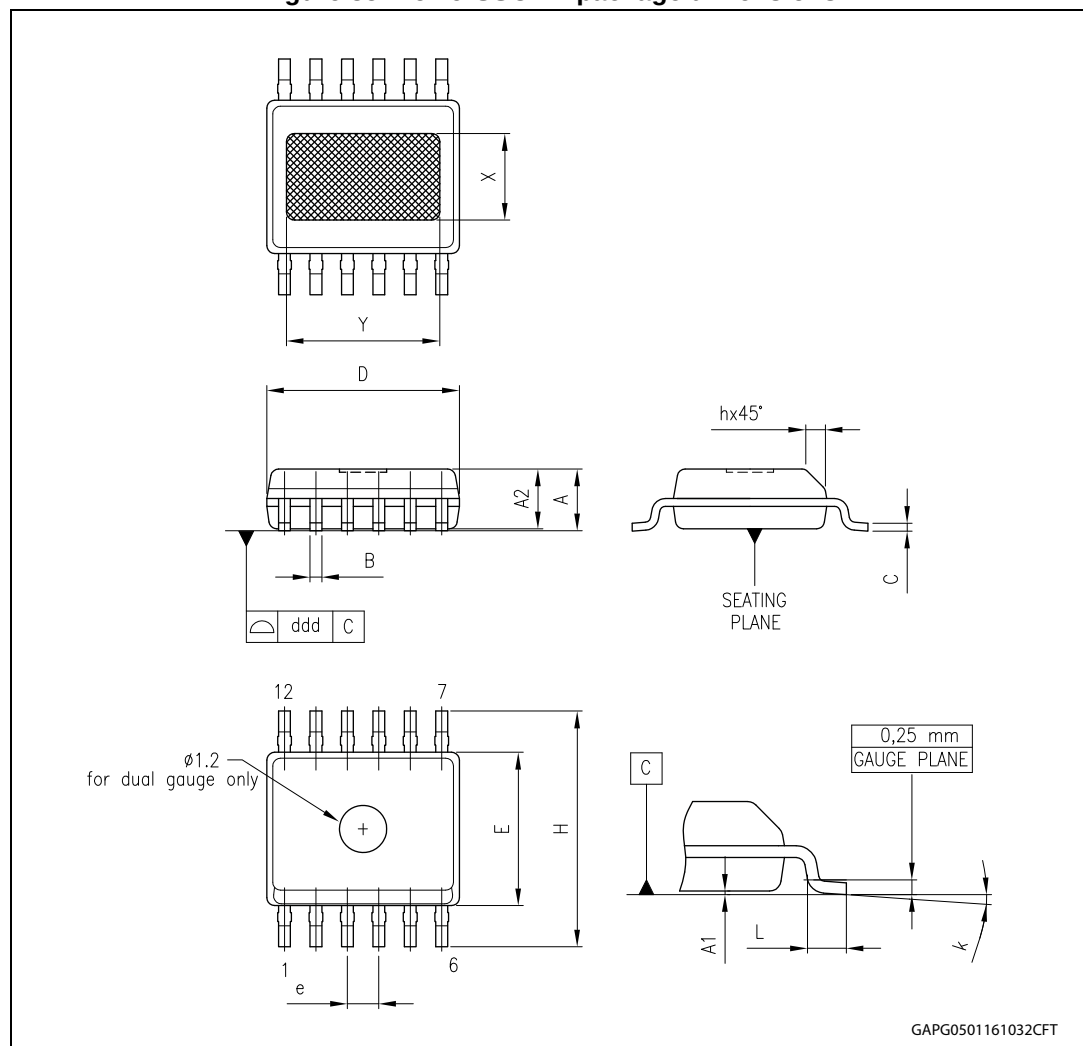


Table 17. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.700
A1	0.000		0.100
A2	1.100		1.600
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.550
L	0.400		1.270
k	0°		8°
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

5.3 SO-16N package information

Figure 36. SO-16N package dimensions

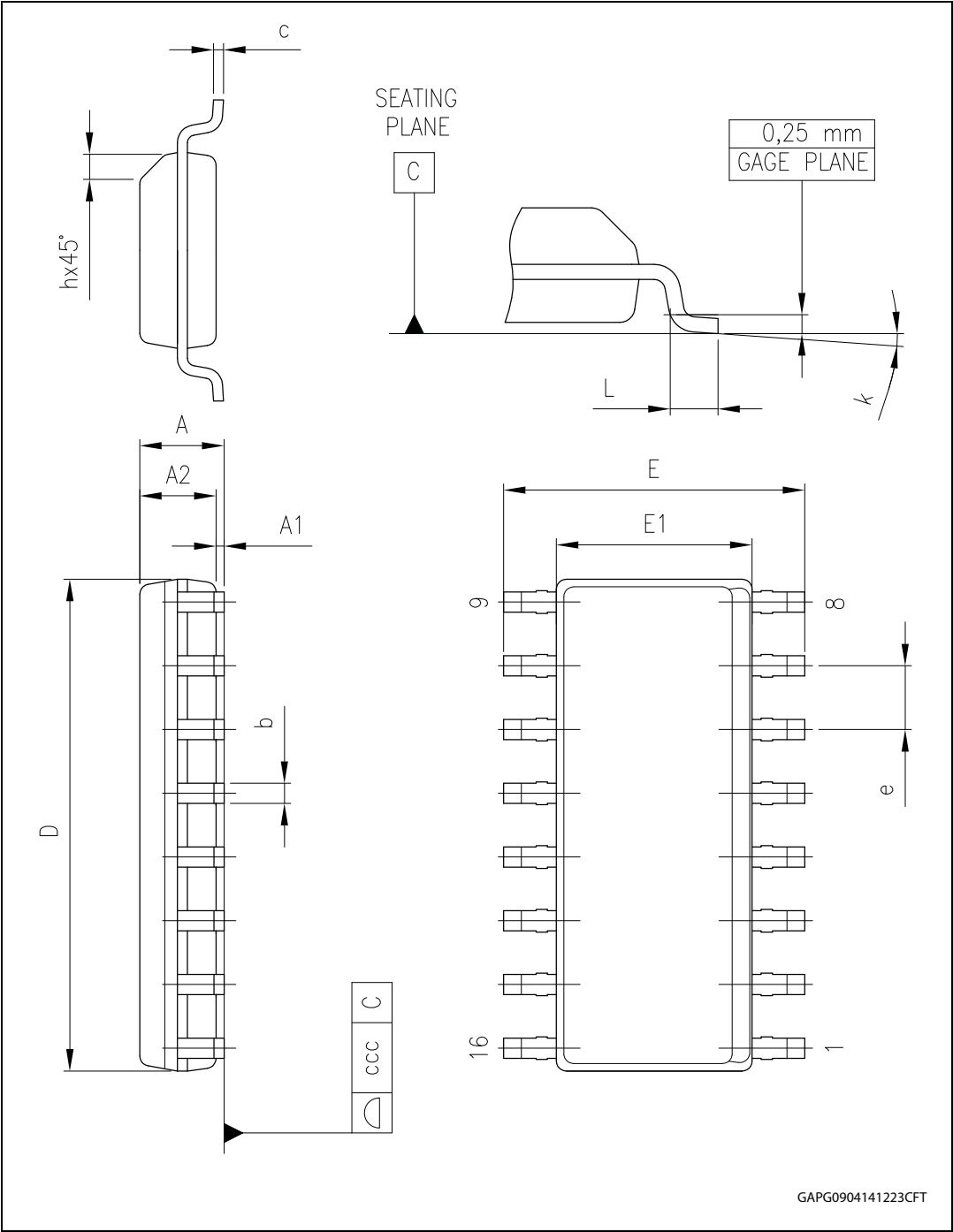


Table 18. SO-16N mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
k	0°		8°
ccc			0.10

6 Packing information

6.1 PowerSSO-12 packing information

Figure 37. PowerSSO-12 tube shipment (no suffix)

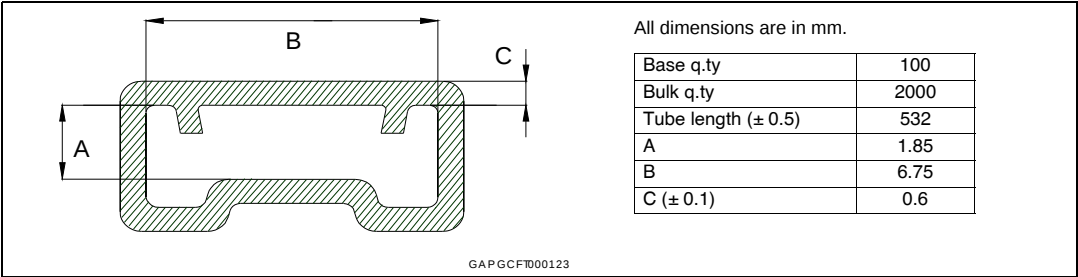
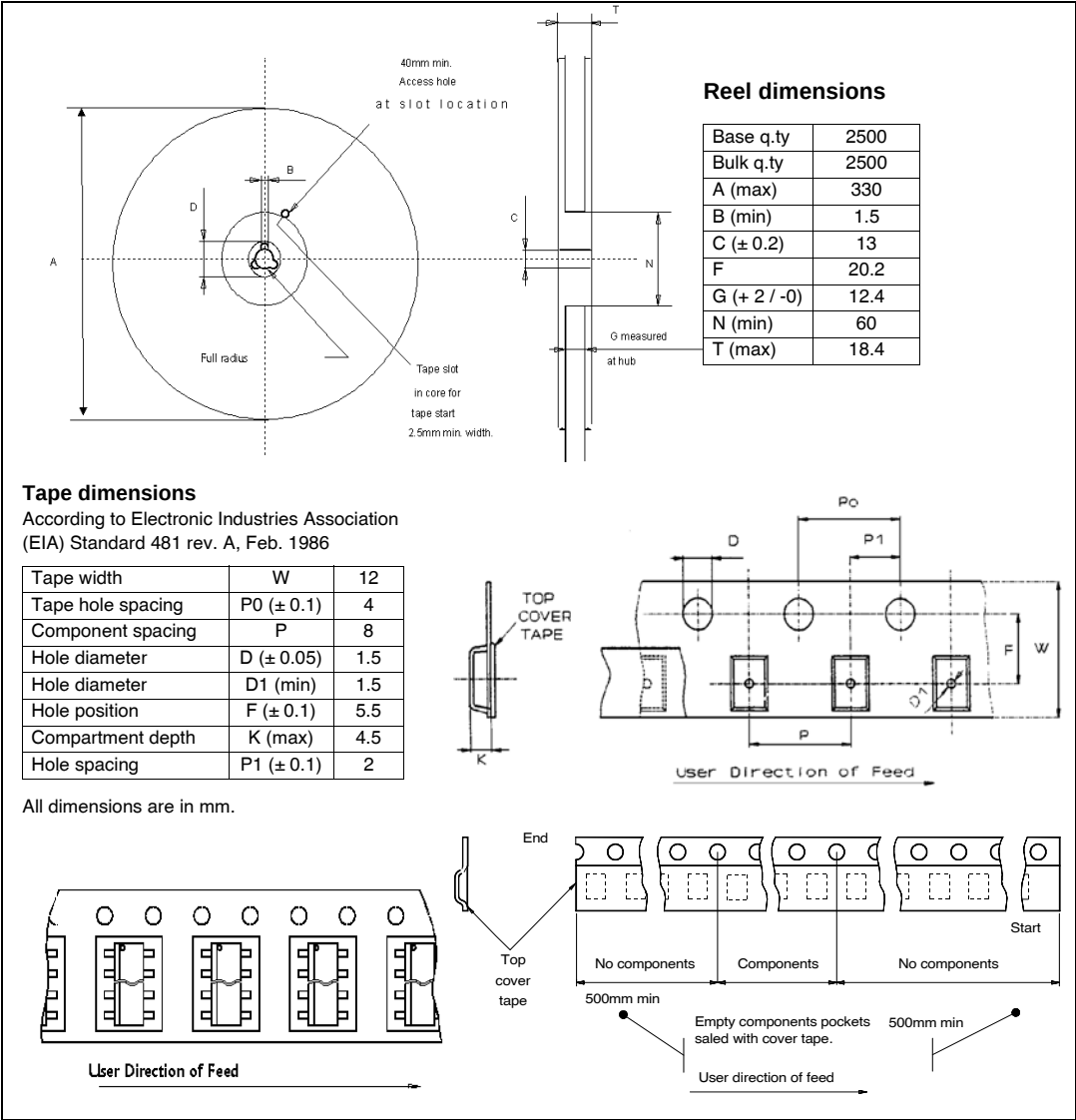


Figure 38. PowerSSO-12 tape and reel shipment (suffix “TR”)



6.2 SO-16N packing information

Figure 39. SO-16N tube shipment (no suffix)

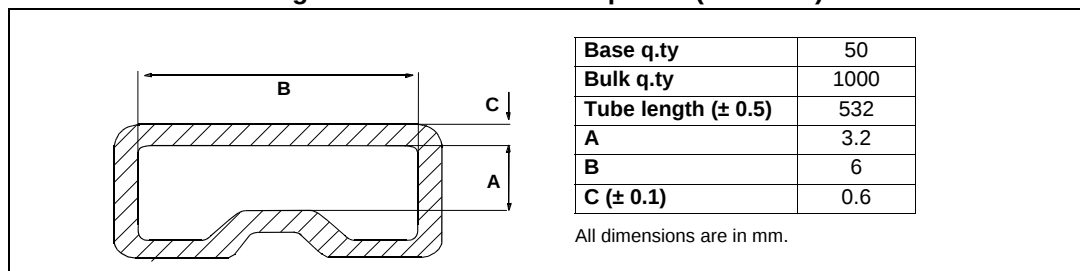
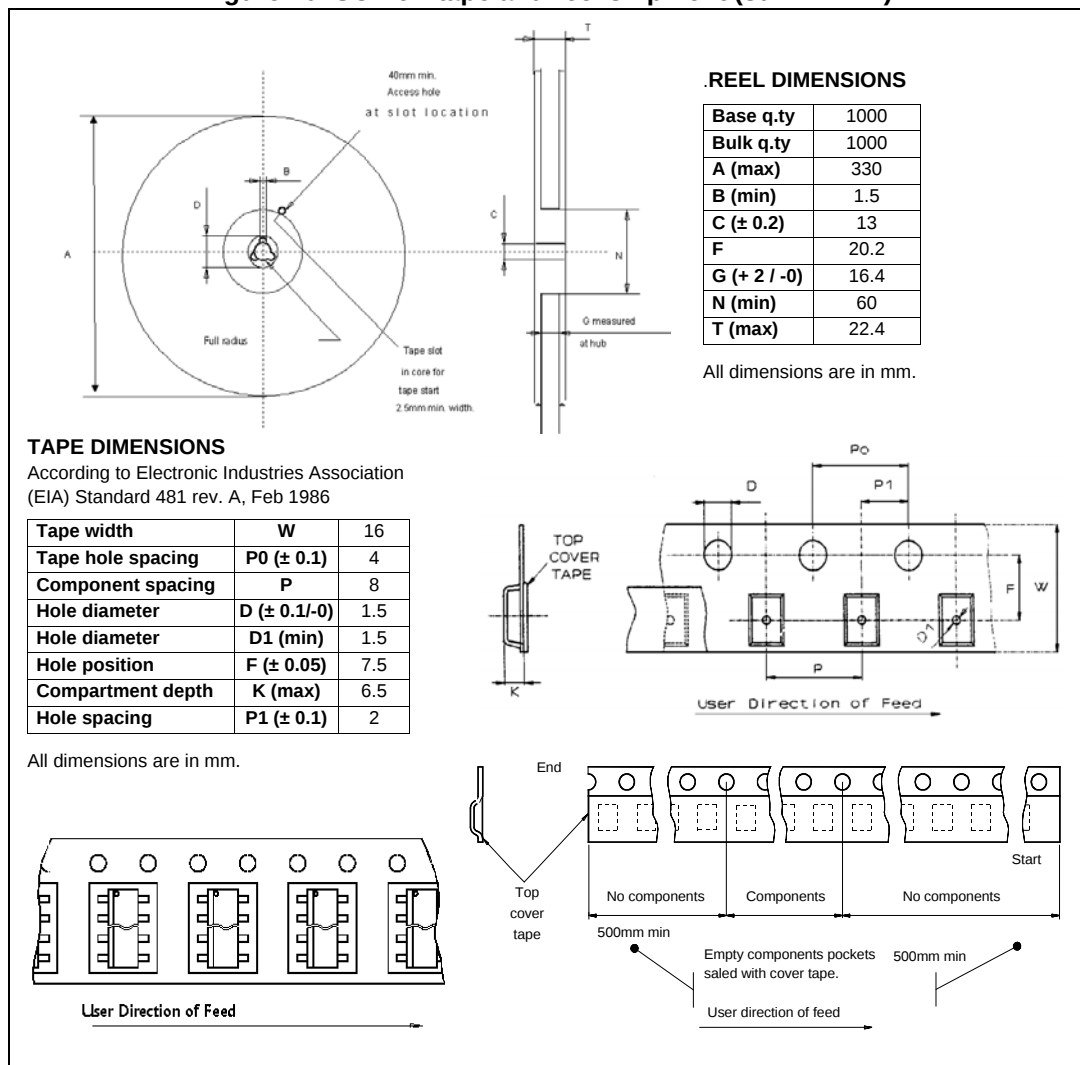


Figure 40. SO-16N tape and reel shipment (suffix "TR")



7 Order code

Table 19. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-12	VND5T100LAJ-E	VND5T100LAJTR-E
SO-16N	VND5T100LAS-E	VND5T100LASTR-E

8 Revision history

Table 20. Document revision history

Date	Revision	Changes
25-Jun-2012	1	Initial release.
18-Sep-2013	2	Updated disclaimer.
30-Apr-2014	3	Added SO-16N package and related details.
08-Feb-2016	4	<i>Table 4: Thermal data:</i> – $R_{thj-case}$: updated values – $R_{thj-pin}$: added row Updated Section 5.2: PowerSSO-12 mechanical data and Section 5.3: SO-16N package information
23-Aug-2016	5	Added indication of AEC-Q100 qualification in Features . Updated Figure 3: Configuration diagram SO-16N (top view) .

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