Single 2-Input AND Gate

The MC74HC1G08 is a high speed CMOS 2-input AND gate fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output.

The MC74HC1G08 output drive current is 1/2 compared to MC74HC series.

Features

- High Speed: $t_{PD} = 7 \text{ ns (Typ)}$ at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu A$ (Max) at $T_A = 25^{\circ}C$
- High Noise Immunity
- Balanced Propagation Delays (t_{pLH} = t_{pHL})
- Symmetrical Output Impedance (I_{OH} = I_{OL} = 2 mA)
- Chip Complexity: < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

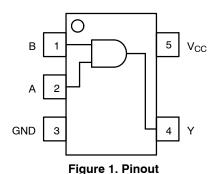


Figure 2. Logic Symbol

PIN ASSIGNMENT				
1	В			
2	А			
3	GND			
4	Y			
5	V _{CC}			



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SC-88A DF SUFFIX CASE 419A



MARKING



TSOP-5 DT SUFFIX CASE 483



XX = Device Code
M = Date Code*
= Pb-Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary
depending upon manufacturing location.



SC-74A DBV SUFFIX CASE 318BQ



XXX = Specific Device Code

M = Date Code ■ Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inp	uts	Output
Α	В	Y
L	L	L
L	Н	L
Н	L	L
Н	Н	Н
н	Н	Н

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data

MAXIMUM RATINGS

Symbol	Paramete	er	Value	Unit
V _{CC}	DC Supply Voltage	SC-88A (NLV), TSOP-5 SC-88A, SC-74A	-0.5 to +7.0 -0.5 to +6.5	V
V _{IN}	DC Input Voltage		-0.5 to V_{CC} $+0.5$	V
V _{OUT}	DC Output Voltage		-0.5 to $V_{CC} + 0.5$	V
I _{IK}	DC Input Diode Current		±20	mA
I _{OK}	DC Output Diode Current		±20	mA
l _{out}	DC Output Source/Sink Current		± 12.5	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground	d Pin	±25	mA
T _{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 S	Seconds	260	°C
TJ	Junction Temperature Under Bias		+ 150	°C
θ _{JA}	Thermal Resistance (Note 1)	SC70-5/SC-88A/SOT-353 SOT23-5/TSOP-5/SC59-5 SC-74A	659 555 555	°C/W
P _D	Power Dissipation in Still Air at 85°C	SC70-5/SC-88A/SOT-353 SOT23-5/TSOP-5/SC59-5 SC-74A	190 225 225	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 1000	V
I _{LATCHUP}	Latchup Performance (Note 3)	SC-88A (NLV), SOT-23 SC-88A, SC-74A	±500 ±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 20 ounce copper trace with no air flow.

2. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to JESD22-C101-F. JEDEC recommends that ESD qualification to

EIA/JESD22-A115A (Machine Model) be discontinued per JEDEC/JEP172A.

3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	6.0	V
V _{IN}	DC Input Voltage	0.0	V _{CC}	٧
V _{OUT}	DC Output Voltage	0.0	V_{CC}	V
T _A	Operating Temperature Range	– 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time $SC-88A \ (NLV), TSOP \ V_{CC}=2.0 \ V_{CC}=3.0 \ V_{CC}=4.5 \ V_{CC}=6.0$	V 0 V 0 V 0	1000 600 500 400	ns/V
	Input Rise and Fall Time $SC-88A, SC-74 \\ V_{CC}=1.65 \ V \ to \ 1.95 \\ V_{CC}=2.3 \ V \ to \ 2.7 \\ V_{CC}=3.0 \ V \ to \ 3.6 \\ V_{CC}=4.5 \ V \ to \ 6.0 \\ \label{eq:CC}$	V 0 V 0 V 0	20 20 10 5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

			V _{CC}	Т	A = 25°	С	-40°C ≤ 1	Γ _A ≤ 85°C	-55°C ≤ T	A ≤ 125°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	High-Level Input Voltage		2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.20	- - - -	- - -	1.5 2.1 3.15 4.20	- - - -	1.5 2.1 3.15 4.20	- - - -	V
V _{IL}	Low-Level Input Voltage		2.0 3.0 4.5 6.0	- - -	- - -	0.5 0.9 1.35 1.80	- - -	0.5 0.9 1.35 1.80	- - -	0.5 0.9 1.35 1.80	V
V _{OH}	High-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -20 \mu A$	2.0 3.0 4.5 6.0	1.9 2.9 4.4 5.9	2.0 3.0 4.5 6.0		1.9 2.9 4.4 5.9	- - -	1.9 2.9 4.4 5.9	- - - -	٧
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -2 \text{ mA}$ $I_{OH} = -2.6 \text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	1 1	4.13 5.63	- -	4.08 5.58	- -	
V _{OL}	Low-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 20 \mu A$	2.0 3.0 4.5 6.0	1 1 1 1	0.0 0.0 0.0 0.0	0.1 0.1 0.1 0.1	1 1 1 1	0.1 0.1 0.1 0.1		0.1 0.1 0.1 0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 2 \text{ mA}$ $I_{OL} = 2.6 \text{ mA}$	4.5 6.0		0.17 0.18	0.26 0.26	1 1	0.33 0.33	-	0.40 0.40	
I _{IN}	Input Leakage Current	V _{IN} = 6.0 V or GND	6.0	_	_	± 0.1	-	±1.0	-	±1.0	μΑ
Icc	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	6.0	-	-	1.0	-	10	-	40	μΑ

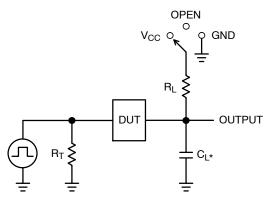
^{*}Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6.0 \text{ ns}$)

			Т	A = 25°	С	-40°C ≤ 1	Γ _A ≤ 85°C	-55°C ≤ T	A ≤ 125°C	
Symbol	Parameter	Test Conditions	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} ,	Propagation Delay,	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$	_	3.5	15	-	20	-	25	ns
tPHL	Input A or B to Y	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	- - -	20 11 8 7	100 27 20 17	- - -	125 35 25 21	- - -	155 90 35 26	
t _{TLH} , t _{THL}	Output Transition Time	$\begin{split} &V_{CC} = 5.0 \text{ V} & C_L = 15 \text{ pF} \\ &V_{CC} = 2.0 \text{ V} & C_L = 50 \text{ pF} \\ &V_{CC} = 3.0 \text{ V} & V_{CC} = 4.5 \text{ V} \\ &V_{CC} = 6.0 \text{ V} \end{split}$		3 25 16 11 9	10 125 35 25 21	- - - -	15 155 45 31 26	- - - -	20 200 60 38 32	ns
C _{IN}	Input Capacitance		_	5	10	-	10	-	10	pF

		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 4)	10	рF

^{4.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.



Test	Switch Position	C _L , pF	R _L , Ω
t _{PLH} / t _{PHL}	Open		Х
t _{TLH} / t _{THL} (Note 5)	Open	See AC Characteristics Table	Х
t _{PLZ} / t _{PZL}	V _{CC}	lable	1 k
t _{PHZ} / t _{PZH}	GND		1 k

X - Don't Care

* C_L includes probe and jig capacitance R_T is Z_{OUT} of pulse generator (typically 50 W) f = 1 MHz

Figure 3. Test Circuit

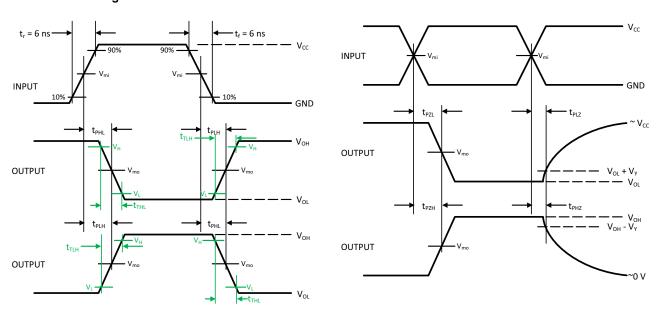


Figure 4. Switching Waveforms

		V _{mo} , V				
V _{CC} , V	V_{mi} , V	t _{PLH} , t _{PHL}	$t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}$	V_L,V	V _H , V	V _Y , V
3.0 to 3.6	V _{CC} /2	(V _{OH} – V _{OL})/2	V _{CC} /2	V _{OL} + 0.1 (V _{OH} – V _{OL})	V _{OL} + 0.9 (V _{OH} – V _{OL})	0.3
4.5 to 5.5	V _{CC} /2	(V _{OH} – V _{OL})/2	V _{CC} /2	V _{OL} + 0.1 (V _{OH} – V _{OL})	V _{OL} + 0.9 (V _{OH} – V _{OL})	0.3

^{5.} t_{TLH} and t_{THL} are measured from 10% to 90% of ($V_{OH} - V_{OL}$), and 90% to 10% of ($V_{OH} - V_{OL}$), respectively.

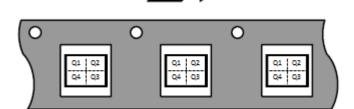
ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping [†]
MC74HC1G08DFT1G	SC-88A	H2	Q2	3000 / Tape & Reel
NLVHC1G08DFT1G*	SC-88A	H2	Q2	3000 / Tape & Reel
MC74HC1G08DFT2G	SC-88A	H2	Q4	3000 / Tape & Reel
NLVHC1G08DFT2G*	SC-88A	H2	Q4	3000 / Tape & Reel
MC74HC1G08DTT1G	TSOP-5	H2	Q4	3000 / Tape & Reel
NLVHC1G08DTT1G*	TSOP-5	H2R	Q4	3000 / Tape & Reel
MC74HC1G08DBVT1G (In Development)	SC-74A	TBD	Q4	3000 / Tape & Reel

[†]For complete information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pin 1 Orientation in Tape and Reel

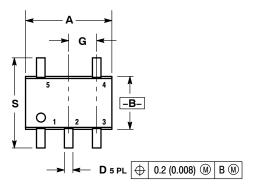
Direction of Feed

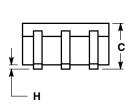


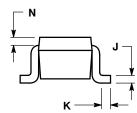
^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE L



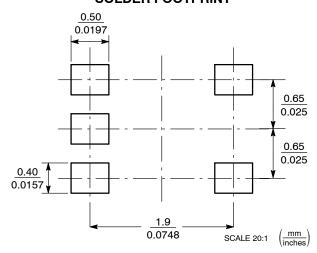




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

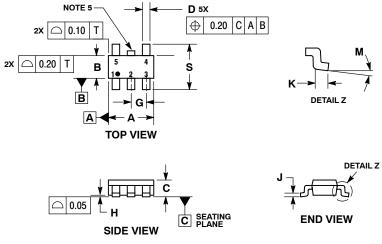
	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.071	0.087	1.80	2.20
В	0.045	0.053	1.15	1.35
С	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026	BSC	0.65	BSC
Н		0.004		0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20	REF
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



PACKAGE DIMENSIONS

TSOP-5 **CASE 483** ISSUE M



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: MILLIMETERS.

 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

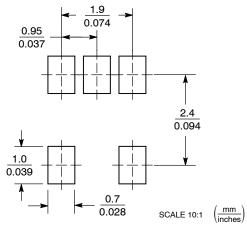
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.

 5. OPTIONAL CONSTRUCTION: AN ADDITIONAL
- EAGEED 0.19 PER SIDE. DIMENSION A.

 5. OPTIONAL CONSTRUCTION: AN ADDITIONAL
 TRIMMED LEAD IS ALLOWED IN THIS LOCATION.
 TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2
 FROM BODY.

	MILLIMETERS				
DIM	MIN	MAX			
Α	2.85	3.15			
В	1.35	1.65			
С	0.90	1.10			
D	0.25	0.50			
G	0.95	BSC			
Н	0.01	0.10			
J	0.10	0.26			
K	0.20	0.60			
М	0 °	10°			
s	2.50	3.00			

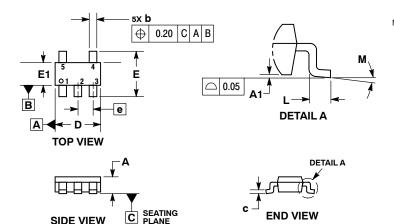
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

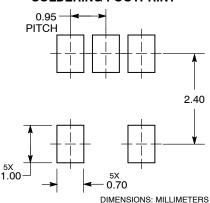
SC-74A CASE 318BQ **ISSUE B**



- DIMENSIONING AND TOLERANCING PER ASME
- CONTROLLING DIMENSION: MILLIMETERS.
 MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH
- THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
Α	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
С	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
е	0.95 BSC	
L	0.20	0.60
М	0 °	10°

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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