Low-Power 12.5-Gbps 8-Channel (Unidirectional) Repeater With Input Equalization

Check for Samples: DS125BR800A

FEATURES

- **Proven System Interoperability**
- **Comprehensive multi-protocol Repeater Family**
- **Low 65-mW/Channel (Typ) Power Consumption, With Option to Power Down Unused Channels**
- **Transparent Management of Link Training Protocol for PCIe and SAS**
- **Advanced Signal Conditioning Features**
  - **Rx CTLE up to 30 dB (24 dB for SAS3)**
  - **Tx De-Emphasis up to -12 dB**
  - **Tx Output Voltage Control: 700 - 1300 mV**
- **Device Configuration Interface:**
  - **Pin Selection, EEPROM, or SMBus Interface**
- **Single Supply Voltage: 2.5 V or 3.3 V**
- **−40°C to 85°C Operating Temperature Range**
- **3-kV HBM ESD Rating**
- **Flow-Thru Pinout: 54-Pin LLP (10 mm x 5.5 mm, 0.5 mm pitch)**
- **Supported Protocols**
  - **SAS/SATA**
  - **PCIe**
  - **Other Proprietary Interface up to 12.5 Gbps**

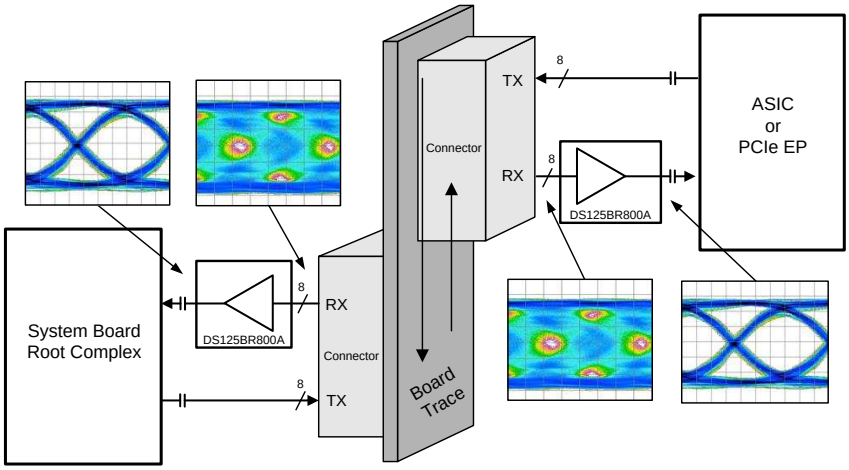
DESCRIPTION

The DS125BR800A is an extremely low-power high-performance multi-protocol repeater/redriver designed to support eight channels of PCIe, SAS, and other high-speed interface serial protocols up to 12.5 Gbps. The receiver's continuous time linear equalizer (CTLE) provides a boost of up to +30 dB at 6.25 GHz (12.5 Gbps) in each of its eight channels and is capable of opening an input eye that is completely closed due to inter symbol interference (ISI) induced by interconnect medium such as 30in+ backplane traces or 8m+ copper cables, hence enabling host controllers to ensure an error free end-to-end link. The strong linear equalization maximizes interconnect channel extension when the DS125BR800A is placed with the majority of channel loss on the devices input side. Adjustable transmit de-emphasis and output voltage amplitude help to compensate for the remaining channel attenuation on the output side.

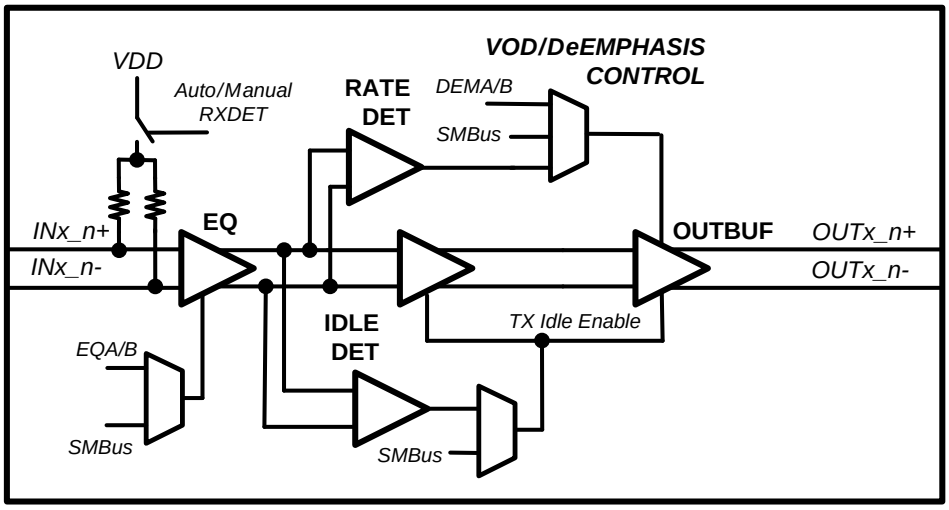
When operating in SAS-3 and PCIe Gen-3 mode, the DS125BR800A transparently allows the host controller and the end point to optimize the full link and negotiate transmit equalizer coefficients. This seamless management of the link training protocol ensures system level interoperability with minimum latency. With a low power consumption of 65 mW/channel (typ) and option to turn-off unused channels, the DS125BR800A enables energy efficient system design. A single supply of 3.3 V or 2.5 V is required to power the device.

The programmable settings can be applied easily via pins, software (SMBus or I2C) or loaded via an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power up, which eliminates the need for an external microprocessor or software driver.

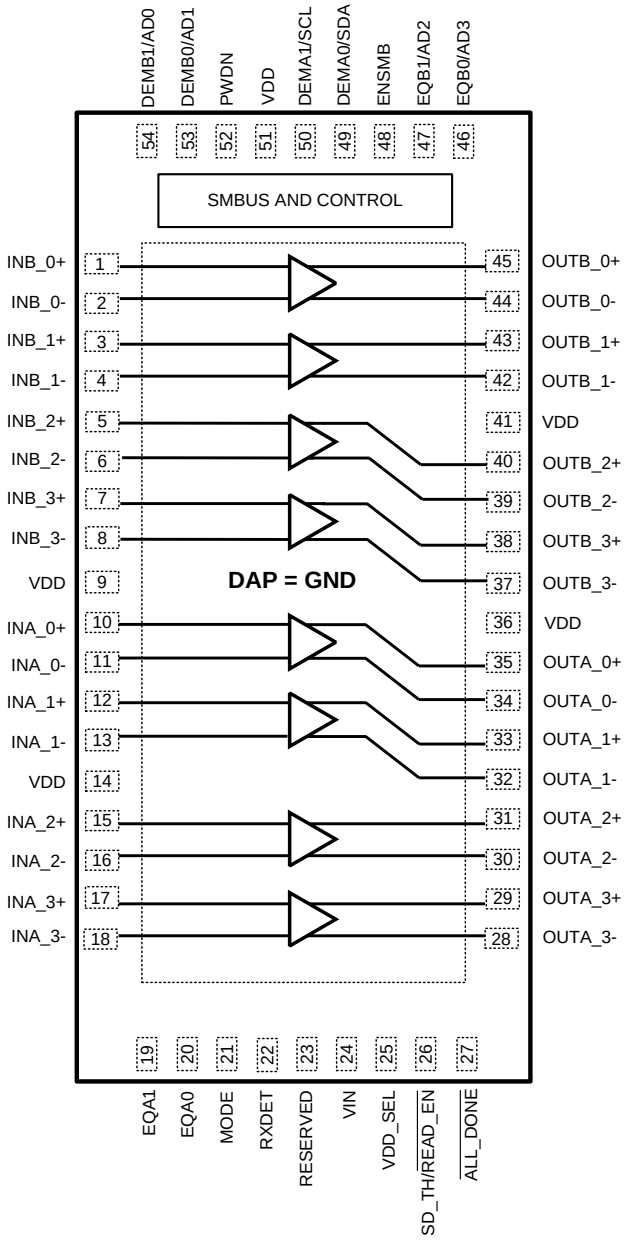
Typical Application



Block Diagram - Detail View Of Channel (1 Of 8)



Pin Diagram



NOTE: Above 54-lead LLP graphic is a TOP VIEW, looking down through the package.

Figure 1. DS125BR800A Pin Diagram 54 lead

Table 1. Pin Descriptions[1]

Pin Name	Pin Number	I/O, Type	Pin Description
Differential High Speed I/O's			
INB_0+, INB_0-,INB_1+, INB_1-,INB_2+, INB_2-,INB_3+, INB_3-	1, 2, 3, 4, 5, 6, 7, 8,	I	Inverting and non-inverting CML differential inputs to the equalizer. On-chip 50Ω termination resistor connects INB_n+ to VDD and INB_n- to VDD when enabled. AC coupling required on high-speed I/O
INA_0+, INA_0-,INA_1+, INA_1-,INA_2+, INA_2-,INA_3+, INA_3-	10, 11, 12, 13, 15, 16, 17, 18	I	Inverting and non-inverting CML differential inputs to the equalizer. On-chip 50Ω termination resistor connects INA_n+ to VDD and INA_n- to VDD when enabled. AC coupling required on high-speed I/O
OUTB_0+, OUTB_0-, OUTB_1+, OUTB_1-, OUTB_2+, OUTB_2-, OUTB_3+, OUTB_3-	45, 44, 43, 42, 40, 39, 38, 37	O	Inverting and non-inverting 50Ω driver outputs with de-emphasis. Compatible with AC coupled CML inputs. AC coupling required on high-speed I/O
OUTA_0+, OUTA_0-, OUTA_1+, OUTA_1-, OUTA_2+, OUTA_2-, OUTA_3+, OUTA_3-	35, 34, 33, 32, 31, 30, 29, 28	O	Inverting and non-inverting 50Ω driver outputs with de-emphasis. Compatible with AC coupled CML inputs. AC coupling required on high-speed I/O
Control Pins — Shared (LVCMOS)			
ENSMB	48	I, 4-LEVEL	System Management Bus (SMBus) enable pin Tie 1kΩ to VDD = Register Access SMBus Slave Mode FLOAT = Read External EEPROM (Master SMBUS Mode) Tie 1kΩ to GND = Pin Mode
ENSMB = 1 (SMBUS MODE)			
SCL	50	I, LVCMOS O, OPEN Drain	ENSMB Master or Slave mode SMBUS clock input is enabled (slave mode). Clock output when loading EEPROM configuration (master mode).
SDA	49	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode The SMBus bidirectional SDA pin is enabled. Data input or open drain (pull-down only) output.
AD0-AD3	54, 53, 47, 46	I, LVCMOS	ENSMB Master or Slave mode SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs.
$\overline{\text{READ\_EN}}$	26	I, LVCMOS	When using an External EEPROM, a transition from high to low starts the load from the external EEPROM
ENSMB = 0 (PIN MODE)			
EQA0, EQA1, EQB0, EQB1	20, 19, 46, 47	I, 4-LEVEL	EQA[1:0] and EQB[1:0] control the level of equalization on the input pins. The pins are active only when ENSMB is de-asserted (low). The 8 channels are organized into two banks. Bank A is controlled with the EQA[1:0] pins and bank B is controlled with the EQB[1:0] pins. When ENSMB goes high the SMBus registers provide independent control of each channel. The EQB[1:0] pins are converted to SMBUS AD2/AD3 inputs. See Table 3.
DEMA0, DEMA1, DEMB0, DEMB1	49, 50, 53, 54	I, 4-LEVEL	DEMA[1:0] and DEMB[1:0] control the level of de-emphasis of the output driver. The pins are only active when ENSMB is de-asserted (low). The 8 channels are organized into two banks. Bank A is controlled with the DEMA[1:0] pins and bank B is controlled with the DEMB[1:0] pins. When ENSMB goes high the SMBus registers provide independent control of each channel. The DEMA[1:0] pins are converted to SMBUS SCL/SDA and DEMB[1:0] pins are converted to AD0, AD1 inputs. See Table 4.
MODE	21	I, 4-LEVEL	MODE control pin selects operating modes. Tie 1kΩ to GND = GEN 1,2 and SAS/SATA (up to 6 Gbps) FLOAT = AUTO Rate Select (for PCIe) Tie 20kΩ to GND = SAS-3 and GEN-3 without De-emphasis Tie 1kΩ to VDD = SAS-3 and GEN-3 with De-emphasis See Table 7

(1) LVCMOS inputs without the "FLOAT" conditions must be driven to a logic low or high at all times or operation is not guaranteed. Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%. For 3.3V mode operation, VIN pin = 3.3V and the "VDD" for the 4-level input is 3.3V. For 2.5V mode operation, VDD pin = 2.5V and the "VDD" for the 4-level input is 2.5V.

Table 1. Pin Descriptions(1) (continued)

Pin Name	Pin Number	I/O, Type	Pin Description
SD_TH	26	I, 4-LEVEL	Controls the internal Signal Detect Threshold. See Table 6.
Control Pins — Both Pin and SMBus Modes (LVCMOS)			
RXDET	22	I, 4-LEVEL	The RXDET pin controls the receiver detect function. Depending on the input level, a 50Ω or >50kΩ termination to the power rail is enabled. See Table 5.
RESERVED	23	I, 4-LEVEL	Float (leave pin open) = Normal Operation
VDD_SEL	25	INPUT	Controls the internal regulator FLOAT = 2.5V mode Tie GND = 3.3V mode
PWDN	52	I, LVCMOS	Tie High = Low power - power down Tie GND = Normal Operation See Table 5.
Outputs			
$\overline{\text{ALL\_DONE}}$	27	O, LVCMOS	Valid Register Load Status Output HIGH = External EEPROM load failed or incomplete LOW = External EEPROM load passed
Power			
VIN	24	Power	In 3.3V mode, feed 3.3V to VIN In 2.5V mode, leave floating
VDD	9, 14, 36, 41, 51	Power	Power supply pins CML/analog 2.5V mode, connect to 2.5V supply 3.3V mode, connect 0.1uF cap to each VDD pin
GND	DAP	Power	Ground pad (DAP - die attach pad)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage (VDD - 2.5V mode)		-0.5V to +2.75V
Supply Voltage (VIN - 3.3V mode)		-0.5V to +4.0V
LVCMOS Input/Output Voltage		-0.5V to +4.0V
CML Input Voltage		-0.5V to (VDD+0.5)
CML Input Current		-30 to +30 mA
Junction Temperature		125°C
Storage Temperature		-40°C to +125°C
Lead Temperature Range Soldering (4 sec.)		+260°C
Derate NJY Package		52.6mW/°C above +25°C
ESD Rating	HBM, STD - JESD22-A114F	3 kV
	CDM, STD - JESD22-C101-D	1000 V
Thermal Resistance	θ_{JC}	11.5°C/W
	θ_{JA}, No Airflow, 4 layer JEDEC	19.1°C/W
For soldering specifications: see product folder at www.ti.com		

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are ensured for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Typ	Max	Unit
Supply voltage (2.5V mode)	2.375	2.5	2.625	V
Supply voltage (3.3V mode)	3.0	3.3	3.6	V
Ambient temperature	-40	25	+85	°C
SMBus (SDA, SCL)			3.6	V
Supply noise up to 50 MHz (1)			100	mVp-p

(1) Allowed supply noise (mVp-p sine wave) under typical conditions.

Electrical Characteristics(1)(2)(3)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power						
PD	Power Dissipation	**VDD = 2.5 V supply**, EQ Enabled, VOD = 1.0 Vp-p, RXDET = 1, PWDN = 0		500	700	mW
		VIN = 3.3 V supply, EQ Enabled, VOD = 1.0 Vp-p, RXDET = 1, PWDN = 0		660	900	mW
LVCMOS / LVTTL DC Specifications						
V_{ih}	High Level Input Voltage		2.0		3.6	V

(1) Typical values represent most likely parametric norms at VDD = 2.5V, TA = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

(2) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

(3) Ensured by device characterization.

Electrical Characteristics[1][2][3] (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{il}	Low Level Input Voltage		0		0.8	V
V_{oh}	High Level Output Voltage (ALL_DONE pin)	I_{oh}= −4mA	2.0			V
V_{ol}	Low Level Output Voltage (ALL_DONE pin)	I_{ol}= 4mA			0.4	V
I_{ih}	Input High Current (PWDN pin)	VIN = 3.6 V (pin 24), Input under test = 3.6 V	-15		+15	uA
	Input High Current with internal resistors (4–level input pin)		+20		+150	uA
I_{il}	Input Low Current (PWDN pin)	VIN = 3.6 V (pin 24), Input under test = 0 V	-15		+15	uA
	Input Low Current with internal resistors (4–level input pin)		-160		-40	uA
CML Receiver Inputs (IN_n+, IN_n-)						
$RL_{rx\text{-}diff}$	RX Differential return loss	0.05 - 7.5 GHz		-15		dB
		7.5 - 15 GHz		-5		dB
$RL_{rx\text{-}cm}$	RX Common mode return loss	0.05 - 5 GHz		-10		dB
$Z_{rx\text{-}dc}$	RX DC common mode impedance	Tested at VDD = 2.5 V	40	50	60	Ω
$Z_{rx\text{-}diff\text{-}dc}$	RX DC differntial mode impedance	Tested at VDD = 2.5 V	80	100	120	Ω
$V_{rx\text{-}diff\text{-}dc}$	Differential RX peak to peak voltage (VID)	Tested at pins	0.6	1.0	1.2	V
$V_{rx\text{-}signal\text{-}det\text{-}diff\text{-}pp}$	Signal detect assert level for active data signal	SD_TH = float, 0101 pattern at 12 Gbps		50		mVp-p
$V_{rx\text{-}idle\text{-}det\text{-}diff\text{-}pp}$	Signal detect de-assert level for electrical idle	SD_TH = float, 0101 pattern at 12 Gbps		37		mVp-p
High Speed Outputs						
$V_{tx\text{-}diff\text{-}pp}$	Output Voltage Differential Swing	Differential measurement with OUT_n+ and OUT_n-, terminated by 50Ω to GND, AC-Coupled, VID = 1.0 Vp-p, DEM0 = 1, DEM1 = 0[4]	0.8	1.0	1.2	Vp-p
$V_{tx\text{-}de\text{-}ratio\_3.5}$	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEM0 = 0, DEM1 = R, Gen 1 and 2 modes only		-3.5		dB
$V_{tx\text{-}de\text{-}ratio\_6}$	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEM0 = R, DEM1 = R Gen1 and 2 modes only		-6		dB
$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	TX Dj > 1.5 MHz				0.15	UI
$T_{TX\text{-}LF\text{-}RMS}$	TX RMS jitter < 1.5 MHz				3.0	ps RMS
$T_{TX\text{-}RISE\text{-}FALL}$	TX rise/fall time	20% to 80% of differential output voltage	35	45		ps
$T_{RF\text{-}MISMATCH}$	TX rise/fall mismatch	20% to 80% of differential output voltage		0.01	0.1	UI
$RL_{TX\text{-}DIFF}$	TX Differential return loss	0.05 - 7.5 GHz		-15		dB
		7.5 - 15 GHz		-5		dB
$RL_{TX\text{-}CM}$	TX Common mode return loss	0.05 - 5 GHz		-10		dB
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential TX impedance			100		Ω
$V_{TX\text{-}CM\text{-}AC\text{-}PP}$	TX AC peak-peak common mode voltage	VOD = 1.0 Vp-p, DEM0 = 1, DEM1 = 0			100	mVpp
$I_{TX\text{-}SHORT}$	TX short circuit current limit	Total current the transmitter can supply when shorted to VDD or GND		20		mA

(4) In SAS3 and GEN3 mode the output VOD level is not fixed. It will be adjusted automatically based on the VID input amplitude level. The output VOD level set by DEMA/B[1:0] is dependent on the VID level and the frequency content. The DS125BR800A repeater in SAS3 and GEN3 mode is designed to be transparent, so the TX-FIR (de-emphasis) is passed to the RX to support link training.

Electrical Characteristics[1][2][3] (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle				100	mV
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode voltage between TX+ and TX-				25	mV
$T_{TX-IDLE-DATA}$	Max time to transition to differential DATA signal after IDLE	VID = 1.0 Vp-p, 3 Gbps		3.5		ns
$T_{TX-DATA-IDLE}$	Max time to transition to IDLE after differential DATA signal	VID = 1.0 Vp-p, 3 Gbps		5.0		ns
$T_{PLHD/PHLD}$	Differential Propagation Delay	EQ = 00[5]		200		ps
T_{LSK}	Lane to lane skew	T = 25C, VDD = 2.5V		25		ps
T_{PPSK}	Part to part propagation delay skew	T = 25C, VDD = 2.5V		40		ps
Equalization						
DJE1	Residual deterministic jitter at 12 Gbps	30in 5mils FR4, VID = 0.6 Vp-p, PRBS15, **EQ = 07'h,** DEM = 0 dB		0.18		UI
DJE2	Residual deterministic jitter at 8 Gbps	30in 5mils FR4, VID = 0.6 Vp-p, PRBS15,**EQ = 07'h,** DEM = 0 dB		0.11		UI
DJE3	Residual deterministic jitter at 5 Gbps	30in 5mils FR4, VID = 0.6 Vp-p, PRBS15, **EQ = 07'h,** DEM = 0 dB		0.07		UI
DJE4	Residual deterministic jitter at 12 Gbps	5m 30 awg cable, VID = 0.6 Vp-p, PRBS15, **EQ = 07'h,** DEM = 0 dB		0.25		UI
DJE5	Residual deterministic jitter at 5 Gbps	8m 30 awg cable, VID = 0.6 Vp-p, PRBS15, **EQ = 0F'h,** DEM = 0 dB		0.33		UI
De-emphasis (GEN 1,2 mode only)						
DJD1	Residual deterministic jitter at 12 Gbps	Input Channel: 20in 5mils FR4, Output Channel: 10in 5mils FR4 VID = 0.6 Vp-p, PRBS15, EQ = 03'h, VOD = 1.0 Vp-p, **DEM = −3.5 dB**		0.1		UI

(5) Propagation Delay measurements will change slightly based on the level of EQ selected. EQ = 00 will result in the shortest propagation delays.

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage	SDA and SCL			0.8	V
V_{IH}	Data, Clock Input High Voltage	SDA and SCL	2.1		3.6	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	(1)	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SCL	(1) (2)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	Pullup V_{DD} = 3.3V (1) (2) (3)		2000		Ω
		Pullup V_{DD} = 2.5V (1) (2) (3)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS						
FSMB	Bus Operating Frequency	ENSMB = VDD (Slave Mode)			400	kHz
		ENSMB = FLOAT (Master Mode)	280	400	520	kHz
TBUF	Bus Free Time Between Stop and Start Condition		1.3			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	0.6			µs
TSU:STA	Repeated Start Condition Setup Time		0.6			µs
TSU:STO	Stop Condition Setup Time		0.6			µs
THD:DAT	Data Hold Time		0			ns
TSU:DAT	Data Setup Time		100			ns
T_{LOW}	Clock Low Period		1.3			µs
T_{HIGH}	Clock High Period	(4)	0.6		50	µs
t_F	Clock/Data Fall Time	(4)			300	ns
t_R	Clock/Data Rise Time	(4)			300	ns
t_{POR}	Time in which a device must be operational after power-on reset	(4) (5)			500	ms

(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Maximum termination voltage should be identical to the device supply voltage.
(4) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.
(5) Ensured by Design. Parameter not tested in production.

TIMING DIAGRAMS

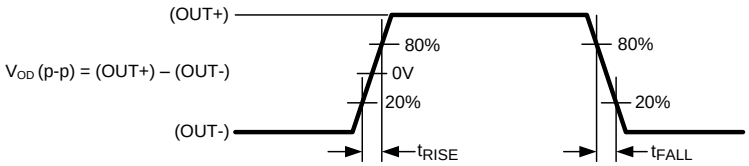


Figure 2. CML Output and Rise and FALL Transition Time

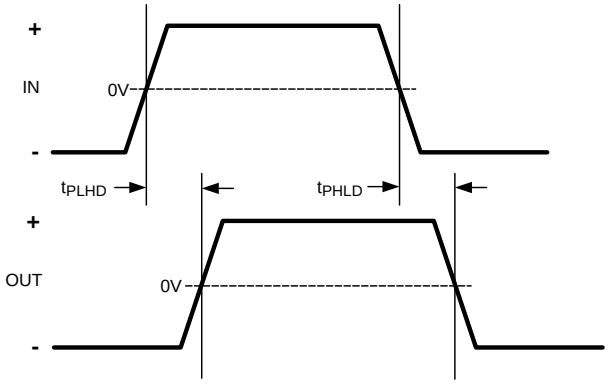


Figure 3. Propagation Delay Timing Diagram

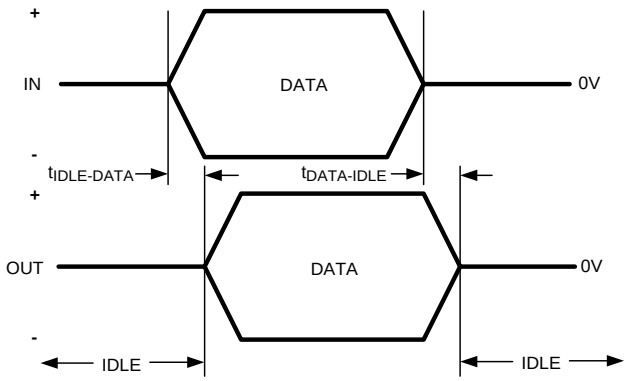


Figure 4. Transmit IDLE-DATA and DATA-IDLE Response Time

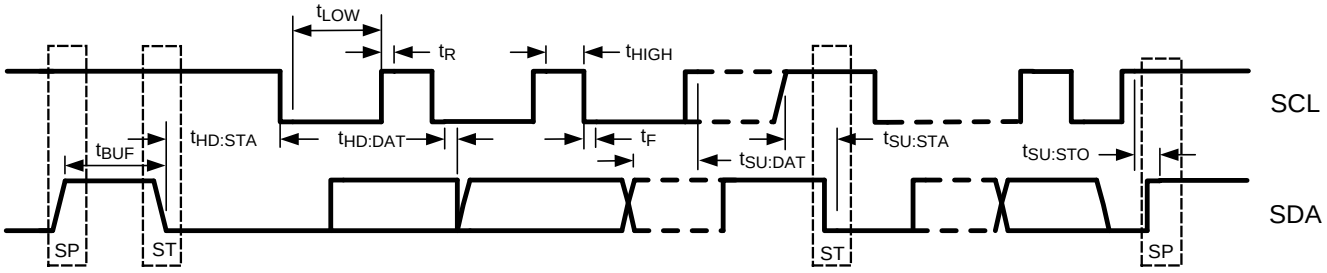


Figure 5. SMBus Timing Parameters

FUNCTIONAL DESCRIPTION

The DS125BR800A compensates for lossy FR-4 printed circuit board backplanes and balanced cables. The DS125BR800A operates in 3 modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = float) to load register information from external EEPROM; please refer to SMBUS Master Mode for additional information.

Pin Control Mode:

When in pin mode (ENSMB = 0), equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically adjusted per Table 4. For PCIe applications, the RXDET pins provides automatic and manual control for input termination (50Ω or >50KΩ). MODE setting is also pin controllable with pin selections (Gen 1/2, auto detect and SAS-3 / PCIe Gen 3). The receiver electrical idle detect threshold is also adjustable via the SD_TH pin.

SMBUS Mode:

When in SMBus mode (ENSMB = 1), the VOD (output amplitude), equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by A or B as in the pin mode case. Upon assertion of ENSMB, the EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins (MODE, RXDET and SD_TH) remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low (pin mode). On power-up and when ENSMB is driven low all registers are reset to their default state. If PWDN is asserted while ENSMB is high, the registers retain their current state.

Equalization settings accessible via the pin controls were chosen to meet the needs of most PCIe applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed via the SMBus registers. Each input has a total of 256 possible equalization settings. The tables show the 16 setting when the device is in pin mode. When using SMBus mode, the equalization, VOD and de-Emphasis levels are set by registers.

The 4-Level input pins utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings when ENSMB=0. There is an internal 30K pull-up and a 60K pull-down connected to the package pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1K pull-up, 1K pull-down, no connect, and 20K pull-down provide the optimal voltage levels for each of the four input states.

Table 2. 4-Level Control Pin Settings

Level	Setting	3.3V Mode	2.5V Mode
0	Tie 1kΩ to GND	0.10 V	0.08 V
R	Tie 20kΩ to GND	1/3 x V_{IN}	1/3 x V_{DD}
Float	Float (leave pin open)	2/3 x V_{IN}	2/3 x V_{DD}
1	Tie 1kΩ to V_{DD}	V_{IN} - 0.05 V	V_{DD} - 0.04 V

Typical 4-Level Input Thresholds

- Level 1 - 2 = 0.2 * V_{IN} or V_{DD}
- Level 2 - 3 = 0.5 * V_{IN} or V_{DD}
- Level 3 - 4 = 0.8 * V_{IN} or V_{DD}

In order to minimize the startup current associated with the integrated 2.5V regulator the 1K pull-up / pull-down resistors are recommended. If several 4 level inputs require the same setting, it is possible to combine two or more 1K resistors into a single lower value resistor. As an example; combining two inputs with a single 500 Ohm resistor is a good way to save board space.

3.3V or 2.5V Supply Mode Operation

The DS125BR800A has an optional internal voltage regulator to provide the 2.5V supply to the device. In 3.3V mode operation, the VIN pin = 3.3V is used to supply power to the device. The internal regulator will provide the 2.5V to the VDD pins of the device and a 0.1 uF cap is needed at each of the 5 VDD pins for power supply de-coupling (total capacitance should be ≤0.5 uF), and the VDD pins should be left open. The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5V mode operation, the VIN pin should be left open and 2.5V supply must be applied to the 5 VDD pins to power the device. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.

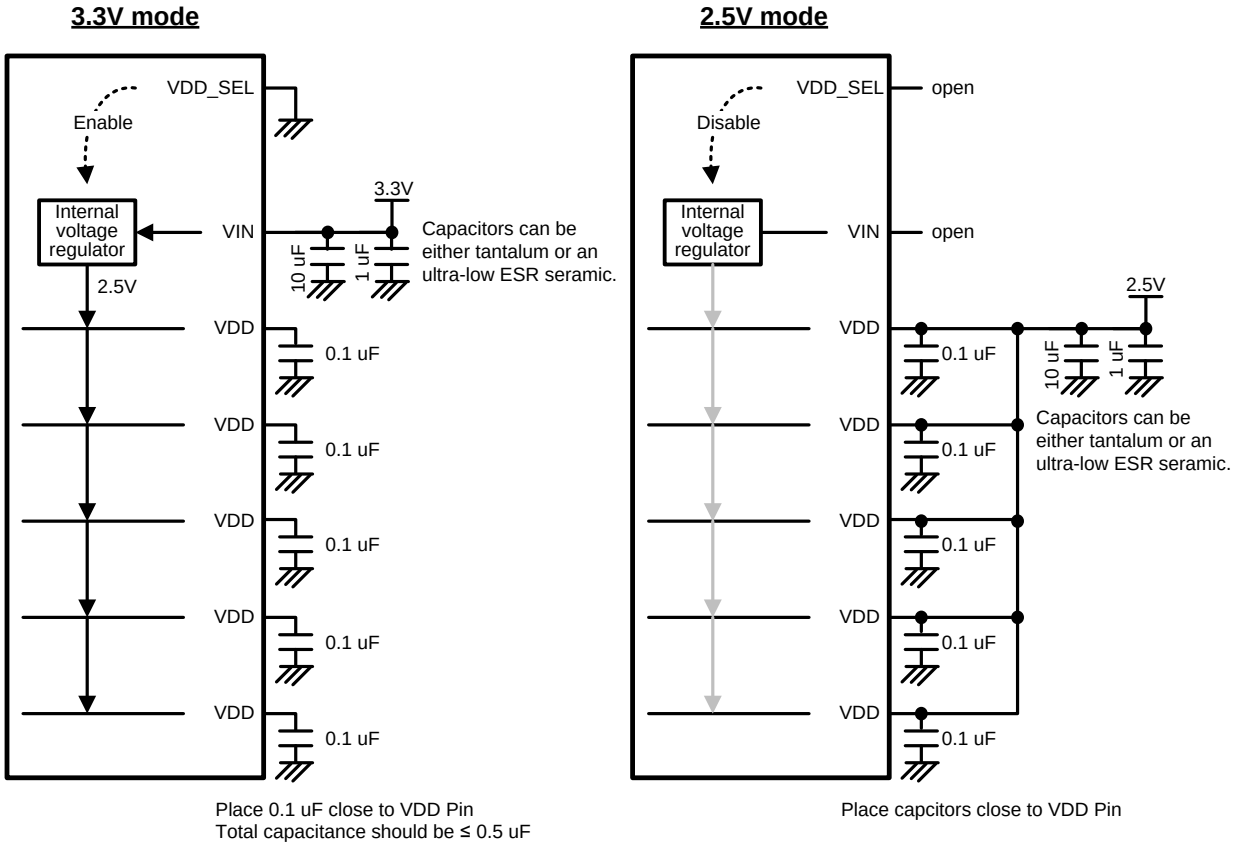


Figure 6. 3.3V or 2.5V Supply Connection Diagram

PCIE SIGNAL INTEGRITY

When using the DS125BR800A in PCIe GEN-3 systems, there are specific signal integrity settings to ensure signal integrity margin. The settings were achieved with completing extensive testing. Please contact your field representative for more information regarding the testing completed to achieve these settings.

For tuning the in the downstream direction (from CPU to EP).

- EQ: use the guidelines outlined in Table 3.
- De-Emphasis: use the guidelines outlined in Table 4.
- VOD: use the guidelines outlined in Table 4.

For tuning in the upstream direction (from EP to CPU).

- EQ: use the guidelines outlined in Table 3.
- De-Emphasis:
  - For trace lengths < 15" set to -3.5 dB
  - For trace lengths > 15" set to -6 dB
- VOD: set to 900 mV

Table 3. Equalizer Settings

Level	EQA1 EQB1	EQA0 EQB	EQ – 8 bits [7:0]	dB at 1.5 GHz	dB at 2.5 GHz	dB at 4 GHz	dB at 6 GHz	Suggested Use(1)
1	0	0	0000 0000 = 0x00	2.5	3.5	3.8	3.1	FR4 < 5 inch trace
2	0	R	0000 0001 = 0x01	3.8	5.4	6.7	6.7	FR4 5-10 inch trace
3	0	Float	0000 0010 = 0x02	5.0	7.0	8.4	8.4	FR4 10 inch trace
4	0	1	0000 0011 = 0x03	5.9	8.0	9.3	9.1	FR4 15-20 inch trace
5	R	0	0000 0111 = 0x07	7.4	10.3	12.8	13.7	FR4 20-30 inch trace
6	R	R	0001 0101 = 0x15	6.9	10.2	13.9	16.2	FR4 25-30 inch trace
7	R	Float	0000 1011 = 0x0B	9.0	12.4	15.3	15.9	FR4 25-30 inch trace
8	R	1	0000 1111 = 0x0F	10.2	13.8	16.7	17.0	8m, 30awg cable
9	Float	0	0101 0101 = 0x55	8.5	12.6	17.5	20.7	> 8m cable
10	Float	R	0001 1111 = 0x1F	11.7	16.2	20.3	21.8	
11	Float	Float	0010 1111 = 0x2F	13.2	18.3	22.8	23.6	
12	Float	1	0011 1111 = 0x3F	14.4	19.8	24.2	24.7	
13	1	0	1010 1010 = 0xAA	14.4	20.5	26.4	28.0	
14	1	R	0111 1111 = 0x7F	16.0	22.2	27.8	29.2	
15	1	Float	1011 1111 = 0xBF	17.6	24.4	30.2	30.9	
16	1	1	1111 1111 = 0xFF	18.7	25.8	31.6	31.9	

(1) Cable and FR4 lengths are for reference only. FR4 lengths based on a 100 Ohm differential stripline with 5-mil traces and 8-mil trace separation. Optimal EQ setting should be determined via simulation and prototype verification.

Table 4. Output Voltage and De-emphasis Settings

Level	DEMA1 DEMB1	DEMA0 DEMB0	VOD Vp-p	DEM dB(1)	Inner Amplitude Vp-p	Suggested Use(2)
1	0	0	0.8	0	0.8	FR4 <5 inch 4–mil trace
2	0	R	0.9	0	0.9	FR4 <5 inch 4–mil trace
3	0	Float	0.9	- 3.5	0.6	FR4 10 inch 4–mil trace
4	0	1	1.0	0	1.0	FR4 <5 inch 4–mil trace
5	R	0	1.0	- 3.5	0.7	FR4 10 inch 4–mil trace
6	R	R	1.0	- 6	0.5	FR4 15 inch 4–mil trace
7	R	Float	1.1	0	1.1	FR4 <5 inch 4–mil trace
8	R	1	1.1	- 3.5	0.7	FR4 10 inch 4–mil trace
9	Float	0	1.1	- 6	0.6	FR4 15 inch 4–mil trace
10	Float	R	1.2	0	1.2	FR4 <5 inch 4–mil trace
11	Float	Float	1.2	- 3.5	0.8	FR4 10 inch 4–mil trace
12	Float	1	1.2	- 6	0.6	FR4 15 inch 4–mil trace
13	1	0	1.3	0	1.3	FR4 <5 inch 4–mil trace
14	1	R	1.3	- 3.5	0.9	FR4 10 inch 4–mil trace
15	1	Float	1.3	- 6	0.7	FR4 15 inch 4–mil trace
16	1	1	1.3	- 9	0.5	FR4 20 inch 4–mil trace

(1) The VOD output amplitude and DEM de-emphasis levels are set with the DEMA/B[1:0] pins. The de-emphasis levels are available in SAS-3 / PCIe GEN-3 modes when MODE = 1

(2) FR4 lengths are for reference only. FR4 lengths based on a 100 Ohm differential stripline with 5-mil traces and 8-mil trace separation. Optimal DEM settings should be determined via simulation and prototype verification.

Table 5. RX-Detect Settings

PWDN (PIN 52)	RXDET (PIN 22)	SMBus REG bit [3:2]	Input Termination	Recommeded Use	Comments
0	0	00	Hi-Z	X	Manual RX-Detect, input is high impedance mode
0	Tie 20kΩ to GND	01	Pre Detect: Hi-Z Post Detect: 50 Ω	PCIe Only	Auto RX-Detect, outputs test every 12 msec for 600 msec then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω Reset function by pulsing PWDN high for 5 usec then low again
0	Float (Default)	10	Pre Detect: Hi-Z Post Detect: 50 Ω	PCIe Only	Auto RX-Detect, outputs test every 12 msec until detection occurs; termination is Hi-Z until RX detection; once detected input termination is 50 Ω
0	1	11	50 Ω	All Others	Manual RX-Detect, input is 50 Ω
1	X		High Impedance	X	Power down mode, input is Hi-Z, output drivers are disabled Used to reset RX-Detect State Machine when held high for 5 usec

RX-Detect in SAS/SATA Applications

Unlike PCIe systems, SAS/SATA systems use a low speed Out-Of-Band or OOB communications sequence to detect and communicate between Controllers/Expanders and target drives. This communication eliminates the need to detect for endpoints like PCIe. For SAS systems, it is recommended to tie the RXDET pin high. This will ensure any OOB sequences sent from the Controller/Expander will reach the target drive without any additional latency due to the termination detection sequence defined by PCIe.

Table 6. OOB and Signal Detect Threshold Level(1)

SD_TH (PIN 26)	SMBus REG bit [3:2] and [1:0]	[3:2] Assert Level (mVp-p)		[1:0] De-assert Level (mVp-p)	
		3 Gbps	12 Gbps	3 Gbps	12 Gbps
0	10	18	75	14	55
R	01	12	40	8	22
F (default)	00	15	50	11	37
1	11	16	58	12	45

(1) VDD = 2.5V, 25°C, 11 00 11 00 pattern at 3 Gbps and 101010 pattern at 12 Gbps

Table 7. MODE Operation With Pin Control

MODE (PIN 21)	Driver Characteristics	PCIe	SAS SATA	10GbE	CPRI OBSAI	SRIO (R)XAUI	Interlaken Infiniband
0	Limiting		X (≤ 6G)	X	X	X	X
R	Transparent without DE						
F (default)	Automatic	X					
1	Transparent with DE		X (SAS-3)				

MODE operation with SMBus Registers

When in SMBus mode (Slave or Master), the MODE pin retains control of the output driver characteristics. In order to override this control function, Register 0x08[2] must be written with a "1". Writting this bit enables MODE control of each channel individually using the channel registers defined in Table 11.

SMBUS MASTER MODE

The DS125BR800A devices support reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS125BR800A will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines.

- Maximum EEPROM size is 8 kbits (1024 x 8-bit)
- Set ENSMB = Float — enable the SMBUS master mode.
- The external EEPROM device address byte must be 0xA0'h and capable of 400 kHz operation at 2.5V and 3.3V supply.
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is B0'h.

When tying multiple DS125BR800A devices to the SDA and SCL bus, use these guidelines to configure the devices.

- Use SMBus AD[3:0] address bits so that each device can loaded it's configuration from the EEPROM. Example below is for 4 devices. The first device n the sequence must be address 0xB0'h, subsequent devices must follow the address order listed below.
  - U1: AD[3:0] = 0000 = 0xB0'h,
  - U2: AD[3:0] = 0001 = 0xB2'h,
  - U3: AD[3:0] = 0010 = 0xB4'h,
  - U4: AD[3:0] = 0011 = 0xB6'h
- Use a pull-up resistor on SDA and SCL; value = 2k ohms
- Daisy-chain READEN# (pin 26) and ALL_DONE# (pin 27) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
  1. Tie READEN# of the 1st device in the chain (U1) to GND
  2. Tie ALL_DONE# of U1 to READEN# of U2
  3. Tie ALL_DONE# of U2 to READEN# of U3
  4. Tie ALL_DONE# of U3 to READEN# of U4
  5. Optional: Tie ALL_DONE# output of U4 to a LED to show the devices have been loaded successfully

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for the DS125BR800A device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the I2C bus. CRC enable flag to enable/disable CRC checking. If CRC checking is disabled, a fixed pattern (8'hA5) is written/read instead of the CRC byte from the CRC location, to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS125BR800A address and the configuration data size. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS125BR800A device.

```
:20000000000010000004070 02FAD4002FAD4002FAD4002FAD401805F5A8005F5A8005F5AD8
:20002000 8005F5A800005454 0000000000000000000000000000000000000000000000F6
:20006000000000000000000000000000000000000000000000000000000000000000000080
:20008000000000000000000000000000000000000000000000000000000000000000000060
:2000A000000000000000000000000000000000000000000000000000000000000000000040
:2000C000000000000000000000000000000000000000000000000000000000000000000020
:2000E000000000000000000000000000000000000000000000000000000000000000000000
:20004000000000000000000000000000000000000000000000000000000000000000000A0
```

Note: The maximum EEPROM size supported is 8 kbits (1024 x 8-bits).

Table 8. EEPROM Register Map - Single Device with Default Value

EEPROM Address Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Description	0	CRC EN	Address Map Present	EEPROM > 256 Bytes	RES	DEVICE COUNT[3]	DEVICE COUNT[2]	DEVICE COUNT[1]	DEVICE COUNT[0]
Value		0	0	0	0	0	0	0	0
Description	1	RES	RES	RES	RES	RES	RES	RES	RES
Value		0	0	0	0	0	0	0	0
Description	2	Max EEPROM Burst size[7]	Max EEPROM Burst size[6]	Max EEPROM Burst size[5]	Max EEPROM Burst size[4]	Max EEPROM Burst size[3]	Max EEPROM Burst size[2]	Max EEPROM Burst size[1]	Max EEPROM Burst size[0]
Value		0	0	0	0	0	0	0	0
Description	3	PWDN_ch7	PWDN_ch6	PWDN_ch5	PWDN_ch4	PWDN_ch3	PWDN_ch2	PWDN_ch1	PWDN_ch0
Value		0	0	0	0	0	0	0	0
Description	4	lpbk_1	lpbk_0	PWDN_INPUTS	PWDN_OSC	Ovrd_PWDN	ch7_BST_8	ch7_BST_8	ch7_BST_8
Value		0	0	0	0	0	0	0	0
Description	5	ch7_BST_8	ch7_BST_8	ch7_BST_8	ch7_BST_8	ch7_BST_8	rxdet_btb_en	Ovrd_idle_th	Ovrd_RES
Value		0	0	0	0	0	1	0	0
Description	6	Ovrd_IDLE	Ovrd_RX_DET	Ovrd_MODE	Ovrd_RES	Ovrd_RES	rx_delay_sel_2	rx_delay_sel_1	rx_delay_sel_0
Value		0	0	0	0	0	1	1	1
Description	7	RD_delay_sel_3	RD_delay_sel_2	RD_delay_sel_1	RD_delay_sel_0	ch0_Idle_auto	ch0_Idle_sel	ch0_RXDET_1	ch0_RXDET_0
Value		0	0	0	0	0	0	0	0
Description	8	ch0_BST_7	ch0_BST_6	ch0_BST_5	ch0_BST_4	ch0_BST_3	ch0_BST_2	ch0_BST_1	ch0_BST_0
Value		0	0	1	0	1	1	1	1
Description	9	ch0_Sel_scp	ch0_Sel_mode	ch0_RES_2	ch0_RES_1	ch0_RES_0	ch0_VOD_2	ch0_VOD_1	ch0_VOD_0
Value		1	0	1	0	1	1	0	1
Description	10	ch0_DEM_2	ch0_DEM_1	ch0_DEM_0	ch0_Slow	ch0_idle_tha_1	ch0_idle_tha_0	ch0_idle_thd_1	ch0_idle_thd_0
Value		0	1	0	0	0	0	0	0
Description	11	ch1_Idle_auto	ch1_Idle_sel	ch1_RXDET_1	ch1_RXDET_0	ch1_BST_7	ch1_BST_6	ch1_BST_5	ch1_BST_4
Value		0	0	0	0	0	0	1	0
Description	12	ch1_BST_3	ch1_BST_2	ch1_BST_1	ch1_BST_0	ch1_Sel_scp	ch1_Sel_mode	ch1_RES_2	ch1_RES_1
Value		1	1	1	1	1	0	1	0
Description	13	ch1_RES_0	ch1_VOD_2	ch1_VOD_1	ch1_VOD_0	ch1_DEM_2	ch1_DEM_1	ch1_DEM_0	ch1_Slow
Value		1	1	0	1	0	1	0	0
Description	14	ch1_idle_tha_1	ch1_idle_tha_0	ch1_idle_thd_1	ch1_idle_thd_0	ch2_Idle_auto	ch2_Idle_sel	ch2_RXDET_1	ch2_RXDET_0
Value		0	0	0	0	0	0	0	0
Description	15	ch2_BST_7	ch2_BST_6	ch2_BST_5	ch2_BST_4	ch2_BST_3	ch2_BST_2	ch2_BST_1	ch2_BST_0
Value		0	0	1	0	1	1	1	1
Description	16	ch2_Sel_scp	ch2_Sel_mode	ch2_RES_2	ch2_RES_1	ch2_RES_0	ch2_VOD_2	ch2_VOD_1	ch2_VOD_0
Value		1	0	1	0	1	1	0	1

Table 8. EEPROM Register Map - Single Device with Default Value (continued)

EEPROM Address Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Description	17	ch2_DEM_2	ch2_DEM_1	ch2_DEM_0	ch2_Slow	ch2_idle_tha_1	ch2_idle_tha_0	ch2_idle_thd_1	ch2_idle_thd_0
Value		0	1	0	0	0	0	0	0
Description	18	ch3_Idle_auto	ch3_Idle_sel	ch3_RXDET_1	ch3_RXDET_0	ch3_BST_7	ch3_BST_6	ch3_BST_5	ch3_BST_4
Value		0	0	0	0	0	0	1	0
Description	19	ch3_BST_3	ch3_BST_2	ch3_BST_1	ch3_BST_0	ch3_Sel_scp	ch3_Sel_mode	ch3_RES_2	ch3_RES_1
Value		1	1	1	1	1	0	1	0
Description	20	ch3_RES_0	ch3_VOD_2	ch3_VOD_1	ch3_VOD_0	ch3_DEM_2	ch3_DEM_1	ch3_DEM_0	ch3_Slow
Value		1	1	0	1	0	1	0	0
Description	21	ch3_idle_tha_1	ch3_idle_tha_0	ch3_idle_thd_1	ch3_idle_thd_0	ovrd_fast_idle	en_high_idle_th_n	en_high_idle_th_s	en_fast_idle_n
Value		0	0	0	0	0	0	0	1
Description	22	en_fast_idle_s	eqsd_mgain_n	eqsd_mgain_s	ch4_Idle_auto	ch4_Idle_sel	ch4_RXDET_1	ch4_RXDET_0	ch4_BST_7
Value		1	0	0	0	0	0	0	0
Description	23	ch4_BST_6	ch4_BST_5	ch4_BST_4	ch4_BST_3	ch4_BST_2	ch4_BST_1	ch4_BST_0	ch4_Sel_scp
Value		0	1	0	1	1	1	1	1
Description	24	ch4_Sel_mode	ch4_RES_2	ch4_RES_1	ch4_RES_0	ch4_VOD_2	ch4_VOD_1	ch4_VOD_0	ch4_DEM_2
Value		0	1	0	1	1	0	1	0
Description	25	ch4_DEM_1	ch4_DEM_0	ch4_Slow	ch4_idle_tha_1	ch4_idle_tha_0	ch4_idle_thd_1	ch4_idle_thd_0	ch5_Idle_auto
Value		1	0	0	0	0	0	0	0
Description	26	ch5_Idle_sel	ch5_RXDET_1	ch5_RXDET_0	ch5_BST_7	ch5_BST_6	ch5_BST_5	ch5_BST_4	ch5_BST_3
Value		0	0	0	0	0	1	0	1
Description	27	ch5_BST_2	ch5_BST_1	ch5_BST_0	ch5_Sel_scp	ch5_Sel_mode	ch5_RES_2	ch5_RES_1	ch5_RES_0
Value		1	1	1	1	0	1	0	1
Description	28	ch5_VOD_2	ch5_VOD_1	ch5_VOD_0	ch5_DEM_2	ch5_DEM_1	ch5_DEM_0	ch5_Slow	ch5_idle_tha_1
Value		1	0	1	0	1	0	0	0
Description	29	ch5_idle_tha_0	ch5_idle_thd_1	ch5_idle_thd_0	ch6_Idle_auto	ch6_Idle_sel	ch6_RXDET_1	ch6_RXDET_0	ch6_BST_7
Value		0	0	0	0	0	0	0	0
Description	30	ch6_BST_6	ch6_BST_5	ch6_BST_4	ch6_BST_3	ch6_BST_2	ch6_BST_1	ch6_BST_0	ch6_Sel_scp
Value		0	1	0	1	1	1	1	1
Description	31	ch6_Sel_mode	ch6_RES_2	ch6_RES_1	ch6_RES_0	ch6_VOD_2	ch6_VOD_1	ch6_VOD_0	ch6_DEM_2
Value		0	1	0	1	1	0	1	0
Description	32	ch6_DEM_1	ch6_DEM_0	ch6_Slow	ch6_idle_tha_1	ch6_idle_tha_0	ch6_idle_thd_1	ch6_idle_thd_0	ch7_Idle_auto
Value		1	0	0	0	0	0	0	0
Description	33	ch7_Idle_sel	ch7_RXDET_1	ch7_RXDET_0	ch7_BST_7	ch7_BST_6	ch7_BST_5	ch7_BST_4	ch7_BST_3
Value		0	0	0	0	0	1	0	1
Description	34	ch7_BST_2	ch7_BST_1	ch7_BST_0	ch7_Sel_scp	ch7_Sel_mode	ch7_RES_2	ch7_RES_1	ch7_RES_0
Value		1	1	1	1	0	1	0	1

Table 8. EEPROM Register Map - Single Device with Default Value (continued)

EEPROM Address Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Description	35	ch7_VOD_2	ch7_VOD_1	ch7_VOD_0	ch7_DEM_2	ch7_DEM_1	ch7_DEM_0	ch7_Slow	ch7_idle_tha_1
Value		1	0	1	0	1	0	0	0
Description	36	ch7_idle_tha_0	ch7_idle_thd_1	ch7_idle_thd_0	iph_dac_ns_1	iph_dac_ns_0	ipp_dac_ns_1	ipp_dac_ns_0	ipp_dac_1
Value		0	0	0	0	0	0	0	0
Description	37	ipp_dac_0	RD23_67	RD01_45	RD_PD_ovrd	RD_Sel_test	RD_RESET_ovrd	PWDB_input_DC	DEM_VOD_ovrd
Value		0	0	0	0	0	0	0	0
Description	38	DEM_ovrd_N2	DEM_ovrd_N1	DEM_ovrd_N0	VOD_ovrd_N2	VOD_ovrd_N1	VOD_ovrd_N0	SPARE0	SPARE1
Value		0	1	0	1	0	1	0	0
Description	39	DEM__ovrd_S2	DEM__ovrd_S1	DEM_ovrd_S0	VOD_ovrd_S2	VOD_ovrd_S1	VOD_ovrd_S0	SPARE0	SPARE1
Value		0	1	0	1	0	1	0	0

Table 9. Example of EEPROM for Four Devices Using Two Address Maps

EEPROM Address	Address (Hex)	EEPROM Data	Comments
0	00	0x43	CRC_EN = 0, Address Map = 1, >256 bytes = 0, Device Count[3:0] = 3
1	01	0x00	
2	02	0x08	EEPROM Burst Size
3	03	0x00	CRC not used
4	04	0x0B	Device 0 Address Location
5	05	0x00	CRC not used
6	06	0x0B	Device 1 Address Location
7	07	0x00	CRC not used
8	08	0x30	Device 2 Address Location
9	09	0x00	CRC not used
10	0A	0x30	Device 3 Address Location
11	0B	0x00	Begin Device 0, 1 - Address Offset 3
12	0C	0x00	
13	0D	0x04	
14	0E	0x07	
15	0F	0x00	
16	10	0x00	EQ CHB0 = 00
17	11	0xAB	VOD CHB0 = 1.0V
18	12	0x00	DEM CHB0 = 0 (0dB)
19	13	0x00	EQ CHB1 = 00
20	14	0x0A	VOD CHB1 = 1.0V
21	15	0xB0	DEM CHB1 = 0 (0dB)
22	16	0x00	
23	17	0x00	EQ CHB2 = 00
24	18	0xAB	VOD CHB2 = 1.0V
25	19	0x00	DEM CHB2 = 0 (0dB)
26	1A	0x00	EQ CHB3 = 00
27	1B	0x0A	VOD CHB3 = 1.0V
28	1C	0xB0	DEM CHB3 = 0 (0dB)
29	1D	0x01	
30	1E	0x80	
31	1F	0x01	EQ CHA0 = 00
32	20	0x56	VOD CHA0 = 1.0V
33	21	0x00	DEM CHA0 = 0 (0dB)
34	22	0x00	EQ CHA1 = 00
35	23	0x15	VOD CHA1 = 1.0V
36	24	0x60	DEM CHA1 = 0 (0dB)
37	25	0x00	
38	26	0x01	EQ CHA2 = 00
39	27	0x56	VOD CHA2 = 1.0V
40	28	0x00	DEM CHA2 = 0 (0dB)
41	29	0x00	EQ CHA3 = 00
42	2A	0x15	VOD CHA3 = 1.0V
43	2B	0x60	DEM CHA3 = 0 (0dB)
44	2C	0x00	
45	2D	0x00	
46	2E	0x54	

Table 9. Example of EEPROM for Four Devices Using Two Address Maps (continued)

47	2F	0x54	End Device 0, 1 - Address Offset 39
48	30	0x00	Begin Device 2, 3 - Address Offset 3
49	31	0x00	
50	32	0x04	
51	33	0x07	
52	34	0x00	
53	35	0x00	EQ CHB0 = 00
54	36	0xAB	VOD CHB0 = 1.0V
55	37	0x00	DEM CHB0 = 0 (0dB)
56	38	0x00	EQ CHB1 = 00
57	39	0x0A	VOD CHB1 = 1.0V
58	3A	0xB0	DEM CHB1 = 0 (0dB)
59	3B	0x00	
60	3C	0x00	EQ CHB2 = 00
61	3D	0xAB	VOD CHB2 = 1.0V
62	3E	0x00	DEM CHB2 = 0 (0dB)
63	3F	0x00	EQ CHB3 = 00
64	40	0x0A	VOD CHB3 = 1.0V
65	41	0xB0	DEM CHB3 = 0 (0dB)
66	42	0x01	
67	43	0x80	
68	44	0x01	EQ CHA0 = 00
69	45	0x56	VOD CHA0 = 1.0V
70	46	0x00	DEM CHA0 = 0 (0dB)
71	47	0x00	EQ CHA1 = 00
72	48	0x15	VOD CHA1 = 1.0V
73	49	0x60	DEM CHA1 = 0 (0dB)
74	4A	0x00	
75	4B	0x01	EQ CHA2 = 00
76	4C	0x56	VOD CHA2 = 1.0V
77	4D	0x00	DEM CHA2 = 0 (0dB)
78	4E	0x00	EQ CHA3 = 00
79	4F	0x15	VOD CHA3 = 1.0V
80	50	0x60	DEM CHA3 = 0 (0dB)
81	51	0x00	
82	52	0x00	
83	53	0x54	
84	54	0x54	End Device 2, 3 - Address Offset 39

NOTE: CRC_EN = 0, Address Map = 1, >256 byte = 0, Device Count[3:0] = 3. This example has all 8 channels set to EQ = 00 (min boost), VOD = 1.0V, DEM = 0 (0dB) and multiple device can point to the same address map.

Maximum EEPROM size is 8 kbits (1024 x 8-bits).

SYSTEM MANAGEMENT BUS (SMBUS) AND CONFIGURATION REGISTERS

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB = 1kΩ to VDD to enable SMBus slave mode and allow access to the configuration registers.

The DS125BR800A has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBUS slave address inputs. The AD[3:0] pins have internal pull-down. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is B0'h. Based on the SMBus 2.0 specification, the DS125BR800A has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). The device supports up to 16 address byte, which can be set with the AD[3:0] inputs. Below are the 16 addresses.

Table 10. Device Slave Address Bytes

AD[3:0] Settings	Address Bytes (HEX)
0000	B0
0001	B2
0010	B4
0011	B6
0100	B8
0101	BA
0110	BC
0111	BE
1000	C0
1001	C2
1010	C4
1011	C6
1100	C8
1101	CA
1110	CC
1111	CE

The SDA, SCL pins are 3.3V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 kΩ to 5 kΩ depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See Table 11 for register address, type (Read/Write, Read Only), default value and function information.

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
2. The Device (Slave) drives the ACK bit ("0").
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit ("0").

5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit ("0").
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
2. The Device (Slave) drives the ACK bit ("0").
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit ("0").
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a "1" indicating a READ.
7. The Device drives an ACK bit "0".
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit "1"indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

See Table 11 for more information.

Table 11. SMBUS Slave Mode Register Map

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x00	Observation, Reset	7	Reserved	R/W	0x00	Set bit to 0.
		6:3	Address Bit AD[3:0]	R		Observation of AD[3:0] bit [6]: AD3 [5]: AD2 [4]: AD1 [3]: AD0
		2	EEPROM Read Done	R		1: Device completed the read from external EEPROM.
		1	Reserved	R/W		Set bit to 0.
		0	Reserved	R/W		Set bit to 0.
0x01	PWDN Channels	7:0	PWDN CHx	R/W	0x00	Power Down per Channel [7]: CH7 – CHA_3 [6]: CH6 – CHA_2 [5]: CH5 – CHA_1 [4]: CH4 – CHA_0 [3]: CH3 – CHB_3 [2]: CH2 – CHB_2 [1]: CH1 – CHB_1 [0]: CH0 – CHB_0 00'h = all channels enabled FF'h = all channels disabled Note: override PWDN pin.
0x02	Override PWDN Control	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Override PWDN			1: Block PWDN pin control 0: Allow PWDN pin control
0x04	EQ Limiting	7:0	EQ Control	R/W	0x00	CH7 - CH0 EQ Limiting Control 1 = EQ Limits 0 = EQ Linear (Default)
0x05	Slave Mode CRC Bits	7:0	CRC bits	R/W	0x00	CRC bits [7:0]
0x06	Slave Register Control	7:5	Reserved	R/W	0x10	Set bits to 0.
		4	Reserved			Set bit to 1.
		3	Register Enable			1: Enables high speed channel control via SMBus registers without CRC 0: Channel control via SMBus registers requires correct CRC in Reg 0x05 Note: In order to change VOD, DEM and EQ of the channels in slave mode without also setting CRC each time, set this bit to 1.
		2:0	Reserved			Set bits to 0.
0x07	Digital Reset and Control	7	Reserved	R/W	0x01	Set bit to 0.
		6	Reset Registers			Self clearing reset for SMBus registers. Writing a [1] will return register settings to default values
		5	Reset SMBus Master			Self clearing reset to SMBus master state machine
		4:0	Reserved			Set bits to 0 0001'b.
0x08	Override Pin Control	7	Reserved	R/W	0x00	Set bit to 0.
		6	Override SD_TH			1: Block SD_TH pin control 0: Allow SD_TH pin control
		5	Reserved			Set bit to 0.
		4	Override IDLE			1: IDLE control by registers 0: IDLE control by signal detect
		3	Override RXDET			1: Block RXDET pin control 0: Allow RXDET pin control
		2	Override MODE			1: Block MODE pin control 0: Allow MODE pin control
		1	Reserved			Set bit to 0.
		0	Reserved			Set bit to 0.

Table 11. SMBUS Slave Mode Register Map (continued)

0x0E	CH0 - CHB0 IDLE, RXDET	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE_AUTO			1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x0F	CH0 - CHB0 EQ	7:0	EQ Control	R/W	0x2F	IB0 EQ Control - total of 256 levels. See Table 3.
0x10	CH0 - CHB0 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE_SEL			1: PCIe Gen 1/2, 0: SAS-3 and PCIe Gen 3 Note: override the MODE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OB0 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V
0x11	CH0 - CHB0 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH0 - CHB0. 1: RX = detected 0: RX = not detected
		6:5	MODE_DET STATUS	R		Observation bit for MODE_DET CH0 - CHB0. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G+) Note: Only functions when Mode pin = Automatic
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OB0 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB

Table 11. SMBUS Slave Mode Register Map (continued)

0x12	CH0 - CHB0 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE tha			Assert threshold (1010 pattern 12 Gbps) 00 = 50 mVp-p (default) 01 = 40 mVp-p 10 = 75 mVp-p 11 = 58 mVp-p Note: override the SD_TH pin.
		1:0	IDLE thd			De-assert threshold (1010 pattern 12 Gbps) 00 = 37 mVp-p (default) 01 = 22 mVp-p 10 = 55 mVp-p 11 = 45 mVp-p Note: override the SD_TH pin.
0x15	CH1 - CHB1 IDLE, RXDET	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE_AUTO			1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x16	CH1 - CHB1 EQ	7:0	EQ Control	R/W	0x2F	IB1 EQ Control - total of 256 levels. See Table 3.
0x17	CH1 - CHB1 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE_SEL			1: Gen 1/2, 0: SAS-3 and PCIe Gen 3 Note: override the MODE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OB1 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V

Table 11. SMBUS Slave Mode Register Map (continued)

0x18	CH1 - CHB1 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH1 - CHB1. 1: RX = detected 0: RX = not detected
		6:5	MODE_DET STATUS	R		Observation bit for MODE_DET CH1 - CHB1. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G+) Note: Only functions when Mode pin = Automatic
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OB1 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x19	CH1 - CHB1 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE tha			Assert threshold (1010 pattern 12 Gbps) 00 = 50 mVp-p (default) 01 = 40 mVp-p 10 = 75 mVp-p 11 = 58 mVp-p Note: override the SD_TH pin.
		1:0	IDLE thd			De-assert threshold (1010 pattern 12 Gbps) 00 = 37 mVp-p (default) 01 = 22 mVp-p 10 = 55 mVp-p 11 = 45 mVp-p Note: override the SD_TH pin.
0x1C	CH2 - CHB2 IDLE, RXDET	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE_AUTO			1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x1D	CH2 - CHB2 EQ	7:0	EQ Control	R/W	0x2F	IB2 EQ Control - total of 256 levels. See Table 3.

Table 11. SMBUS Slave Mode Register Map (continued)

0x1E	CH2 - CHB2 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE_SEL			1: Gen 1/2, 0: SAS-3 and PCIe Gen-3 Note: override the MODE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OB2 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V
0x1F	CH2 - CHB2 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH2 - CHB2. 1: RX = detected 0: RX = not detected
		6:5	MODE_DET STATUS	R		Observation bit for MODE_DET CH2 - CHB2. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) Note: Only functions when Mode pin = Automatic
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OB2 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x20	CH2 - CHB2 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE tha			Assert threshold (1010 pattern 12 Gbps) 00 = 50 mVp-p (default) 01 = 40 mVp-p 10 = 75 mVp-p 11 = 58 mVp-p Note: override the SD_TH pin.
		1:0	IDLE thd			De-assert threshold (1010 pattern 12 Gbps) 00 = 37 mVp-p (default) 01 = 22 mVp-p 10 = 55 mVp-p 11 = 45 mVp-p Note: override the SD_TH pin.

Table 11. SMBUS Slave Mode Register Map (continued)

0x23	CH3 - CHB3 IDLE, RXDET	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE_AUTO			1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x24	CH3 - CHB3 EQ	7:0	EQ Control	R/W	0x2F	IB3 EQ Control - total of 256 levels. See Table 3.
0x25	CH3 - CHB3 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE_SEL			1: Gen 1/2, 0: SAS-3 and PCIe Gen-3 Note: override the MODE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OB0 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V
0x26	CH3 - CHB3 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH3 - CHB3. 1: RX = detected 0: RX = not detected
		6:5	MODE_DET STATUS	R		Observation bit for MODE_DET CH3 - CHB3. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) Note: Only functions when Mode pin = Automatic
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OB3 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB

Table 11. SMBUS Slave Mode Register Map (continued)

0x27	CH3 - CHB3 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE tha			Assert threshold (1010 pattern 12 Gbps) 00 = 50 mVp-p (default) 01 = 40 mVp-p 10 = 75 mVp-p 11 = 58 mVp-p Note: override the SD_TH pin.
		1:0	IDLE thd			De-assert threshold (1010 pattern 12 Gbps) 00 = 37 mVp-p (default) 01 = 22 mVp-p 10 = 55 mVp-p 11 = 45 mVp-p Note: override the SD_TH pin.
0x28	Signal Detect Control	7	Reserved	R/W	0x4C	Set bit to 0.
		6	Override Fast IDLE			Override Fast IDLE [1]: Use values in 0x28[3:2] [0]: Based on MODE pin
		5:4	High IDLE			Enable higher range of Signal Detect Thresholds [1]: CH0 - CH3 [0]: CH4 - CH7
		3:2	Fast IDLE			Enable Fast OOB response [1]: CH0 - CH3 [0]: CH4 - CH7
		1:0	Reduced SD Gain			Enable reduced Signal Detect Gain [1]: CH0 - CH3 [0]: CH4 - CH7
0x2B	CH4 - CHA0 IDLE, RXDET	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE_AUTO			1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x2C	CH4 - CHA0 EQ	7:0	EQ Control	R/W	0x2F	IA0 EQ Control - total of 256 levels. See Table 3.
0x2D	CH4 - CHA0 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE_SEL			1: Gen 1/2, 0: SAS-3 and PCIe Gen-3 Note: override the MODE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OA0 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V

Table 11. SMBUS Slave Mode Register Map (continued)

0x2E	CH4 - CHA0 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH4 - CHA0. 1: RX = detected 0: RX = not detected
		6:5	MODE_DET STATUS	R		Observation bit for MODE_DET CH4 - CHA0. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) Note: Only functions when Mode pin = Automatic
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OA0 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x2F	CH4 - CHA0 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE tha			Assert threshold (1010 pattern 12 Gbps) 00 = 50 mVp-p (default) 01 = 40 mVp-p 10 = 75 mVp-p 11 = 58 mVp-p Note: override the SD_TH pin.
		1:0	IDLE thd			De-assert threshold (1010 pattern 12 Gbps) 00 = 37 mVp-p (default) 01 = 22 mVp-p 10 = 55 mVp-p 11 = 45 mVp-p Note: override the SD_TH pin.
0x32	CH5 - CHA1 IDLE, RXDET	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE_AUTO			1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x33	CH5 - CHA1 EQ	7:0	EQ Control	R/W	0x2F	IA1 EQ Control - total of 256 levels. See Table 3.

Table 11. SMBUS Slave Mode Register Map (continued)

0x34	CH5 - CHA1 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE_SEL			1: Gen 1/2, 0: SAS-3 and PCIe Gen-3 Note: override the MODE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OA1 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V
0x35	CH5 - CHA1 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH5 - CHA1. 1: RX = detected 0: RX = not detected
		6:5	MODE_DET STATUS	R		Observation bit for MODE_DET CH5 - CHA1. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) Note: Only functions when Mode pin = Automatic
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OA1 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x36	CH5 - CHA1 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE tha			Assert threshold (1010 pattern 12 Gbps) 00 = 50 mVp-p (default) 01 = 40 mVp-p 10 = 75 mVp-p 11 = 58 mVp-p Note: override the SD_TH pin.
		1:0	IDLE thd			De-assert threshold (1010 pattern 12 Gbps) 00 = 37 mVp-p (default) 01 = 22 mVp-p 10 = 55 mVp-p 11 = 45 mVp-p Note: override the SD_TH pin.

Table 11. SMBUS Slave Mode Register Map (continued)

0x39	CH6 - CHA2 IDLE, RXDET	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE_AUTO			1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x3A	CH6 - CHA2 EQ	7:0	EQ Control	R/W	0x2F	IA2 EQ Control - total of 256 levels. See Table 3.
0x3B	CH6 - CHA2 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE_SEL			1: PCIe Gen 1/2, 0: SAS-3 and PCIe Gen-3 Note: override the MODE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OA2 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V
0x3C	CH6 - CHA2 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH6 - CHA2. 1: RX = detected 0: RX = not detected
		6:5	MODE_DET STATUS	R		Observation bit for MODE_DET CH6 - CHA2. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) Note: Only functions when Mode pin = Automatic
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OA2 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB

Table 11. SMBUS Slave Mode Register Map (continued)

0x3D	CH6 - CHA2 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE tha			Assert threshold (1010 pattern 12 Gbps) 00 = 50 mVp-p (default) 01 = 40 mVp-p 10 = 75 mVp-p 11 = 58 mVp-p Note: override the SD_TH pin.
		1:0	IDLE thd			De-assert threshold (1010 pattern 12 Gbps) 00 = 37 mVp-p (default) 01 = 22 mVp-p 10 = 55 mVp-p 11 = 45 mVp-p Note: override the SD_TH pin.
0x40	CH7 - CHA3 IDLE, RXDET	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE_AUTO			1: Automatic IDLE detect 0: Allow IDLE_SEL control in bit 4 Note: override IDLE control.
		4	IDLE_SEL			1: Output is MUTED (electrical idle) 0: Output is ON Note: override IDLE control.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved			Set bits to 0.
0x41	CH7 - CHA3 EQ	7:0	EQ Control	R/W	0x2F	IA3 EQ Control - total of 256 levels. See Table 3.
0x42	CH7 - CHA3 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE_SEL			1: PCIe Gen 1/2, 0: SAS-3 and PCIe Gen-3 Note: override the MODE pin.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OA3 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V

Table 11. SMBUS Slave Mode Register Map (continued)

0x43	CH7 - CHA3 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH7 - CHA3. 1: RX = detected 0: RX = not detected
		6:5	MODE_DET STATUS	R		Observation bit for MODE_DET CH7 - CHA3. 00: GEN1 (2.5G) 01: GEN2 (5G) 11: GEN3 (8G) Note: Only functions when Mode pin = Automatic
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OA3 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x44	CH7 - CHA3 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE tha			Assert threshold (1010 pattern 12 Gbps) 00 = 50 mVp-p (default) 01 = 40 mVp-p 10 = 75 mVp-p 11 = 58 mVp-p Note: override the SD_TH pin.
		1:0	IDLE thd			De-assert threshold (1010 pattern 12 Gbps) 00 = 37 mVp-p (default) 01 = 22 mVp-p 10 = 55 mVp-p 11 = 45 mVp-p Note: override the SD_TH pin.
0x51	Device ID	7:5	VERSION	R	0x65	011'b
		4:0	ID			00101'b

APPLICATIONS INFORMATION

GENERAL RECOMMENDATIONS

The DS125BR800A is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the information below and Revision 4 of the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

SAS-3 and PCIe Gen-3 PLACEMENT WITHIN CHANNEL

SAS-3 and PCIe Gen-3 interfaces implement a training sequence between connected Tx and Rx pairs. While the DS125BR800A circuitry is designed to be transparent for this training sequence and protocol, it is optimized for receiver equalization. This linear equalization maximizes interconnect channel extension when the DS125BR800A is placed with the majority of channel loss on the DS125BR800A input side. Adjustable transmit de-emphasis and output voltage amplitude help to compensate for the remaining channel attenuation on the output side.

When working with SAS-3 applications the maximum recommended input channel loss is -24 dB @ 6 GHz.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and outputs have been optimized to work with interconnects using a controlled differential impedance of 85 - 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on QFN (WQFN) packages.

To minimize the effects of crosstalk, a 5:1 ratio or greater should be maintained between inter-pair and intra-pair spacing.

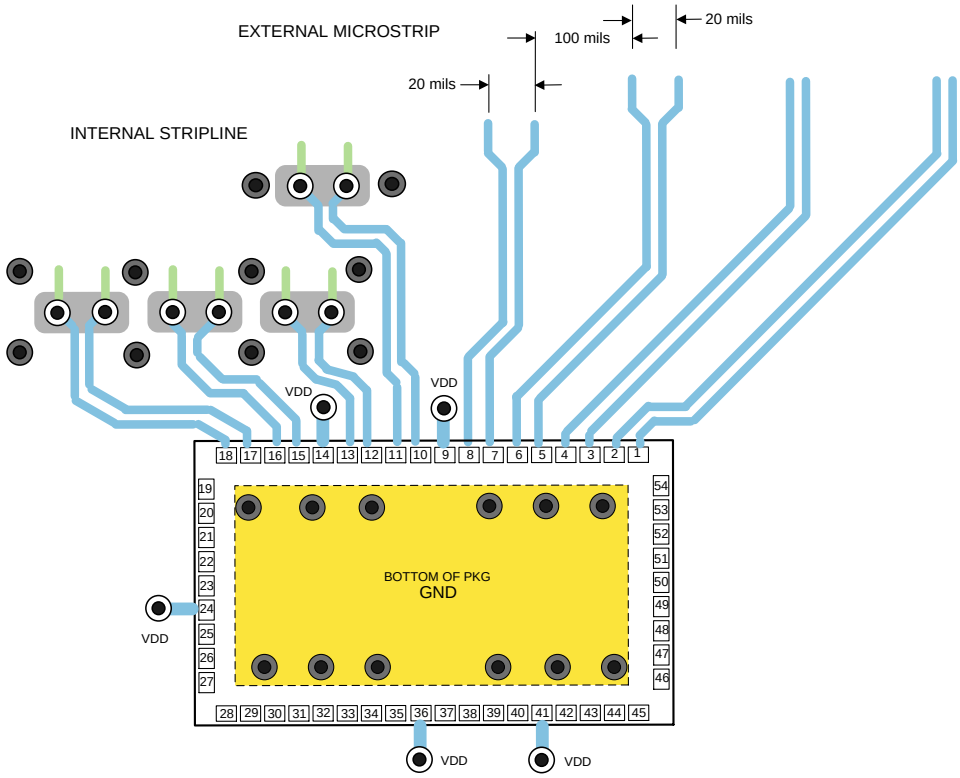


Figure 7. Typical Routing Options

Figure 7 depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the detrimental high frequency effects of stubs on the signal path.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS125BR800A is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS125BR800A. Smaller body size capacitors can help facilitate proper component placement. Additionally, capacitor with capacitance in the range of 1 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

Typical Performance Curves Characteristics

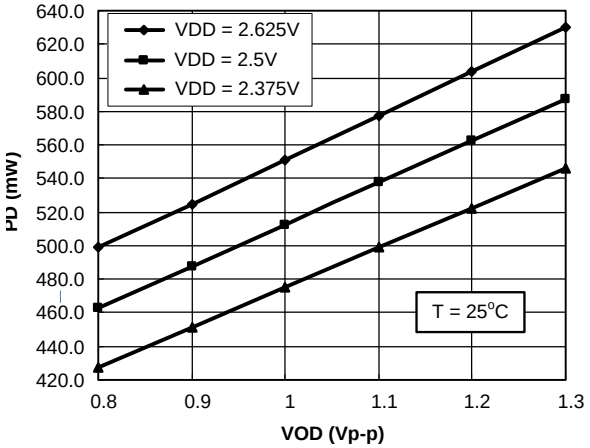


Figure 8. Power Dissipation (PD) vs. Output Differential Voltage (VOD)

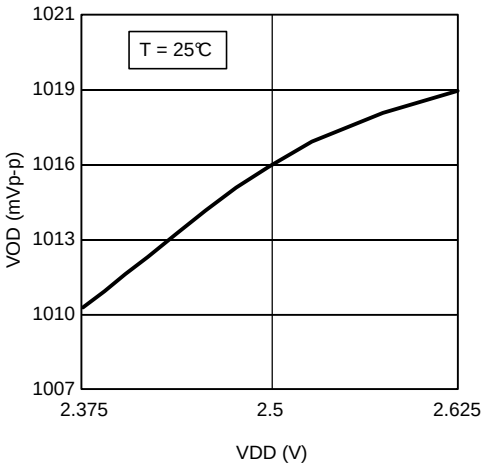


Figure 9. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Supply Voltage (VDD)

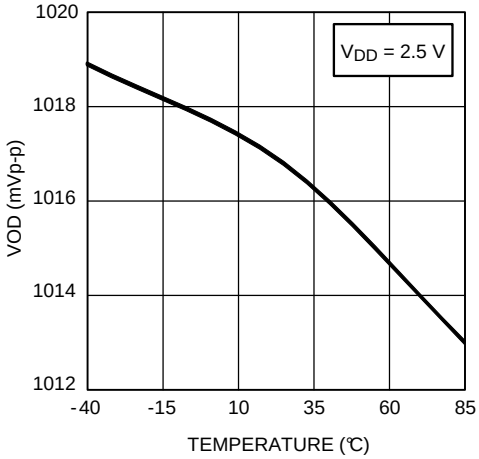


Figure 10. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Temperature

Typical Performance Eye Diagrams Characteristics

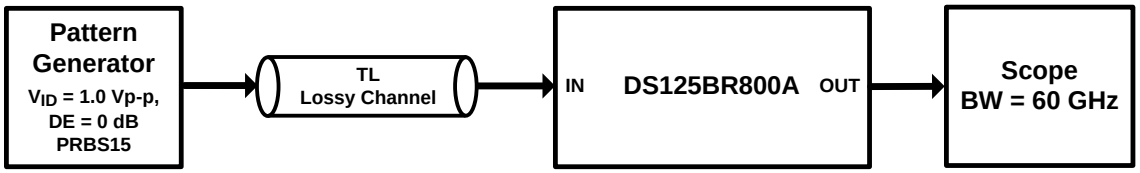


Figure 11. Test Setup Connections Diagram

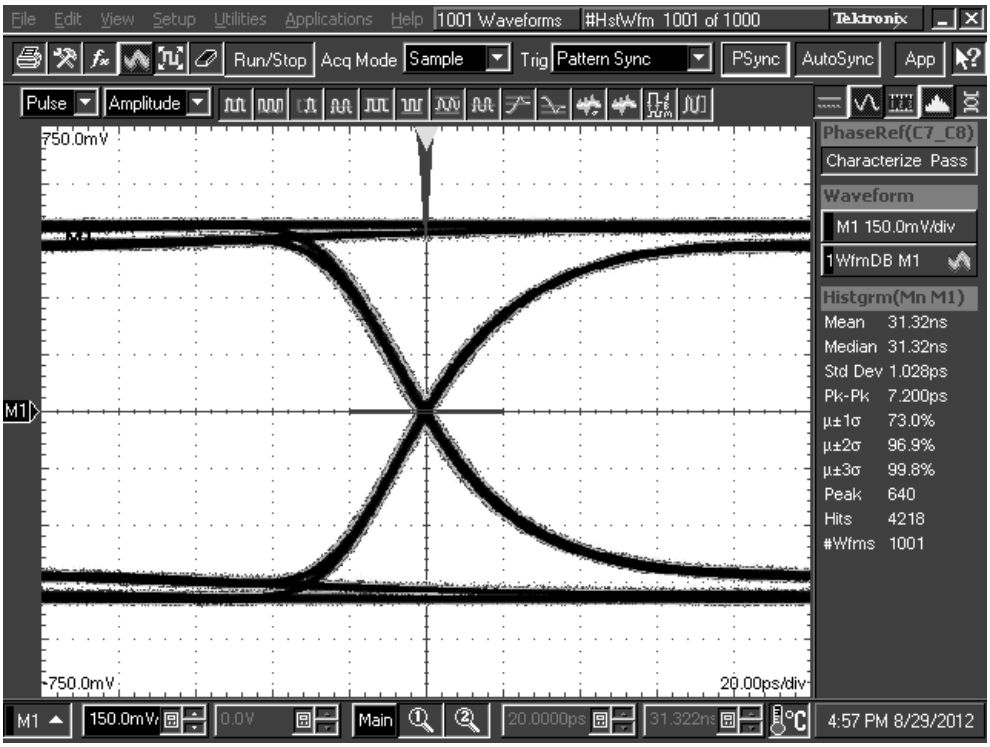


Figure 12. TL = 10 inch 5–mil FR4 trace, 5 Gbps
DS125BR800A settings: EQ[1:0] = 0, F = 02'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

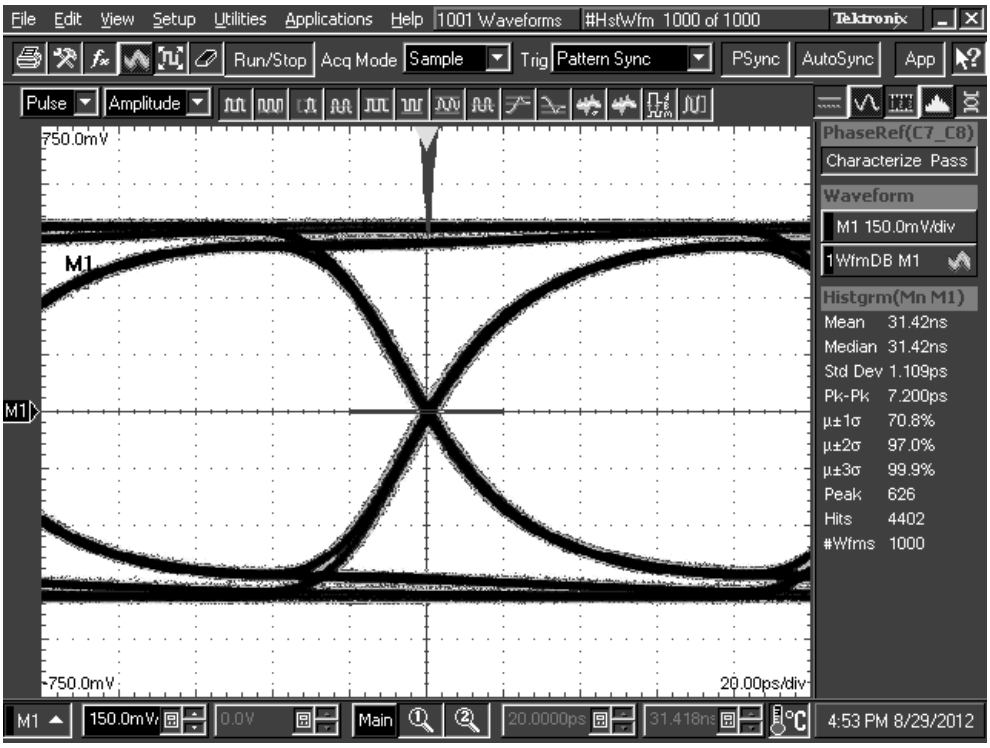


Figure 13. TL = 10 inch 5–mil FR4 trace, 8 Gbps
DS125BR800A settings: EQ[1:0] = 0, F = 02'h, DEM[1:0] = 0, 1

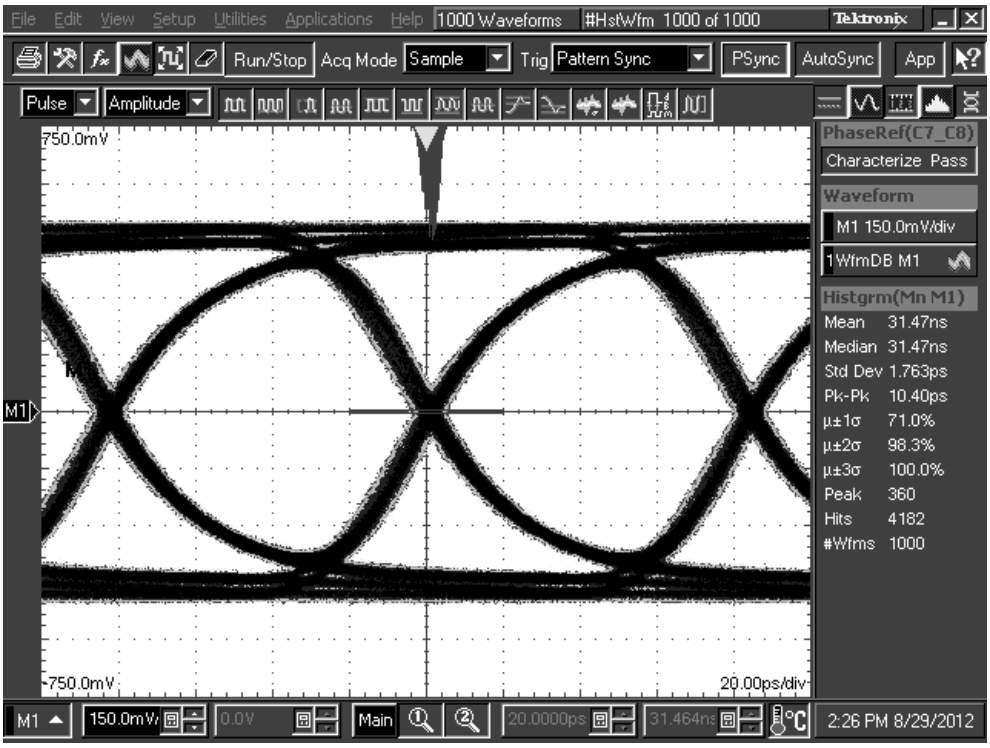


Figure 14. TL = 10 inch 5–mil FR4 trace, 12 Gbps
DS125BR800A settings: EQ[1:0] = 0, R = 01'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

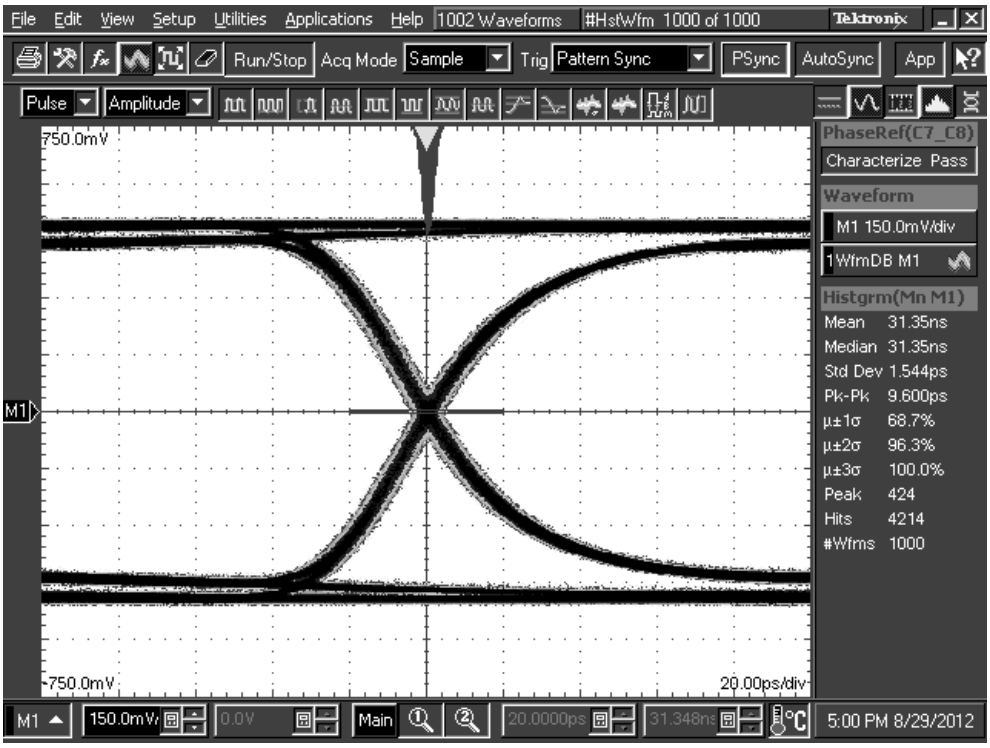


Figure 15. TL = 20 inch 5–mil FR4 trace, 5 Gbps
DS125BR800A settings: EQ[1:0] = 0, 1 = 03'h, DEM[1:0] = 0, 1

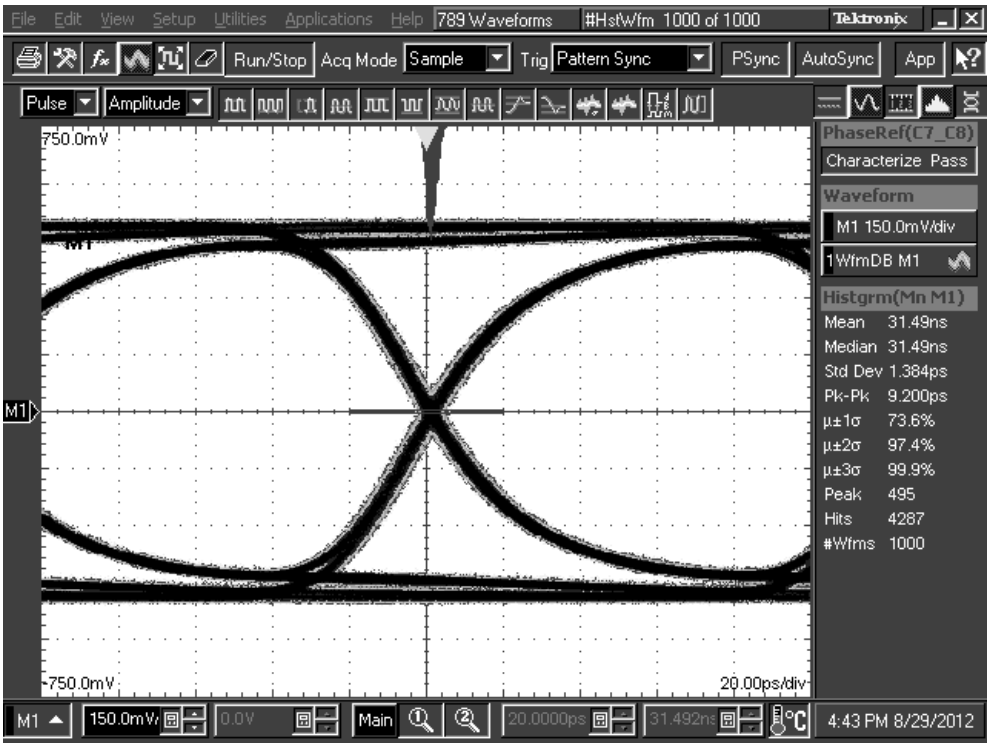


Figure 16. TL = 20 inch 5–mil FR4 trace, 8 Gbps
DS125BR800A settings: EQ[1:0] = 0, 1 = 03'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

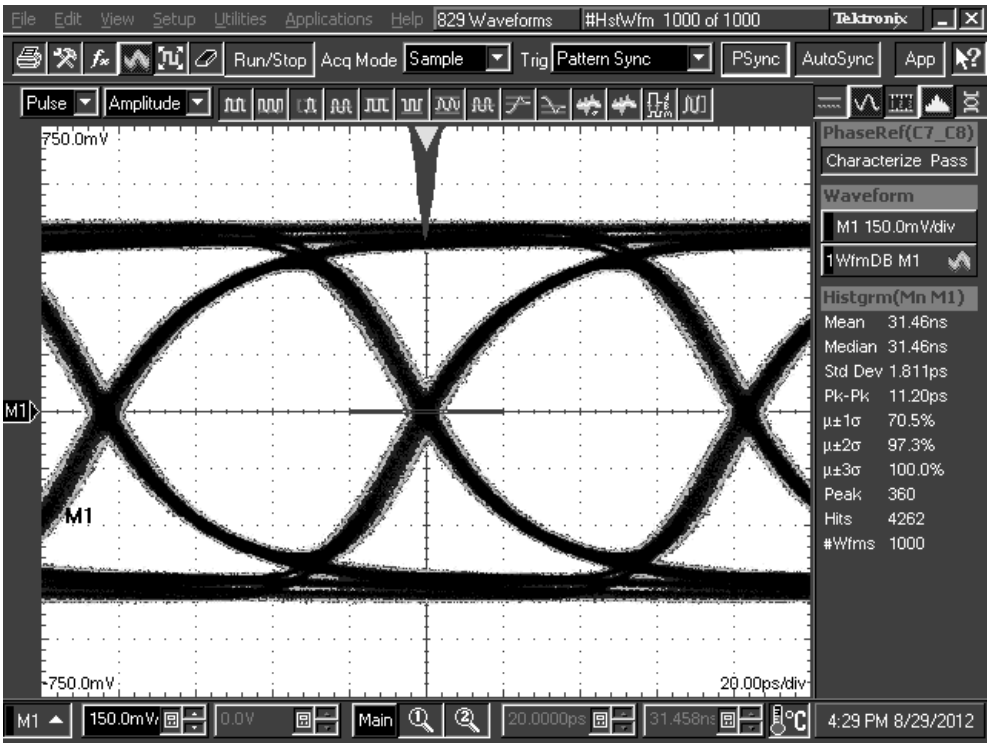


Figure 17. TL = 20 inch 5–mil FR4 trace, 12 Gbps
DS125BR800A settings: EQ[1:0] = 0, 1 = 03'h, DEM[1:0] = 0, 1

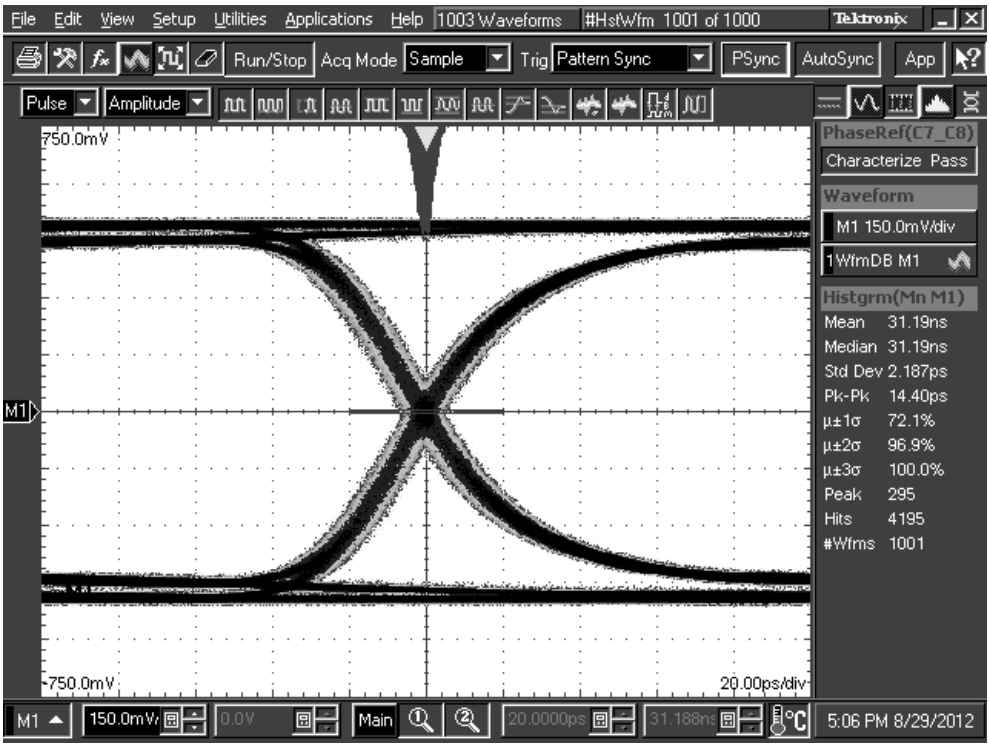


Figure 18. TL = 30 inch 5–mil FR4 trace, 5 Gbps
DS125BR800A settings: EQ[1:0] = R, 0 = 07'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

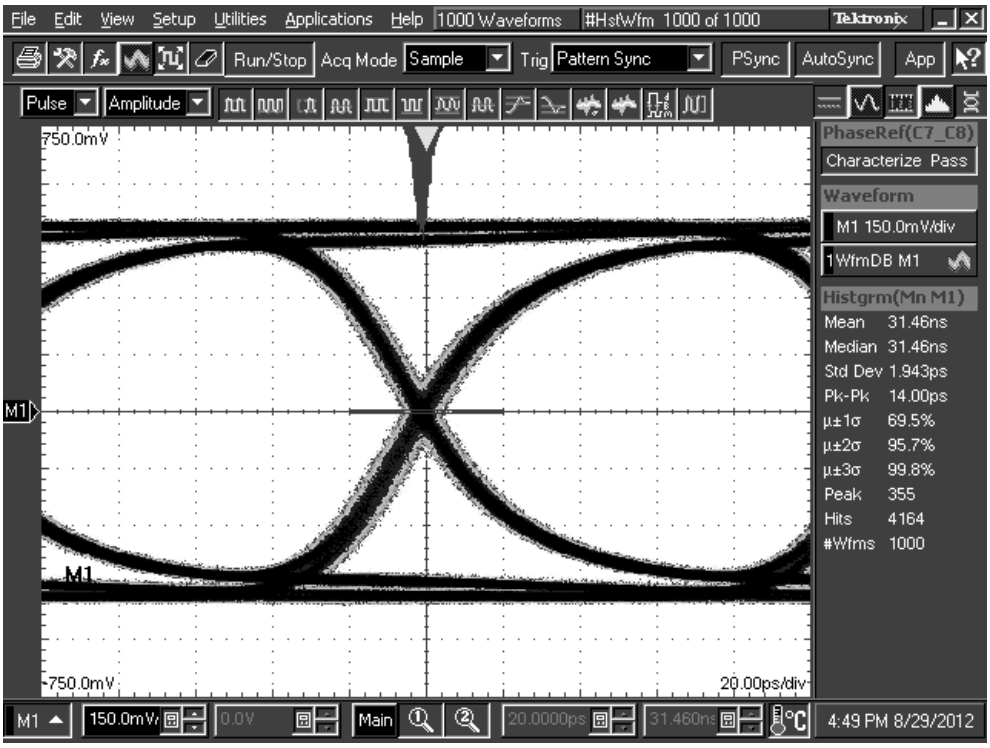


Figure 19. TL = 30 inch 5–mil FR4 trace, 8 Gbps
DS125BR800A settings: EQ[1:0] = R, 0 = 07'h, DEM[1:0] = 0, 1

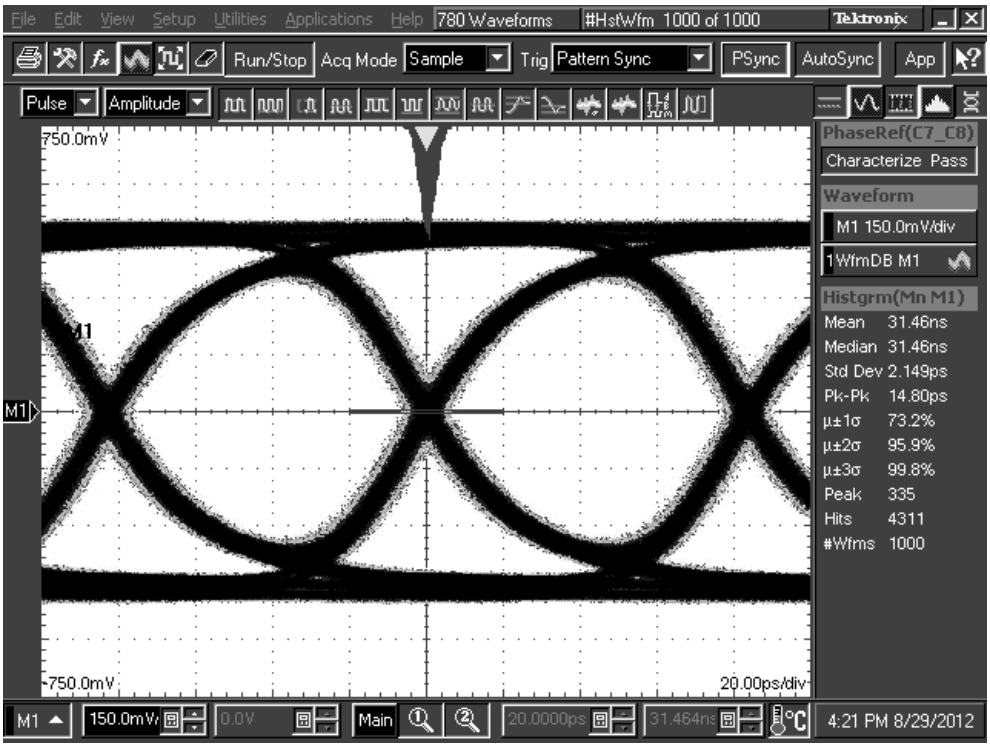


Figure 20. TL = 30 inch 5–mil FR4 trace, 12 Gbps
DS125BR800A settings: EQ[1:0] = R, 0 = 07'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

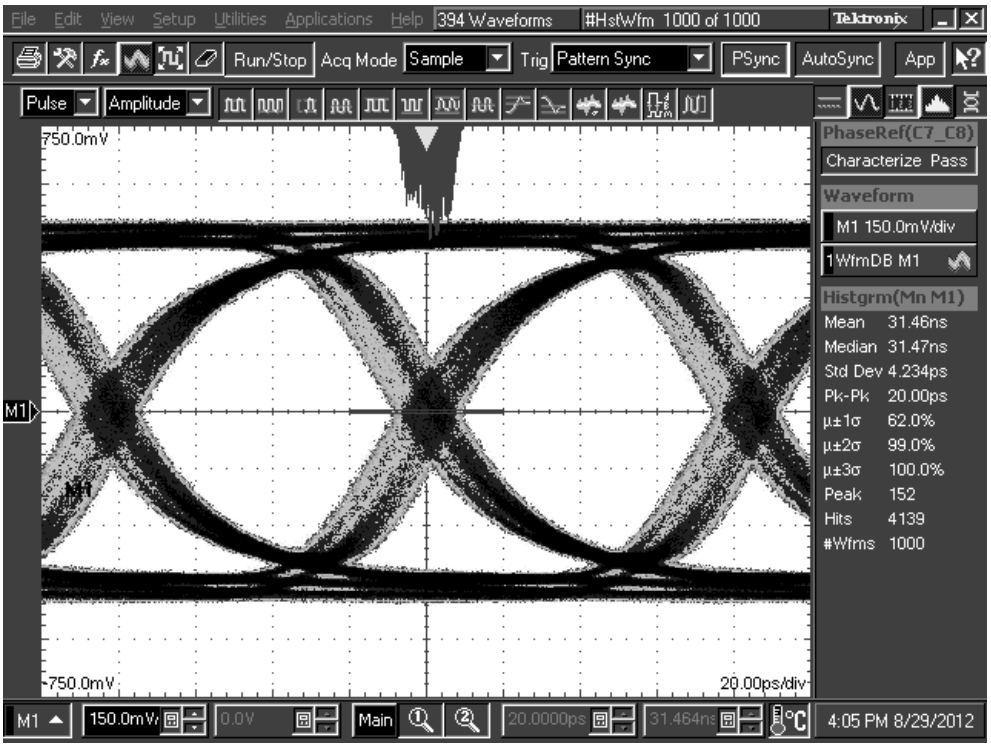


Figure 21. TL1 = 5-meter 30-AWG 100 Ohm Twin-axial Cable, 12 Gbps
DS125BR800A settings: EQ[1:0] = R, 0 = 07'h, DEM[1:0] = 0, 1

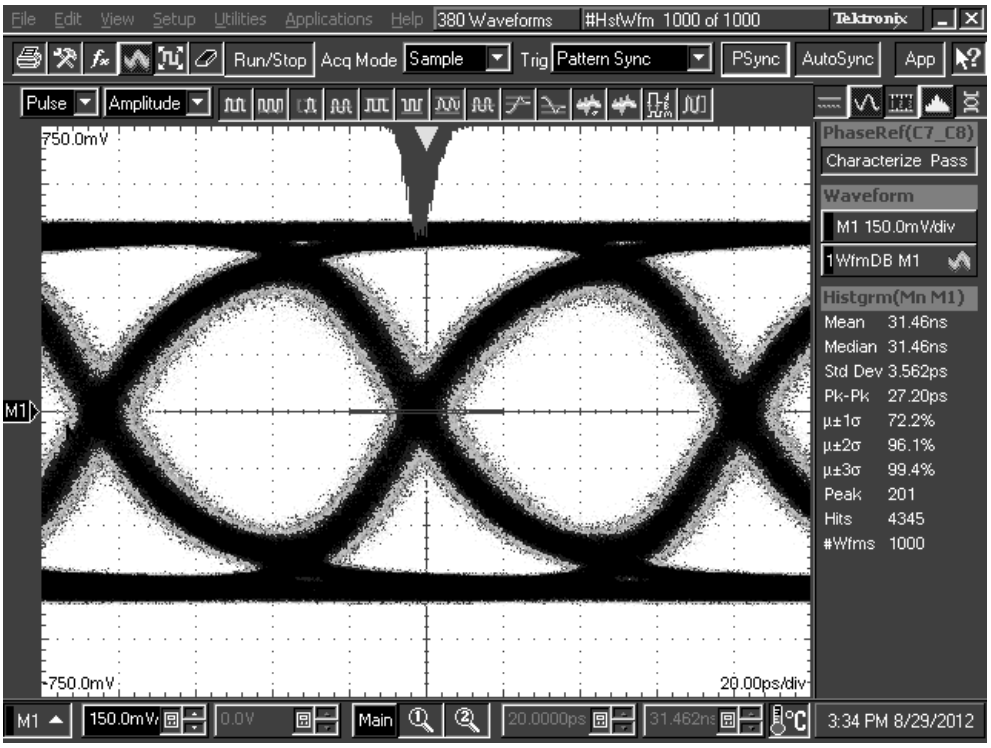


Figure 22. TL1 = 8-meter 30-AWG 100 Ohm Twin-axial Cable, 12 Gbps
DS125BR800A settings: EQ[1:0] = R, 1 = 0F'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

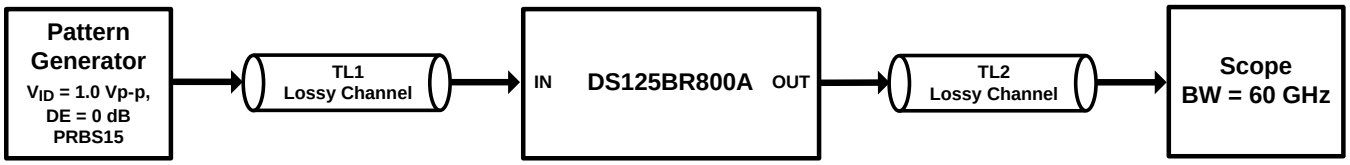


Figure 23. Test Setup Connections Diagram

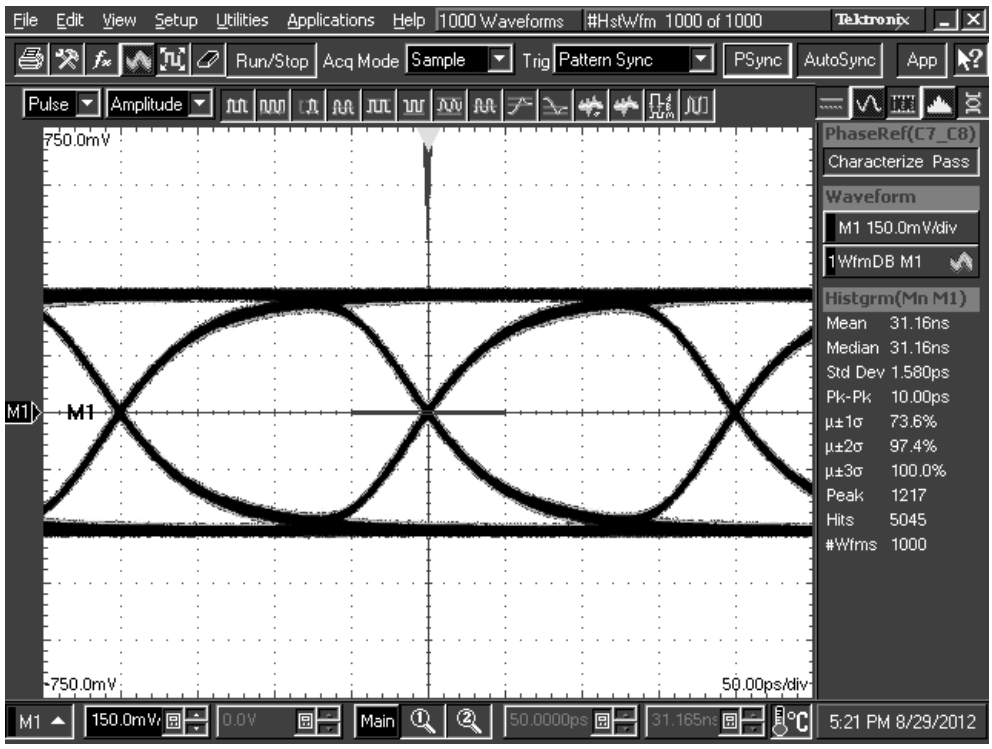


Figure 24. TL1 = 20 inch 5–mil FR4 trace, TL2 = 10 inch 5–mil FR4 trace, 5 Gbps DS125BR800A settings: EQ[1:0] = 0, 1 = 03'h, DEM[1:0] = R, 0

Typical Performance Eye Diagrams Characteristics (continued)

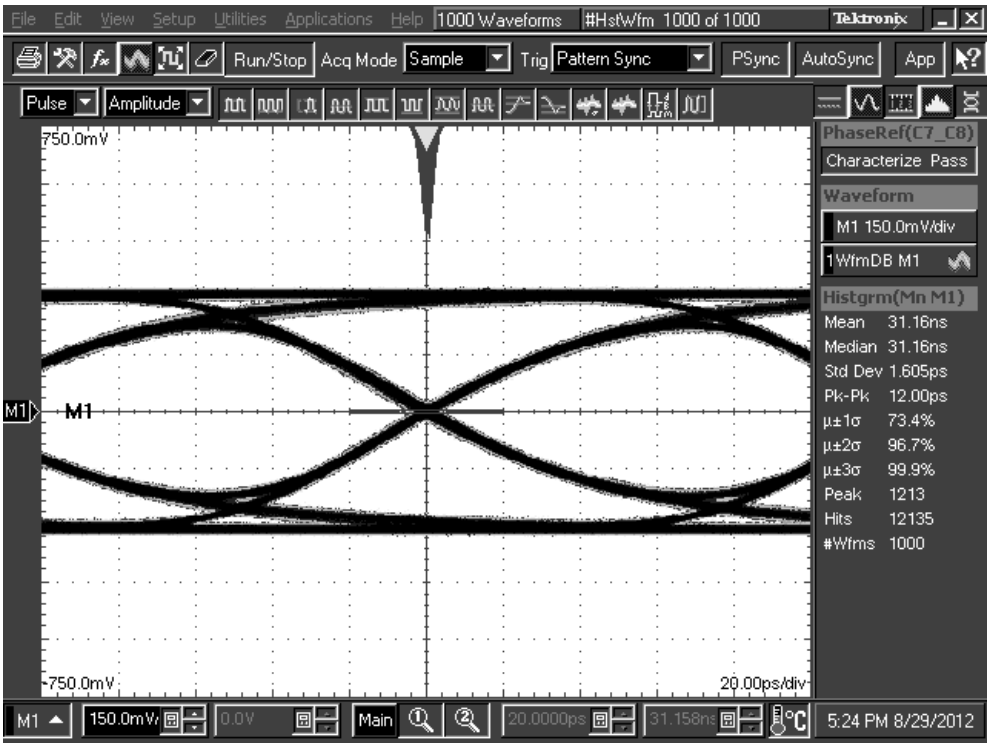


Figure 25. TL1 = 20 inch 5–mil FR4 trace, TL2 = 10 inch 5–mil FR4 trace, 8 Gbps DS125BR800A settings: EQ[1:0] = R, 1 = 03'h, DEM[1:0] = R, 0

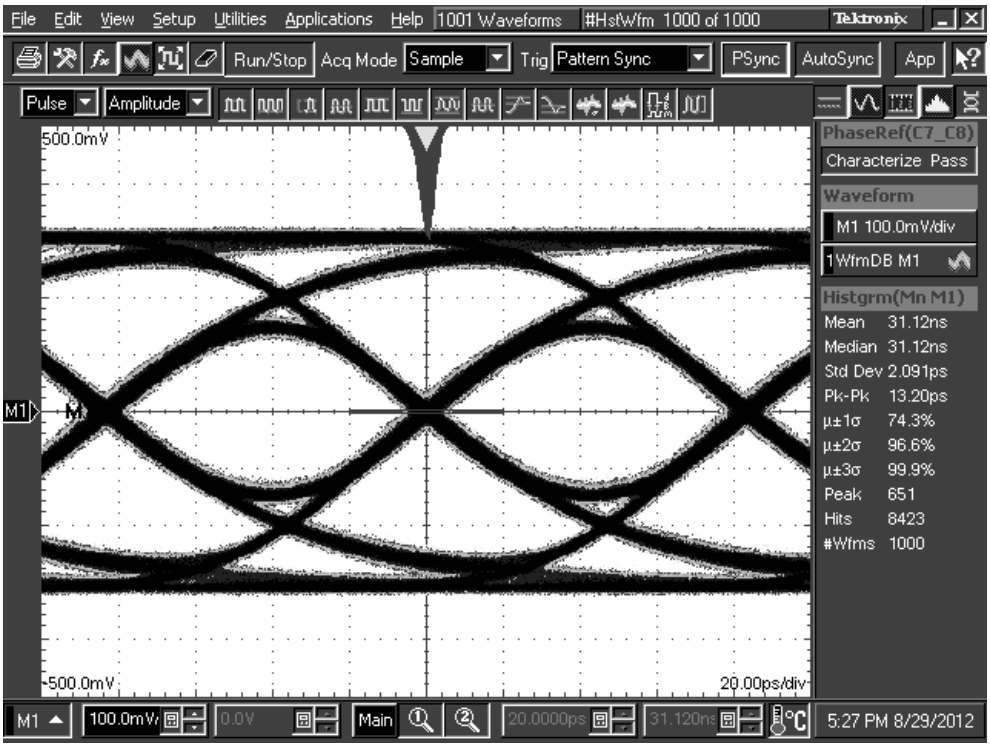


Figure 26. TL1 = 20 inch 5–mil FR4 trace, TL2 = 10 inch 5–mil FR4 trace, 12 Gbps DS125BR800A settings: EQ[1:0] = R, 1 = 03'h, DEM[1:0] = R, 0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS125BR800ANJYR	ACTIVE	WQFN	NJY	54	2000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS125BR800A	Samples
DS125BR800ANJYT	ACTIVE	WQFN	NJY	54	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS125BR800A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

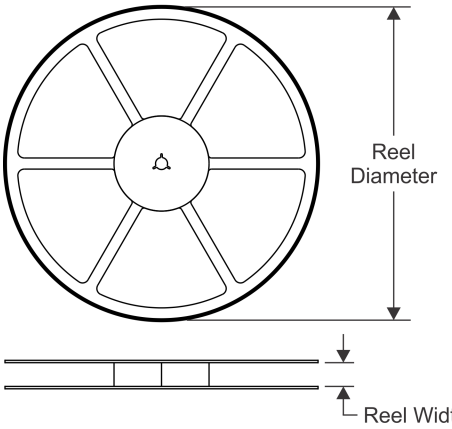
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

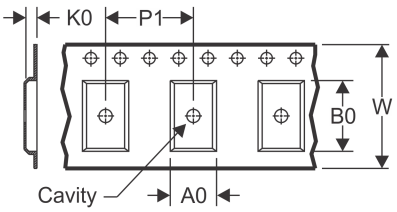
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

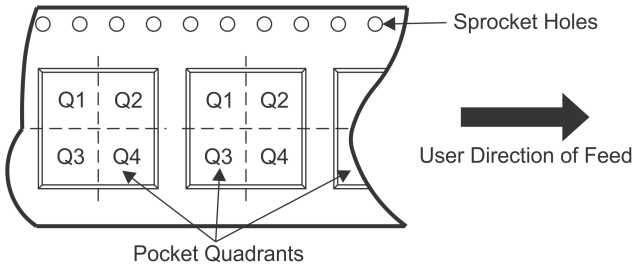


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

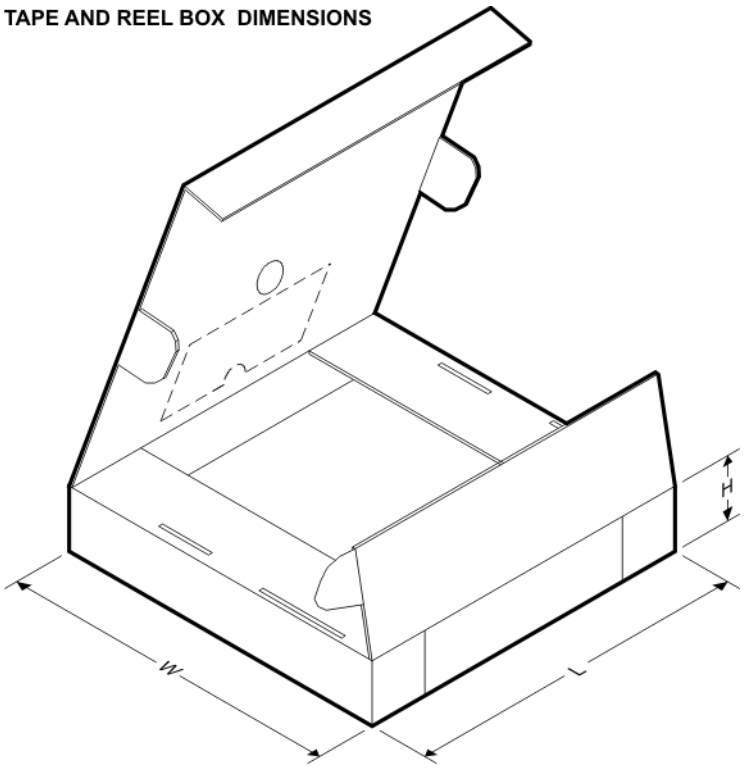
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

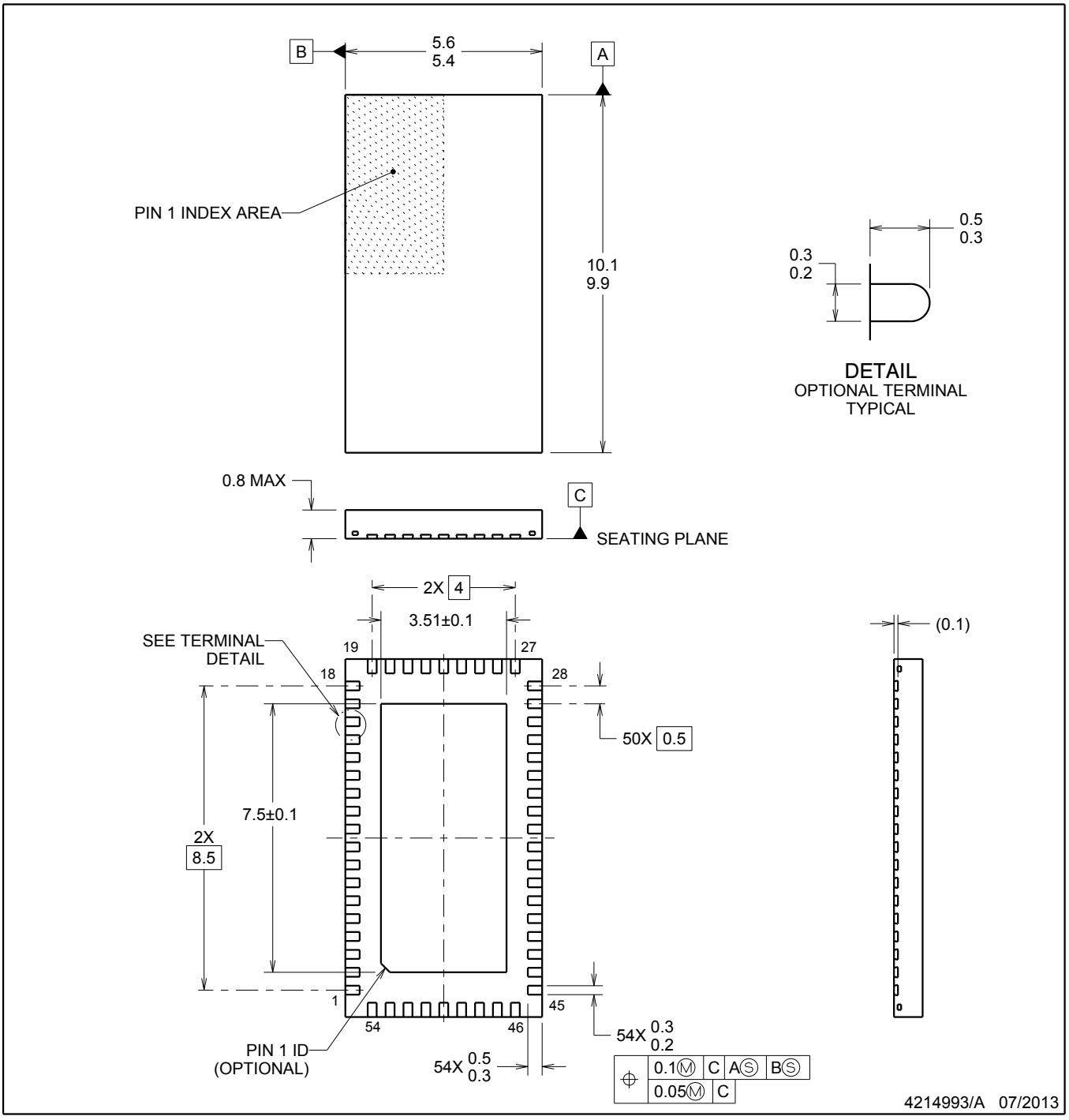
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS125BR800ANJYR	WQFN	NJY	54	2000	330.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1
DS125BR800ANJYT	WQFN	NJY	54	250	178.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



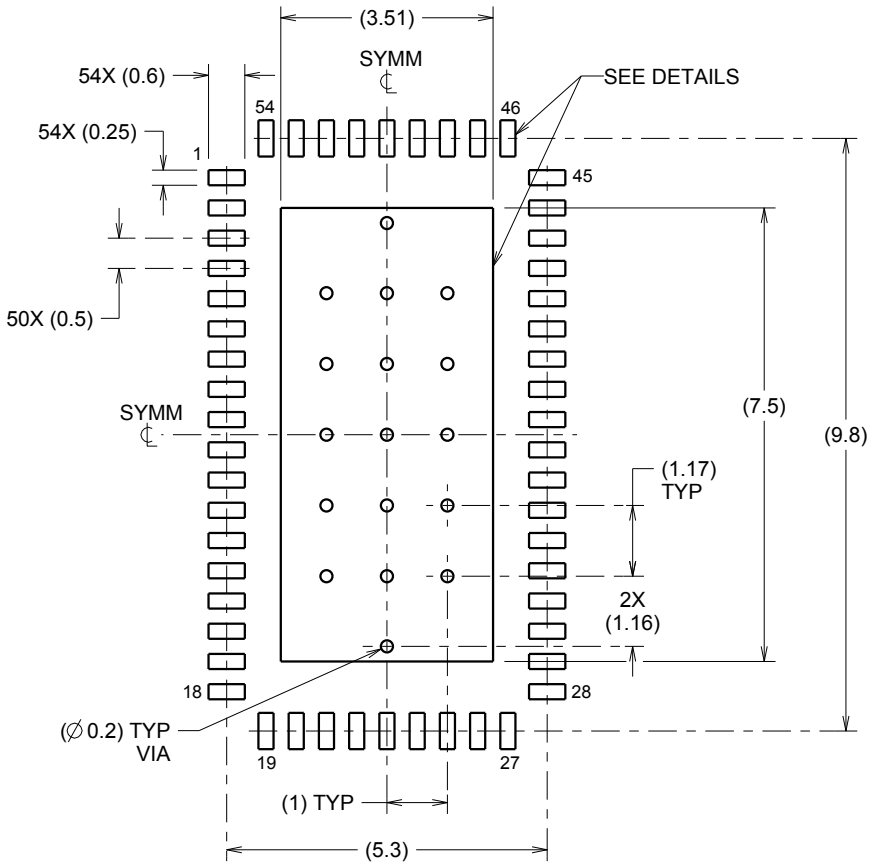
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS125BR800ANJYR	WQFN	NJY	54	2000	367.0	367.0	38.0
DS125BR800ANJYT	WQFN	NJY	54	250	210.0	185.0	35.0

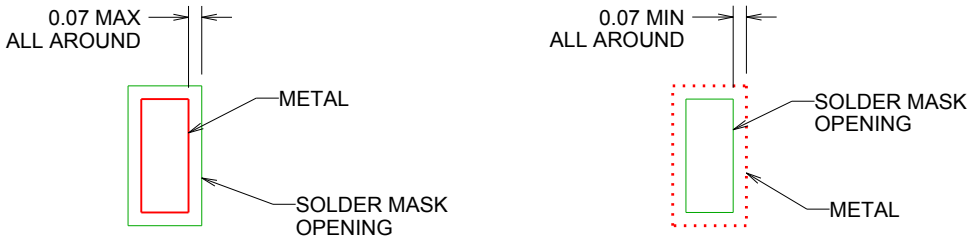


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED
(PREFERRED)

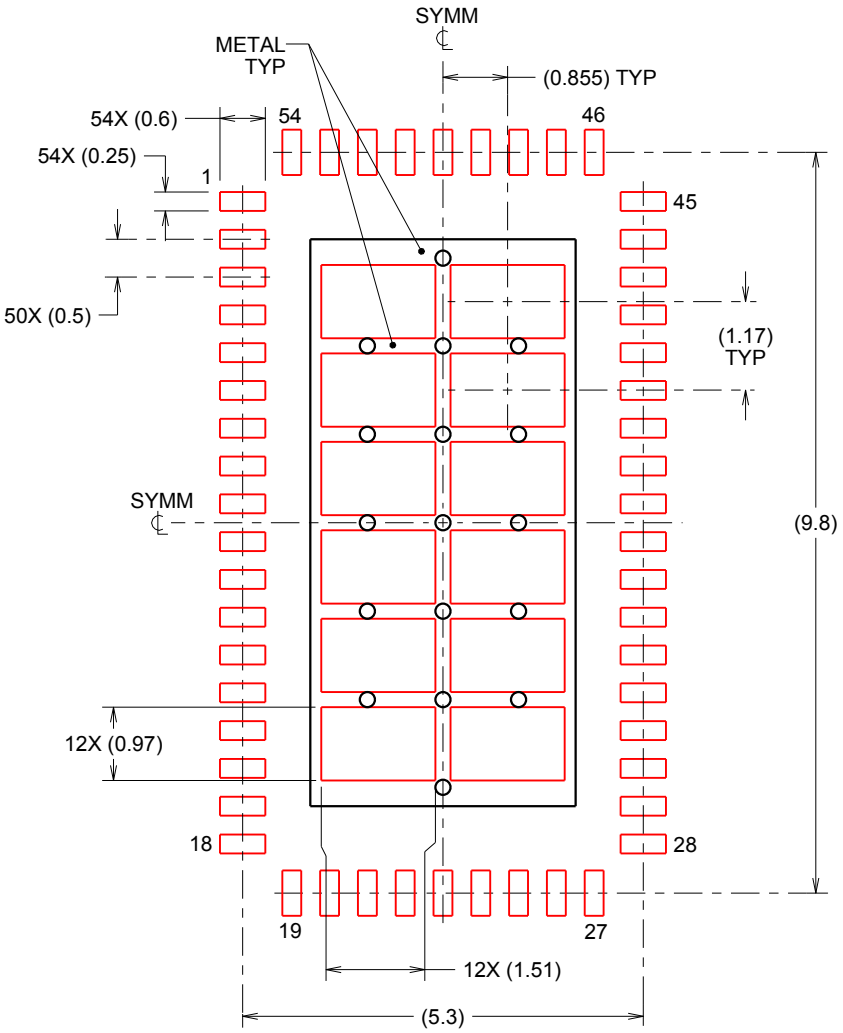
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214993/A 07/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4214993/A 07/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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