

# TLE4964-6M

High Precision Automotive Hall Effect Switch

## Data Sheet

Revision 1.0, 2013-07-05

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## Revision History

| Page or Item | Subjects (major changes since previous revision) |
|--------------|--------------------------------------------------|
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Revision 1.0, 2013-07-05

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# 1 Product Description



## 1.1 Overview

| Characteristic              | Supply Voltage | Supply Current | Sensitivity                                                | Interface         | Temperature    |
|-----------------------------|----------------|----------------|------------------------------------------------------------|-------------------|----------------|
| Unipolar Hall Effect Switch | 3.0~32 V       | 1.6 mA         | High<br>B <sub>OP</sub> :3.5 mT<br>B <sub>RP</sub> :2.5 mT | Open Drain Output | -40°C to 170°C |



**Figure 1-1** Image of TLE4964-6M in the PG-SOT23-3-15 Package

## 1.2 Features

- 3.0 V to 32 V operating supply voltage
- Operation from unregulated power supply
- Reverse polarity protection (-18 V)
- Overvoltage capability up to 42 V without external resistor
- Output overcurrent & overtemperature protection
- Active error compensation
- High stability of magnetic thresholds
- Low jitter (typ. 0.35 µs)
- High ESD performance
- Small SMD package PG-SOT23-3-15 (TLE4964-6M)

## 1.3 Target Applications

Target applications for the TLE496x Hall switch family are all applications which require a high precision Hall Switch with an operating temperature range from -40°C to 170°C. Its superior supply voltage range from 3.0 V to 32 V with overvoltage capability (e.g. load-dump) up to 42 V without external resistor makes it ideally suited for automotive and industrial applications.

**Table 1-1** Ordering Information

| Product Name | Product Type         | Ordering Code | Package       |
|--------------|----------------------|---------------|---------------|
| TLE4964-6M   | Unipolar Hall Switch | SP001042418   | PG-SOT23-3-15 |



## 2 Functional Description

### 2.1 General

The TLE4964-6M is an integrated Hall effect designed specifically for highly accurate applications with superior supply voltage capability, operating temperature range and temperature stability of the magnetic thresholds.

### 2.2 Pin Configuration (top view)

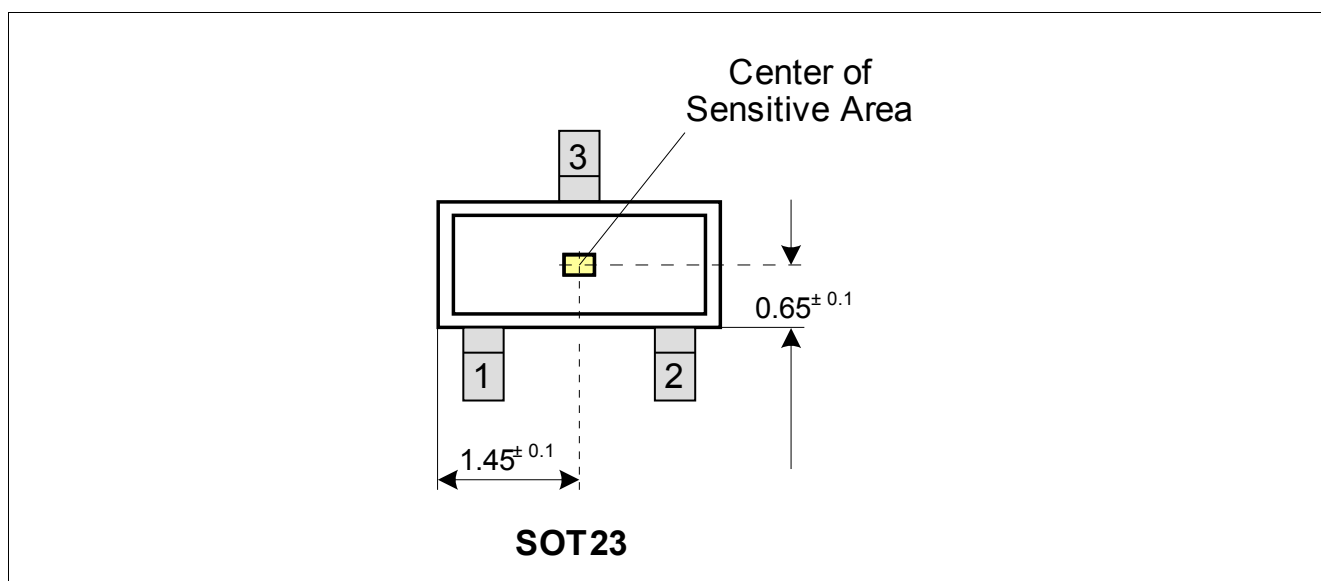


Figure 2-1 Pin Configuration and Center of Sensitive Area

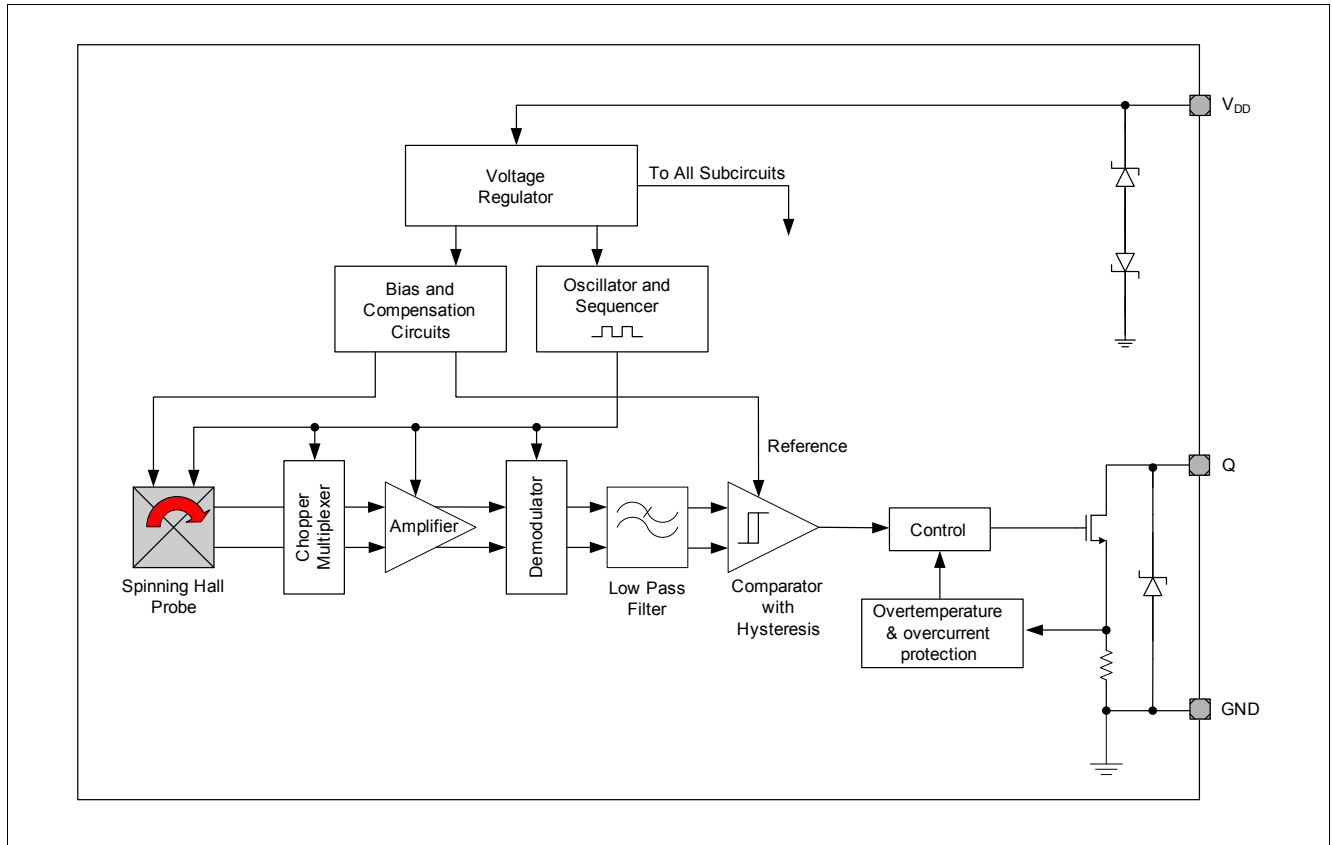
### 2.3 Pin Description

Table 2-1 Pin Description PG-SOT23-3-15

| Pin No. | Symbol | Function       |
|---------|--------|----------------|
| 1       | VDD    | Supply voltage |
| 2       | Q      | Output         |
| 3       | GND    | Ground         |



## 2.4 Block Diagram



**Figure 2-2 Functional Block Diagram TLE4964-6M**

## 2.5 Functional Block Description

The chopped Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensation (chopping technique) rejects offsets in the signal path and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stress in the package. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds.

The output transistor has an integrated overcurrent and overtemperature protection.

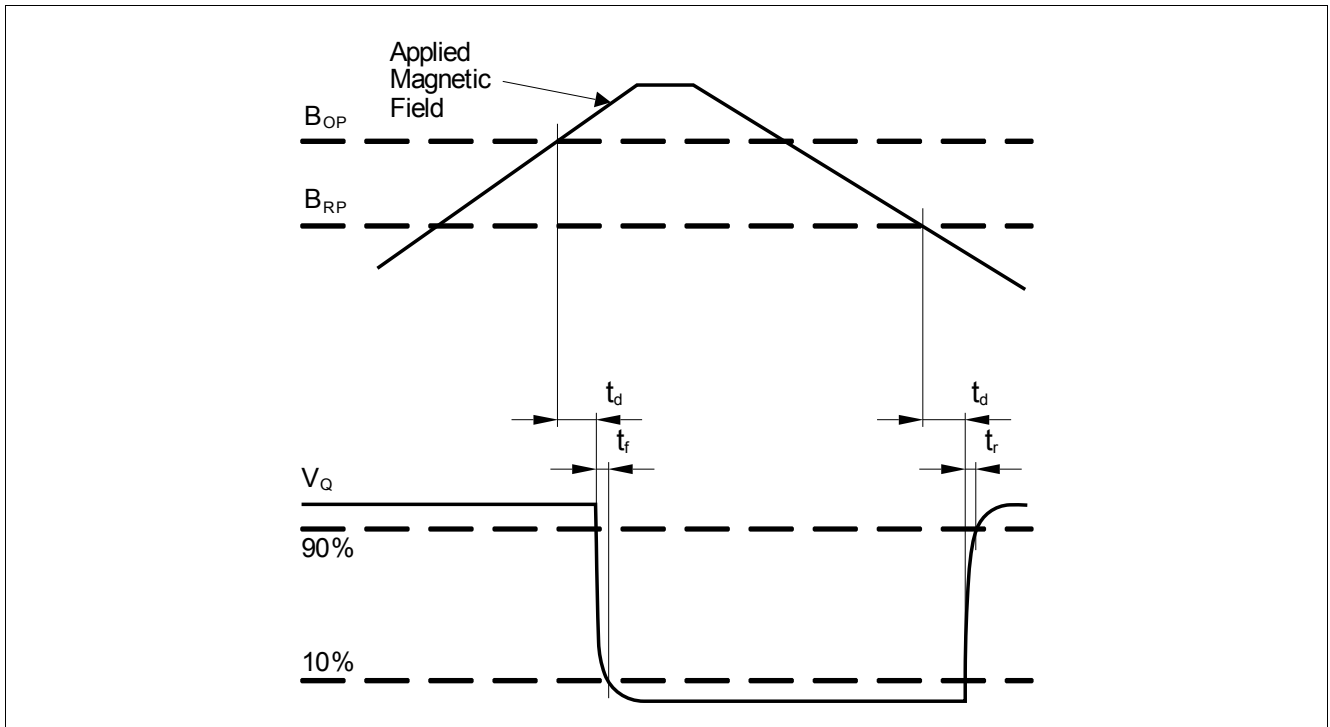


Figure 2-3 Timing Diagram TLE4964-6M

## 2.6 Default Start-up Behavior

The magnetic thresholds exhibit a hysteresis  $B_{HYS} = B_{OP} - B_{RP}$ . In case of a power-on with a magnetic field  $B$  within hysteresis ( $B_{OP} > B > B_{RP}$ ) the output of the sensor is set to the pull up voltage level ( $V_Q$ ) per default. After the first crossing of  $B_{OP}$  or  $B_{RP}$  of the magnetic field the internal decision logic is set to the corresponding magnetic input value.

$V_{DDA}$  is the internal supply voltage which is following the external supply voltage  $V_{DD}$ .

This means for  $B > B_{OP}$  the output is switching, for  $B < B_{RP}$  and  $B_{OP} > B > B_{RP}$  the output stays at  $V_Q$ .

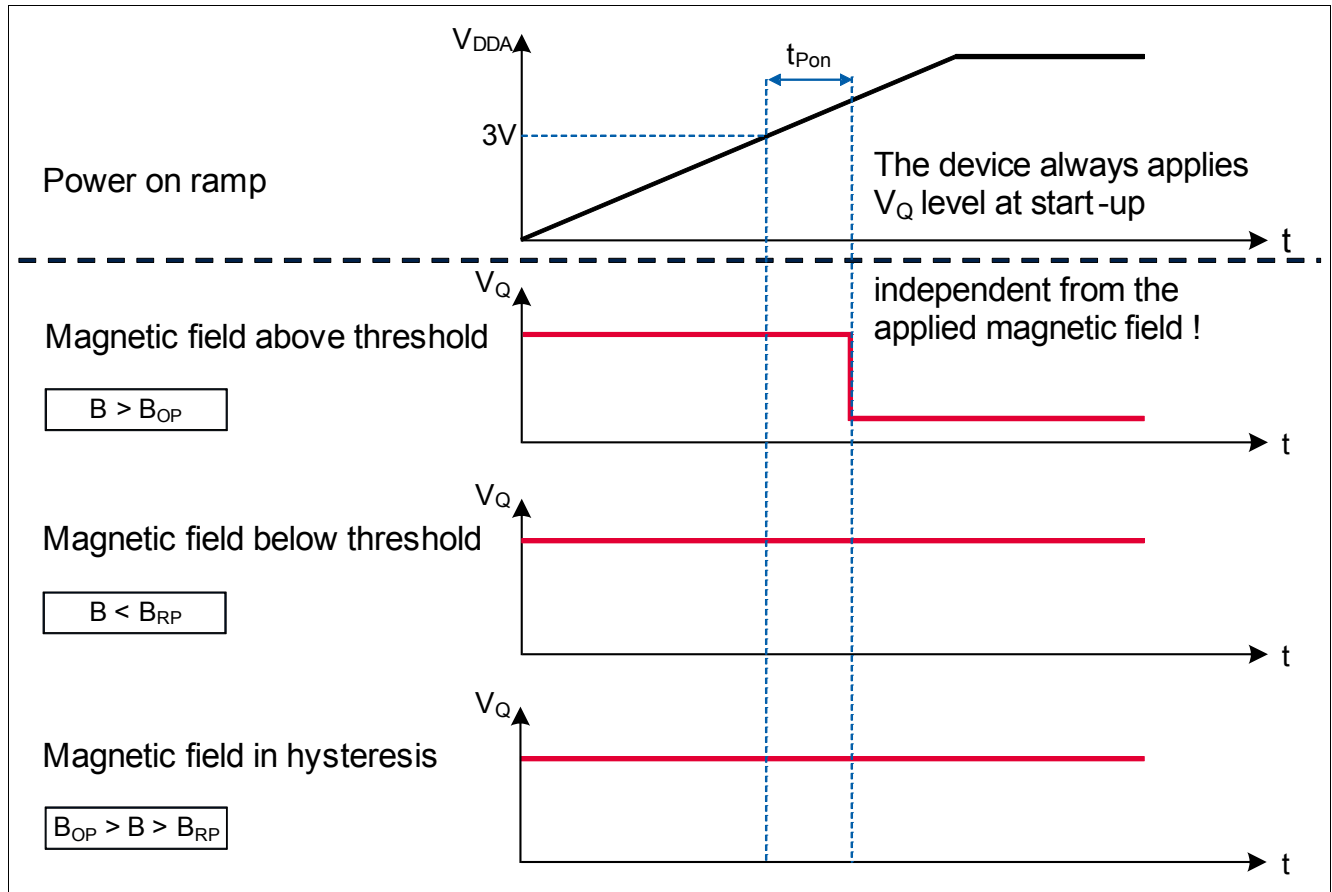


Figure 2-4 Illustration of the Start-up Behavior of the TLE4964-6M

### 3 Specification

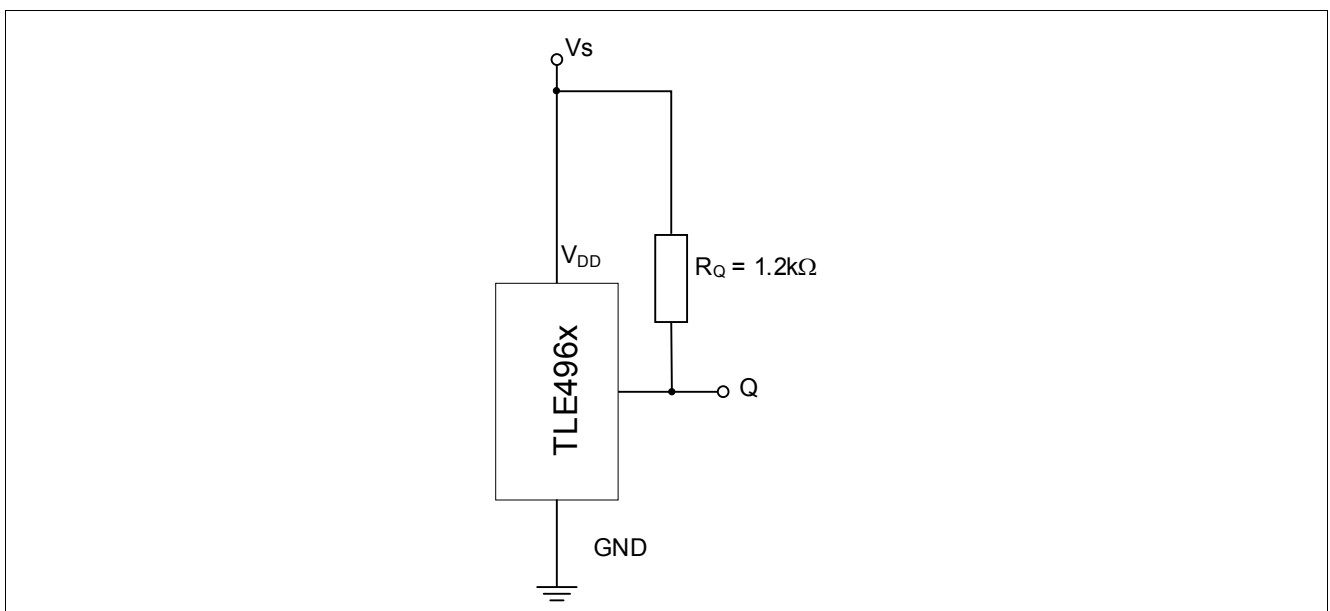
#### 3.1 Application Circuit

The following **Figure 3-1** shows the basic option of an application circuit. Only a pull-up resistor  $R_Q$  is necessary. An external series resistor for  $V_S$  is not needed. The resistor  $R_Q$  has to be in a dimension to match the applied  $V_S$  to keep  $I_Q$  limited to the operating range of maximum 25 mA.

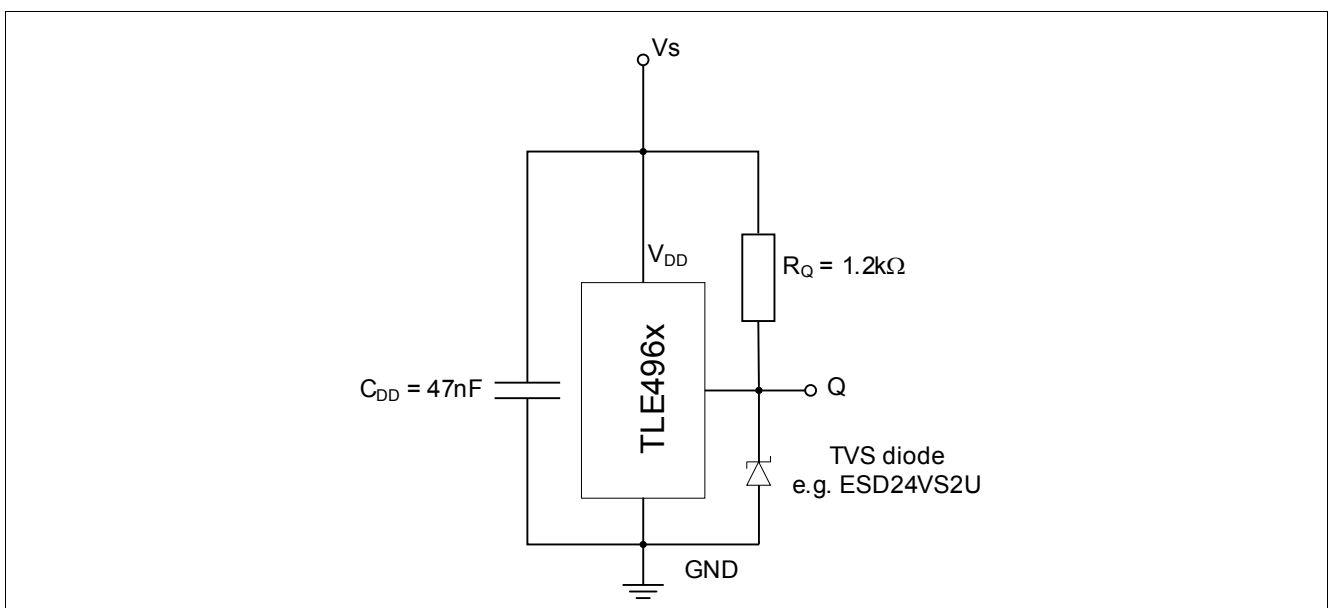
e.g.:

$$V_S = 12 \text{ V}$$

$$I_Q = 12 \text{ V} / 1200 \text{ } \Omega = 10 \text{ mA}$$



**Figure 3-1 Application Circuit #1: Only Pull-Up Resistor is necessary**



**Figure 3-2 Application Circuit #2 for extended ESD robustness**

## 3.2 Absolute Maximum Ratings

**Table 3-1 Absolute Maximum Rating Parameters**

| Parameter                              | Symbol            | Values |      |                          | Unit | Note / Test Condition                                                                                    |
|----------------------------------------|-------------------|--------|------|--------------------------|------|----------------------------------------------------------------------------------------------------------|
|                                        |                   | Min.   | Typ. | Max.                     |      |                                                                                                          |
| Supply voltage <sup>1)</sup>           | V <sub>DD</sub>   | -18    |      | 32<br>42                 | V    | 10h, no external resistor required                                                                       |
| Output voltage                         | V <sub>Q</sub>    | -0.5   |      | 32                       | V    |                                                                                                          |
| Reverse output current                 | I <sub>Q</sub>    | -70    |      |                          | mA   |                                                                                                          |
| Junction temperature <sup>1)</sup>     | T <sub>J</sub>    | -40    |      | 155<br>165<br>175<br>195 | °C   | for 2000h (not additive)<br>for 1000h (not additive)<br>for 168h (not additive)<br>for 3 x 1h (additive) |
| Storage temperature                    | T <sub>S</sub>    | -40    |      | 150                      | °C   |                                                                                                          |
| Thermal resistance<br>Junction ambient | R <sub>thJA</sub> |        |      | 300                      | K/W  | for PG-SOT23-3-15 (2s2p)                                                                                 |
| Thermal resistance<br>Junction lead    | R <sub>thJL</sub> |        |      | 100                      | K/W  | for PG-SOT23-3-15                                                                                        |

1) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

**Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

Calculation of the dissipated power P<sub>DIS</sub> and junction temperature T<sub>J</sub> of the chip (SOT23 example):

e.g. for: V<sub>DD</sub> = 12 V, I<sub>S</sub> = 2.5 mA, V<sub>QSAT</sub> = 0.5 V, I<sub>Q</sub> = 20 mA

Power dissipation: P<sub>DIS</sub> = 12 V x 2.5 mA + 0.5 V x 20 mA = 30 mW + 10 mW = 40 mW

Temperature ΔT = R<sub>thJA</sub> x P<sub>DIS</sub> = 300 K/W x 40 mW = 12 K

For T<sub>A</sub> = 150 °C: T<sub>J</sub> = T<sub>A</sub> + ΔT = 150 °C + 12 K = 162 °C

**Table 3-2 ESD Protection<sup>1)</sup> (TA = 25°C)**

| Parameter                                | Symbol           | Values |      |      | Unit | Note / Test Condition                            |
|------------------------------------------|------------------|--------|------|------|------|--------------------------------------------------|
|                                          |                  | Min.   | Typ. | Max. |      |                                                  |
| ESD voltage (HBM) <sup>2)</sup>          | V <sub>ESD</sub> | -7     |      | 7    | kV   | R = 1.5 kΩ, C = 100 pF                           |
| ESD voltage (CDM) <sup>3)</sup>          |                  | -1     |      | 1    |      |                                                  |
| ESD voltage (system level) <sup>4)</sup> |                  | -15    |      | 15   |      | with circuit shown in <a href="#">Figure 3-2</a> |

1) Characterization of ESD is carried out on a sample basis, not subject to production test.

2) Human Body Model (HBM) tests according to ANSI/ESDA/JEDEC JS-001.

3) Charge device model (CDM) tests according to JESD22-C101.

4) Gun test (2kΩ / 330pF or 330Ω / 150pF) according to ISO 10605-2008.

### 3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4964-6M. All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

**Table 3-3 Operating Conditions Parameters**

| Parameter                                     | Symbol   | Values |      |                  | Unit | Note / Test Condition |
|-----------------------------------------------|----------|--------|------|------------------|------|-----------------------|
|                                               |          | Min.   | Typ. | Max.             |      |                       |
| Supply voltage                                | $V_{DD}$ | 3.0    |      | 32 <sup>1)</sup> | V    |                       |
| Output voltage                                | $V_Q$    | -0.3   |      | 32               | V    |                       |
| Junction temperature                          | $T_j$    | -40    |      | 170              | °C   |                       |
| Output current                                | $I_Q$    | 0      |      | 25               | mA   |                       |
| Magnetic signal input frequency <sup>2)</sup> | $f_{SW}$ | 0      |      | 10               | kHz  |                       |

1) Latch-up test with factor 1.5 is not covered. Please see max ratings also.

2) For operation at the maximum switching frequency the magnetic input signal must be 1.4 times higher than for static fields. This is due to the -3dB corner frequency of the internal low-pass filter in the signal path.

### 3.4 Electrical and Magnetic Characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production and correspond to  $V_{DD} = 12\text{ V}$  and  $T_A = 25^\circ\text{C}$ . The below listed specification is valid in combination with the application circuit shown in [Figure 3-1](#) and [Figure 3-2](#)

**Table 3-4 General Electrical Characteristics**

| Parameter                       | Symbol       | Values |      |      | Unit          | Note / Test Condition                                                                      |
|---------------------------------|--------------|--------|------|------|---------------|--------------------------------------------------------------------------------------------|
|                                 |              | Min.   | Typ. | Max. |               |                                                                                            |
| Supply current                  | $I_S$        | 1.1    | 1.6  | 2.5  | mA            |                                                                                            |
| Reverse current                 | $I_{SR}$     |        | 0.05 | 1    | mA            | for $V_{DD} = -18\text{ V}$                                                                |
| Output saturation voltage       | $V_{QSAT}$   |        | 0.2  | 0.5  | V             | $I_Q = 20\text{ mA}$                                                                       |
|                                 |              |        | 0.24 | 0.6  | V             | $I_Q = 25\text{ mA}$                                                                       |
| Output leakage current          | $I_{QLEAK}$  |        |      | 10   | $\mu\text{A}$ |                                                                                            |
| Output current limitation       | $I_{QLIMIT}$ | 30     | 56   | 70   | mA            | internally limited & thermal shutdown                                                      |
| Output fall time <sup>1)</sup>  | $t_f$        | 0.17   | 0.4  | 1    | $\mu\text{s}$ | 1.2 k $\Omega$ / 50 pF, see <a href="#">Figure 2-3</a>                                     |
| Output rise time <sup>1)</sup>  | $t_r$        | 0.4    | 0.5  | 1    | $\mu\text{s}$ | 1.2 k $\Omega$ / 50 pF, see <a href="#">Figure 2-3</a>                                     |
| Output jitter <sup>1)2)</sup>   | $t_{QJ}$     |        | 0.35 | 1    | $\mu\text{s}$ | For square wave signal with 1 kHz                                                          |
| Delay time <sup>1)3)</sup>      | $t_d$        | 12     | 15   | 30   | $\mu\text{s}$ | see <a href="#">Figure 2-3</a>                                                             |
| Power-on time <sup>1)4)</sup>   | $t_{PON}$    |        | 80   | 150  | $\mu\text{s}$ | $V_{DD} = 3\text{ V}$ , $B \leq B_{RP} - 0.5\text{ mT}$ or $B \geq B_{OP} + 0.5\text{ mT}$ |
| Chopper frequency <sup>1)</sup> | $f_{OSC}$    |        | 350  |      | kHz           |                                                                                            |

1) Not subject to production test, verified by design/characterization.

2) Output jitter is the 1 $\sigma$  value of the output switching distribution.

3) Systematic delay between magnetic threshold reached and output switching.

4) Time from applying  $V_{DD} = 3.0\text{ V}$  to the sensor until the output is valid.

Table 3-5 Magnetic Characteristics

| Parameter                                                            | Symbol            | T (°C) | Values |       |      | Unit  | Note / Test Condition |
|----------------------------------------------------------------------|-------------------|--------|--------|-------|------|-------|-----------------------|
|                                                                      |                   |        | Min.   | Typ.  | Max. |       |                       |
| Operating point                                                      | B <sub>OP</sub>   | -40    | 2      | 4     | 6    | mT    |                       |
|                                                                      |                   | 25     | 1.6    | 3.5   | 5.4  |       |                       |
|                                                                      |                   | 170    | 0.9    | 2.5   | 4.1  |       |                       |
| Release point                                                        | B <sub>RP</sub>   | -40    | 1.1    | 2.8   | 4.5  | mT    |                       |
|                                                                      |                   | 25     | 0.9    | 2.5   | 4.1  |       |                       |
|                                                                      |                   | 170    | 0.3    | 1.8   | 3.2  |       |                       |
| Hysteresis                                                           | B <sub>HYS</sub>  | -40    |        | 1.1   |      | mT    |                       |
|                                                                      |                   | 25     |        | 1     |      |       |                       |
|                                                                      |                   | 170    |        | 0.7   |      |       |                       |
| Effective noise value of the magnetic switching points <sup>1)</sup> | B <sub>Neff</sub> | 25     |        | 62    |      | μT    |                       |
| Temperature compensation of magnetic thresholds <sup>2)</sup>        | T <sub>C</sub>    |        |        | -2000 |      | ppm/K |                       |

1) The magnetic noise is normal distributed and can be assumed as nearly independent to frequency without sampling noise or digital noise effects. The typical value represents a the rms-value and corresponds therefore to a 1  $\sigma$  probability of normal distribution. Consequently a 3  $\sigma$  value corresponds to 99.7% probability of appearance.

2) Not subject to production test, verified by design/characterization.

### Field Direction Definition

Positive magnetic fields are defined with the south pole of the magnet to the branded side of package.

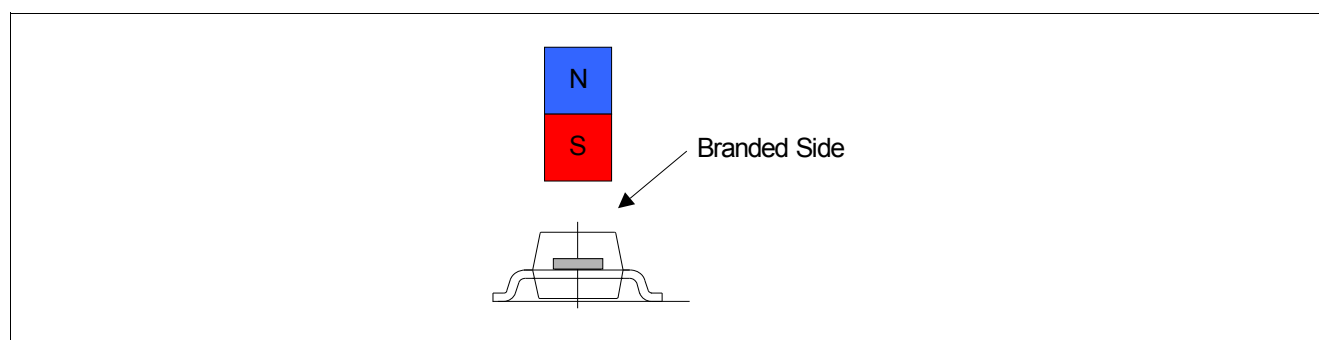
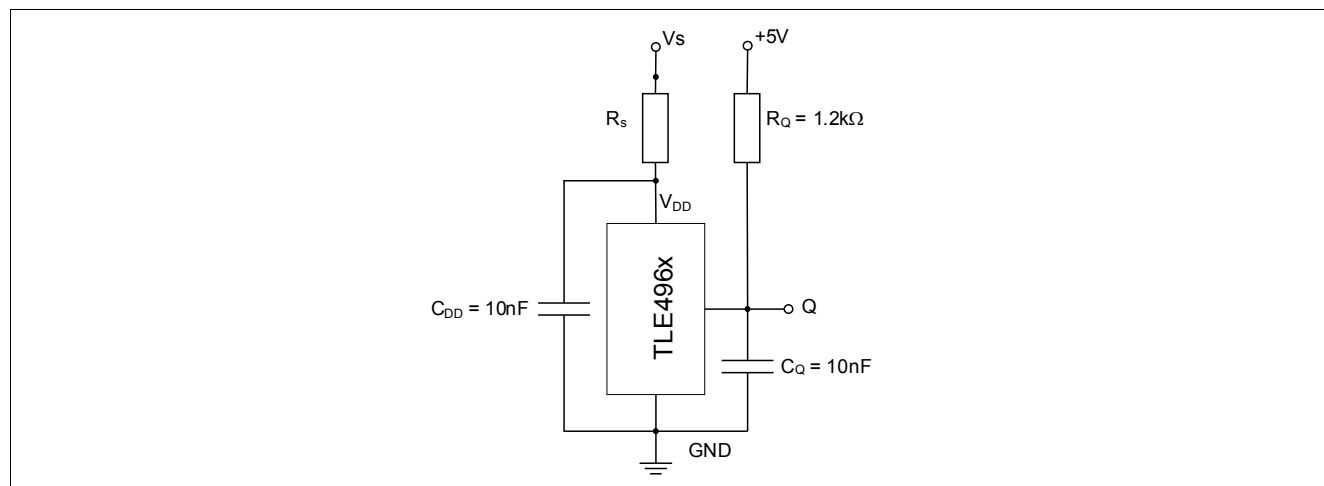


Figure 3-3 Definition of Magnetic Field Direction PG-SOT23-3-15



### 3.5 Electro Magnetic Compatibility

Characterization of Electro Magnetic Compatibility is carried out on a sample basis from one qualification lot. Not all specification parameters have been monitored during EMC exposure.



**Figure 3-4 EMC Test Circuit**

Ref: ISO 7637-2 (Version 2004), test circuit [Figure 3.4](#) (with external resistor,  $R_S = 100 \Omega$ )

**Table 3-6 Magnetic Compatibility**

| Parameter                  | Symbol    | Level / Type                                    | Status |
|----------------------------|-----------|-------------------------------------------------|--------|
| Testpulse 1                | $V_{EMC}$ | -100 V                                          | C      |
| Testpulse 2a <sup>1)</sup> |           | 60 V/110 V                                      | A/C    |
| Testpulse 2b               |           | 10 V                                            | C      |
| Testpulse 3a               |           | -150 V                                          | A      |
| Testpulse 3b               |           | 100 V                                           | A      |
| Testpulse 4 <sup>2)</sup>  |           | -7 V / -5.5 V                                   | A      |
| Testpulse 5b <sup>3)</sup> |           | $U_S = 86.5 \text{ V} / U_S^* = 28.5 \text{ V}$ | A      |

1) ISO 7637-2 (2004) describes internal resistance = 2  $\Omega$  (former 10  $\Omega$ ).

2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V +/- 0.2 V.

3) A central load dump protection of 42 V is used.  $U_S^* = 42 \text{ V}$ -13.5 V.

Ref: ISO 7637-2 (Version 2004), test circuit [Figure 3.4](#) (without external resistor,  $R_S = 0 \Omega$ )

**Table 3-7 Electro Magnetic Compatibility**

| Parameter                  | Symbol    | Level / Type                                    | Status |
|----------------------------|-----------|-------------------------------------------------|--------|
| Testpulse 1                | $V_{EMC}$ | -50 V                                           | C      |
| Testpulse 2a <sup>1)</sup> |           | 50 V                                            | A      |
| Testpulse 2b               |           | 10 V                                            | C      |
| Testpulse 3a               |           | -150 V                                          | A      |
| Testpulse 3b               |           | 100 V                                           | A      |
| Testpulse 4 <sup>2)</sup>  |           | -7 V / 5.5 V                                    | A      |
| Testpulse 5b <sup>3)</sup> |           | $U_S = 86.5 \text{ V} / U_S^* = 28.5 \text{ V}$ | A      |

1) ISO 7637-2 (2004) describes internal resistance = 2  $\Omega$  (former 10  $\Omega$ ).

2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V +/- 0.2 V.

3) A central load dump protection of 42 V is used.  $U_S^* = 42 \text{ V}$ -13.5 V.

## 4 Package Information

The TLE4964-6M is available in the small halogen free SMD package PG-SOT23-3-15.

### 4.1 Package Outline PG-SOT23-3-15

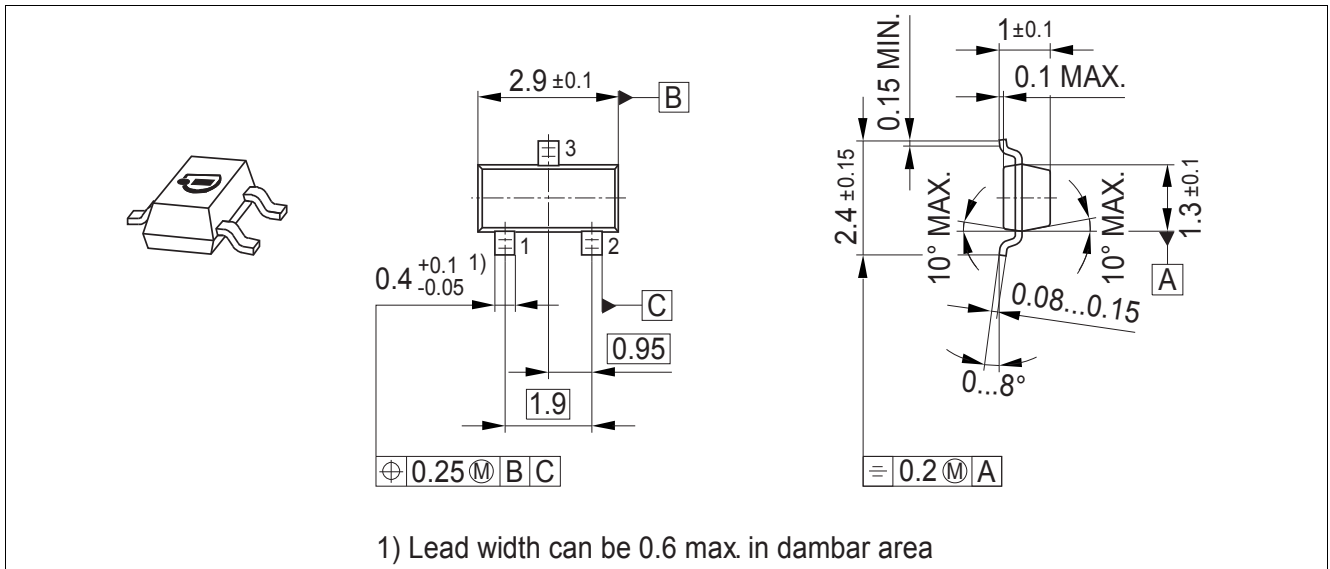


Figure 4-1 PG-SOT23-3-15 Package Outline (All Dimensions in mm)

### 4.2 Packing Information PG-SOT23-3-15

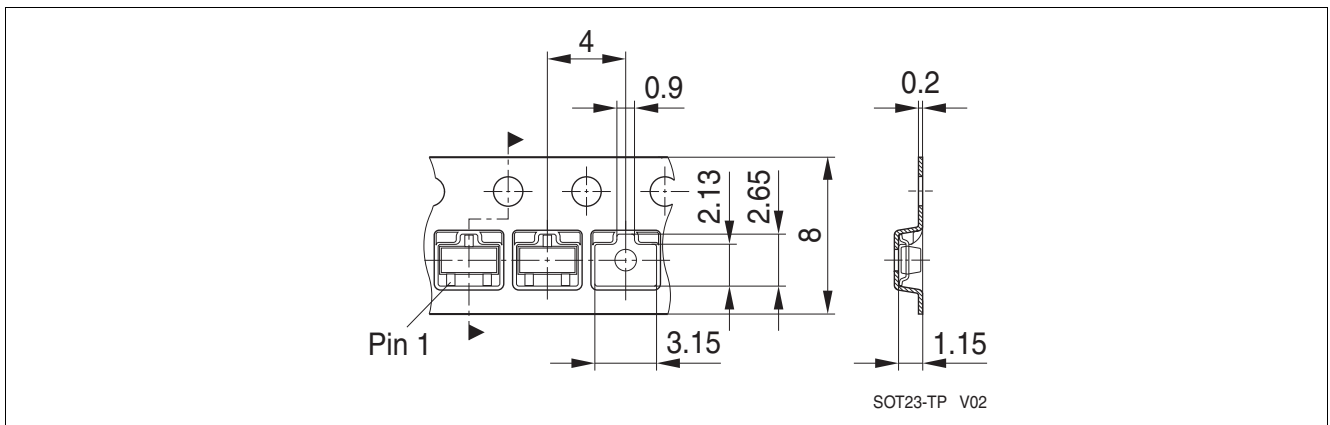


Figure 4-2 Packing of the PG-SOT23-3-15 in a Tape

### 4.3 Footprint PG-SC59-3-5 and PG-SOT23-3-15

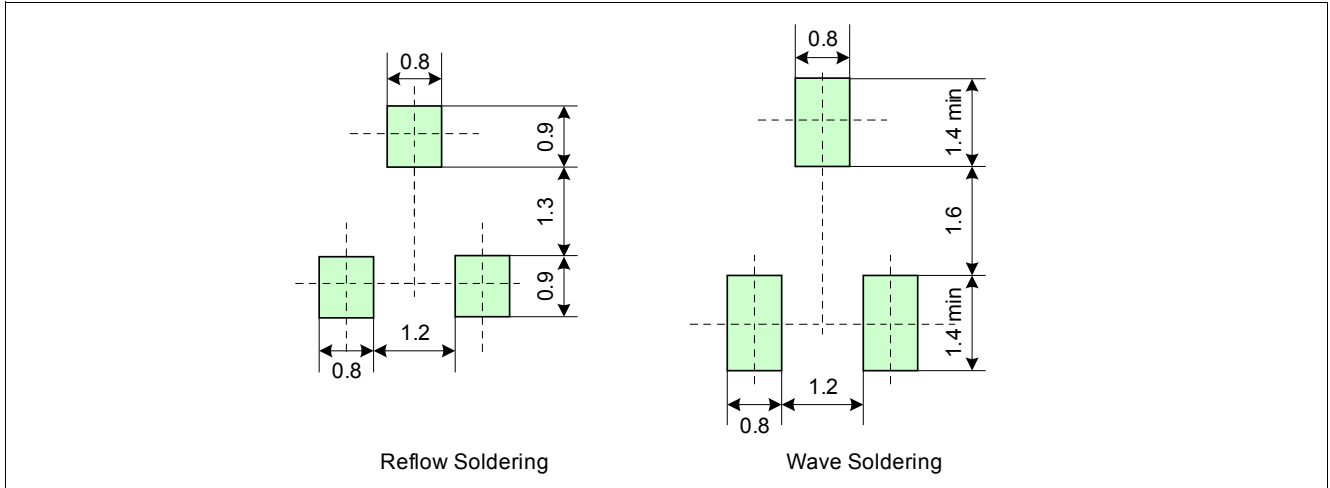


Figure 4-3 Footprint PG-SC59-3-5 and PG-SOT23-3-15

### 4.4 PG-SOT23-3-15 Distance between Chip and Package

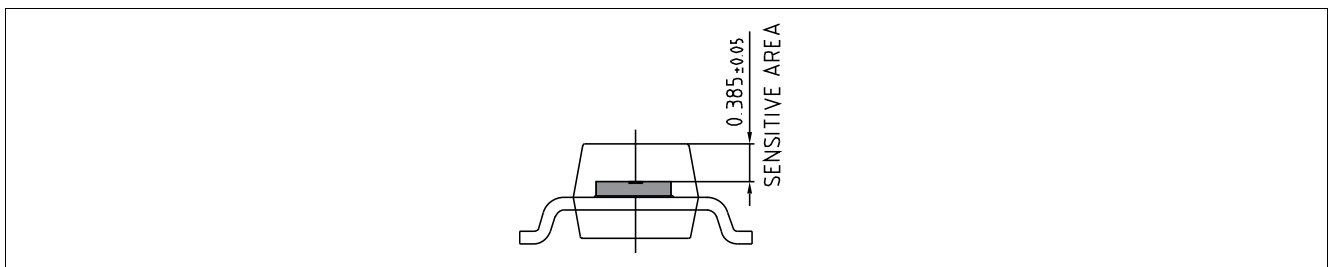


Figure 4-4 Distance between Chip and Package

### 4.5 Package Marking

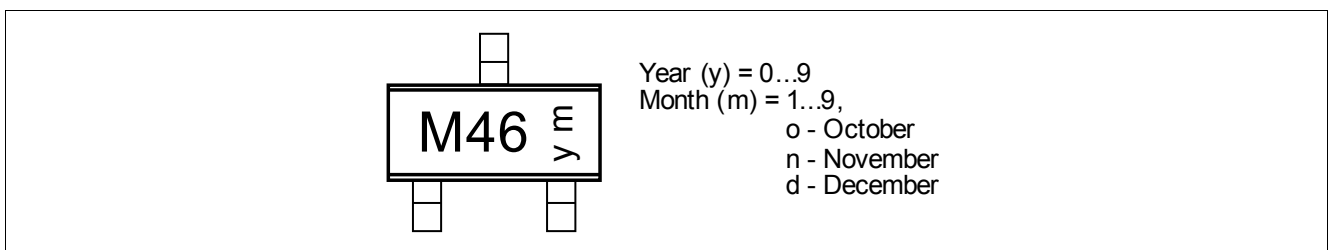


Figure 4-5 Marking of TLE4964-6M

## 5 Graphs of the Magnetic Parameters

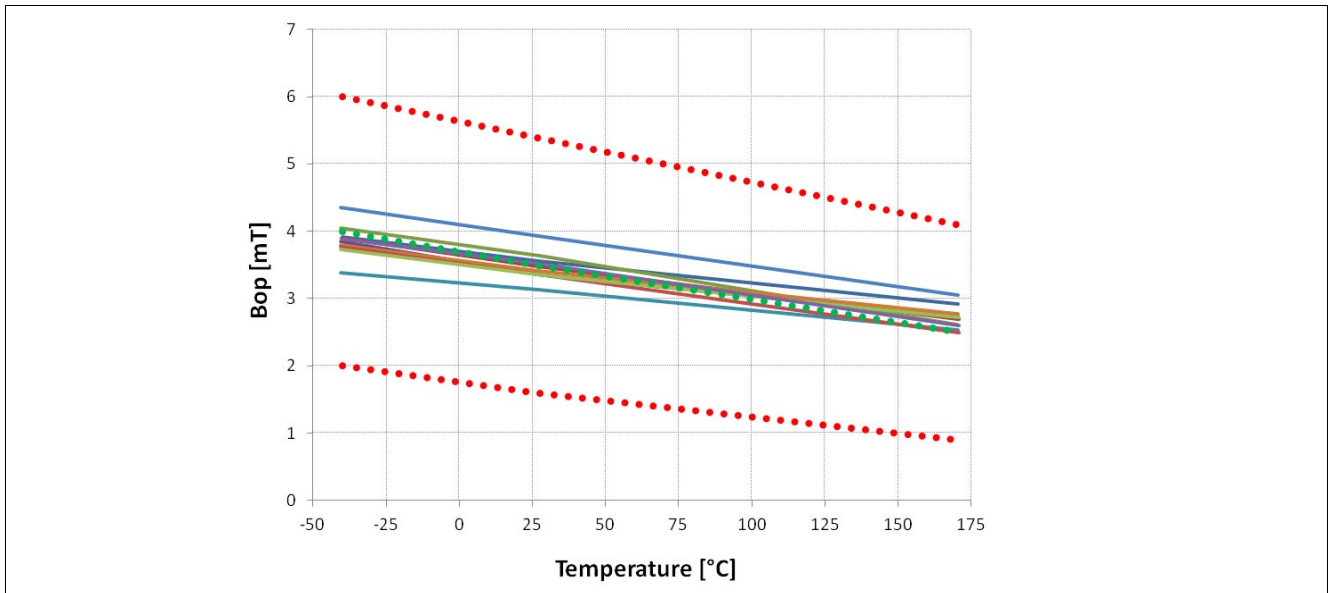


Figure 5-1 Operating Point ( $B_{OP}$ ) of the TLE4964-6M over Temperature

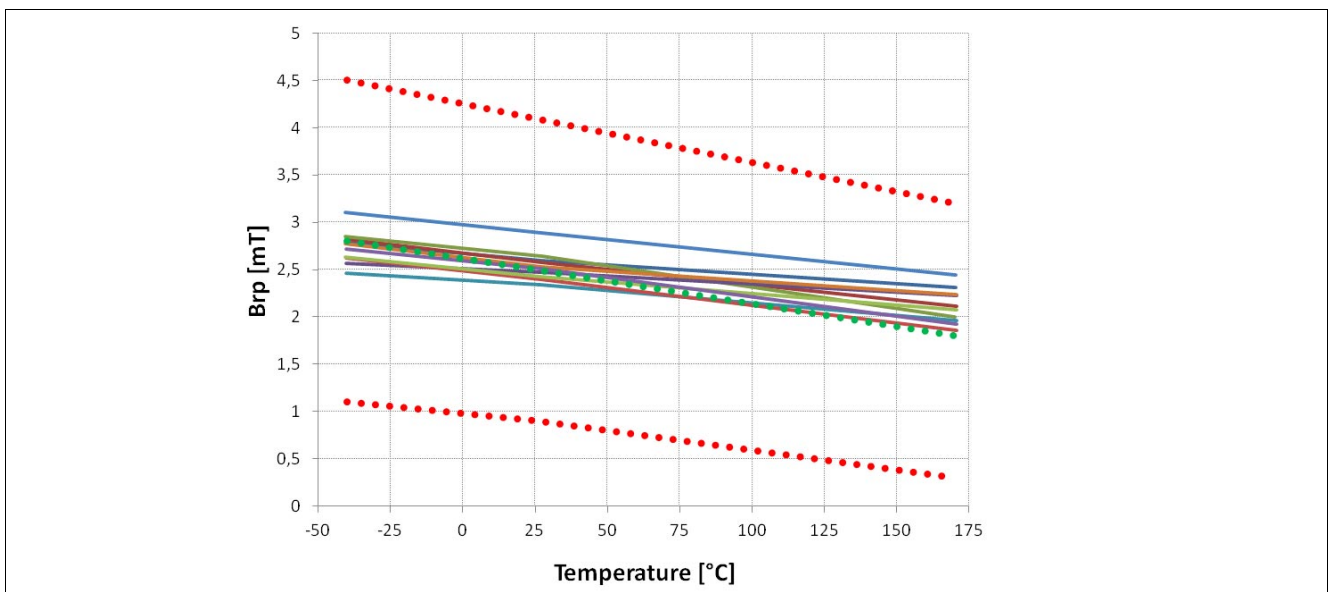


Figure 5-2 Release Point ( $B_{RP}$ ) of the TLE4964-6M over Temperature

## Graphs of the Electrical Parameters

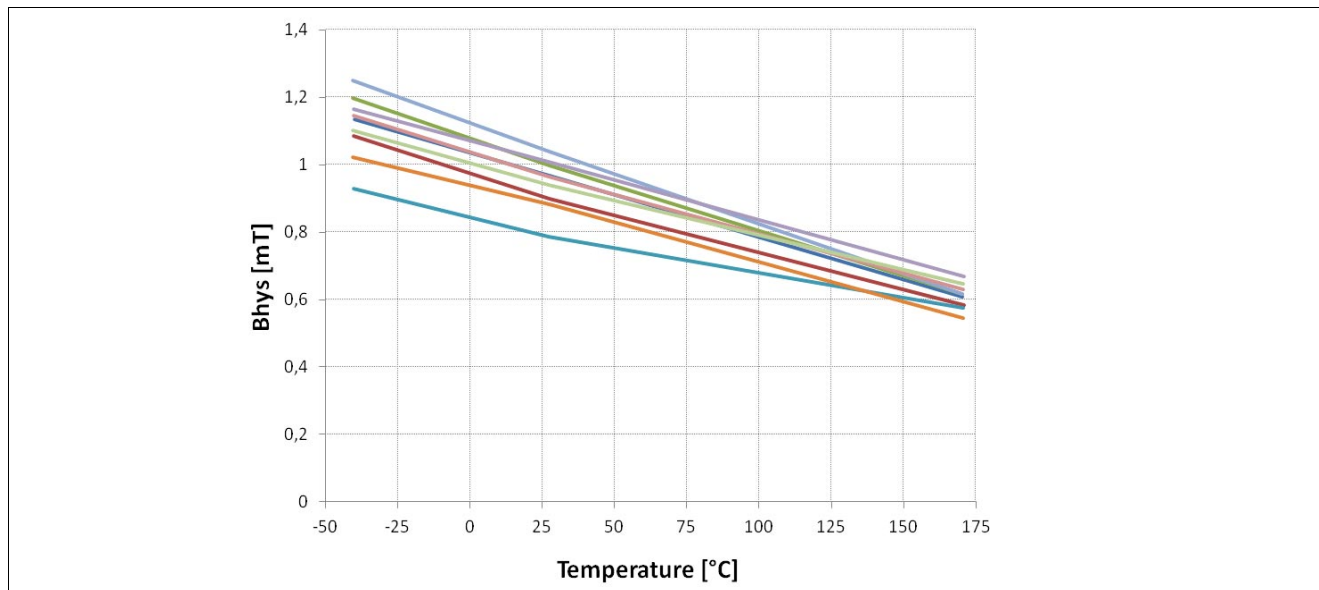


Figure 5-3 Hysteresis ( $B_{Hys}$ ) of the TLE4964-6M over Temperature

## 6 Graphs of the Electrical Parameters

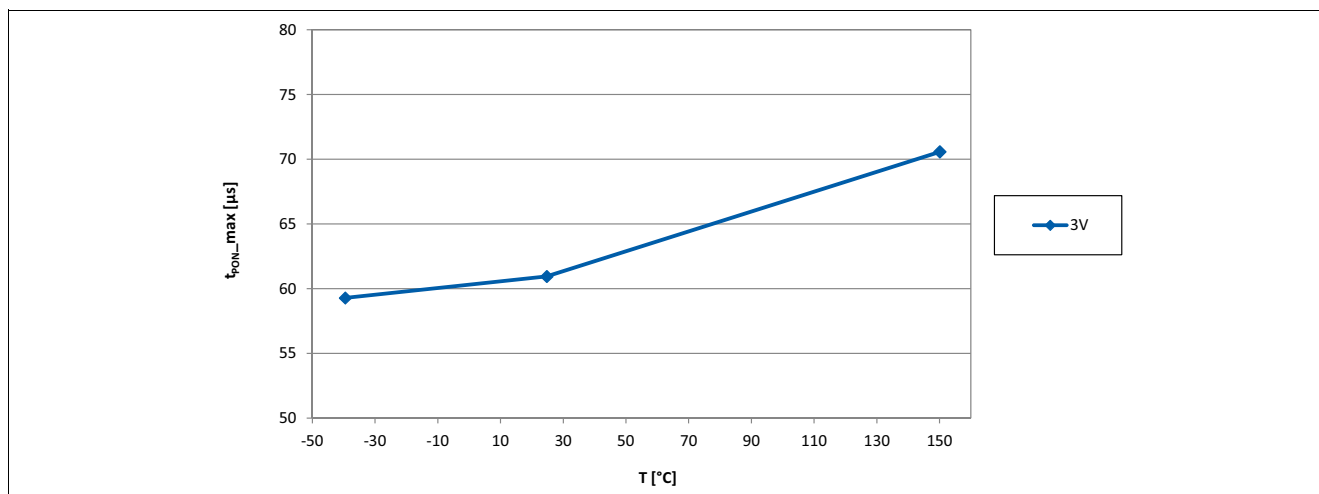
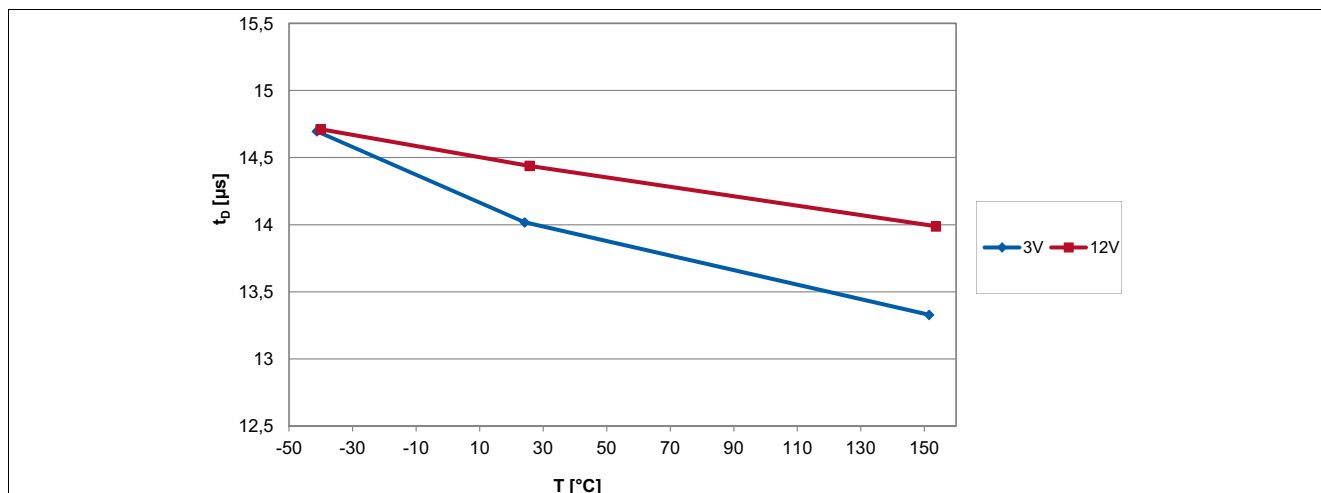
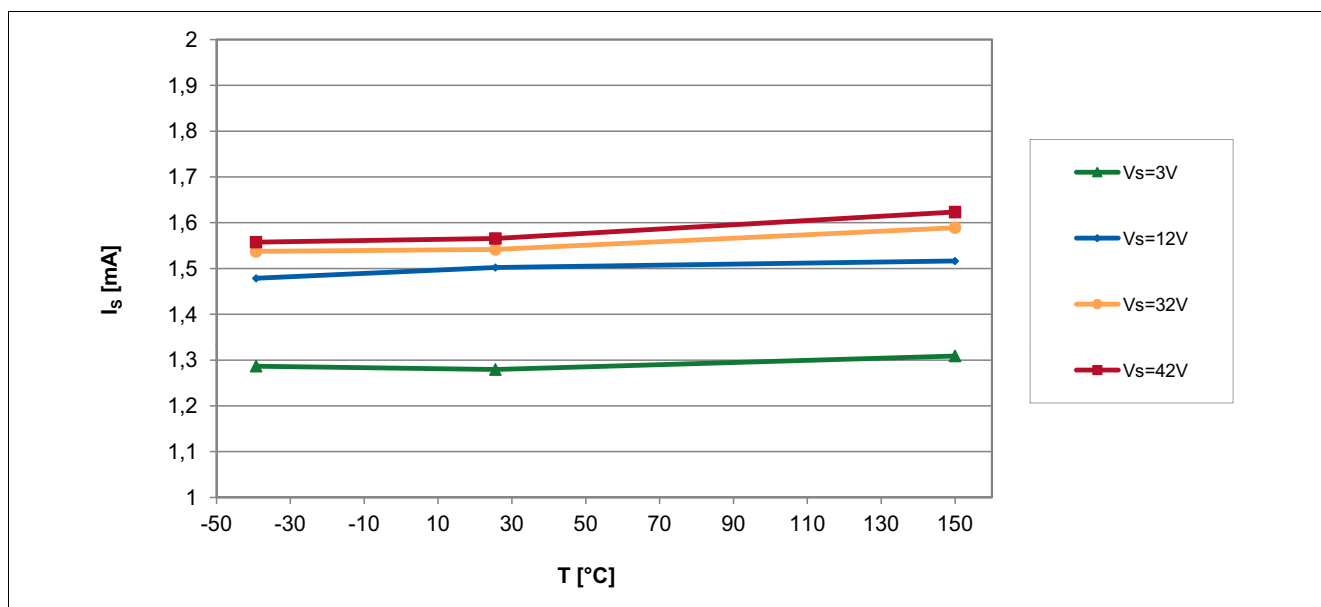


Figure 6-1 Power On Time  $t_{PON}$  of the TLE4964-6M over Temperature

# Graphs of the Electrical Parameters

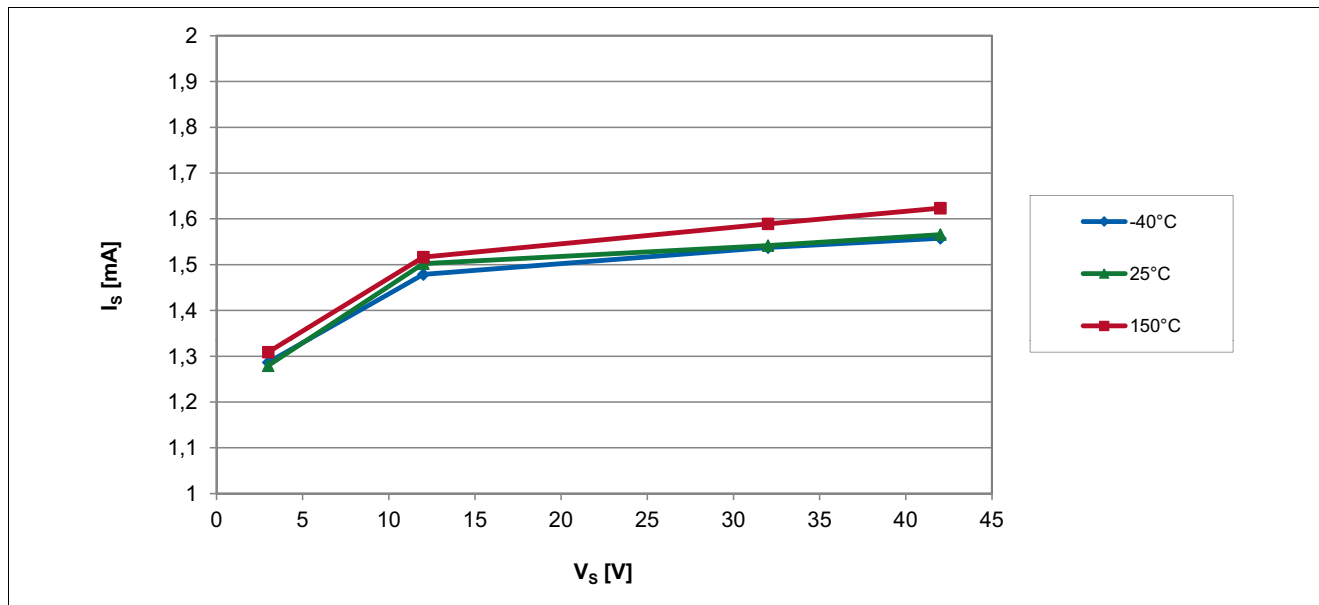


**Figure 6-2** Signal Delay Time of the TLE4964-6M over Temperature

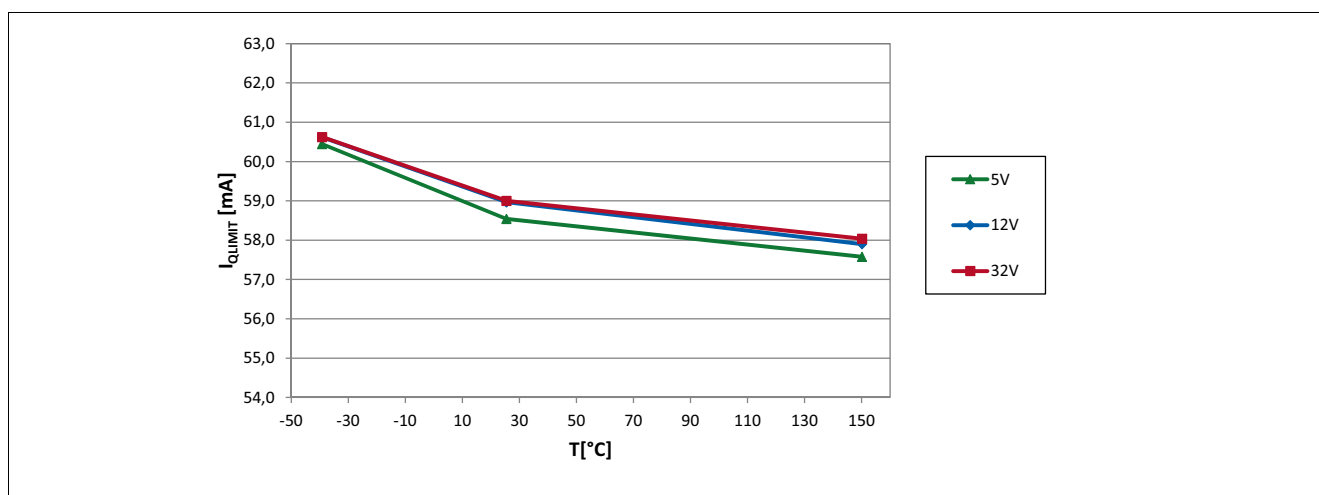


**Figure 6-3** Supply Current of the TLE4964-6M over Temperature

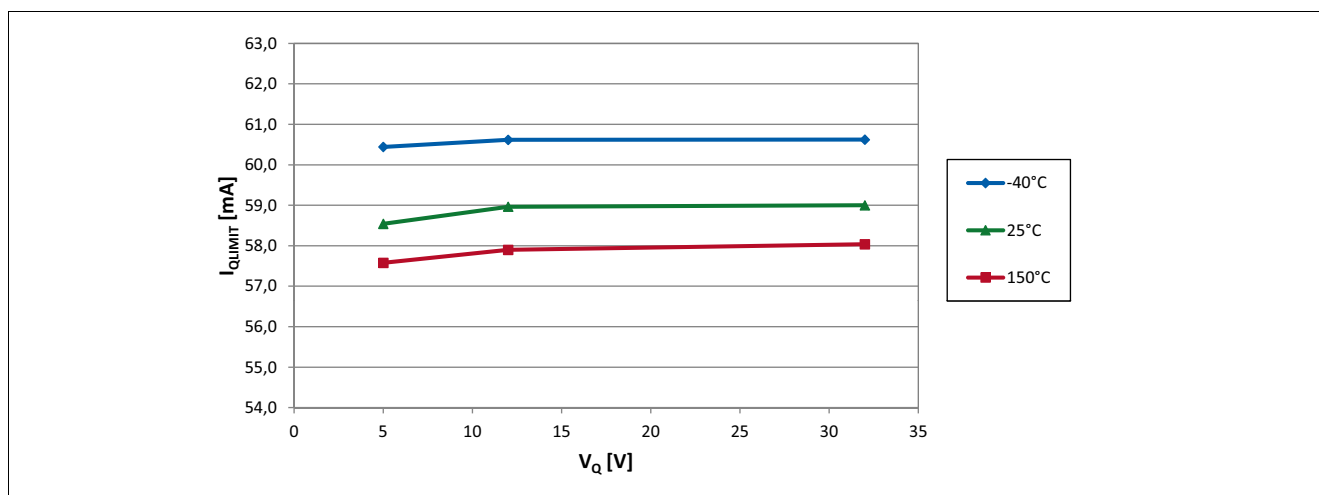
# Graphs of the Electrical Parameters



**Figure 6-4 Supply Current of the TLE4964-6M over Supply Voltage**

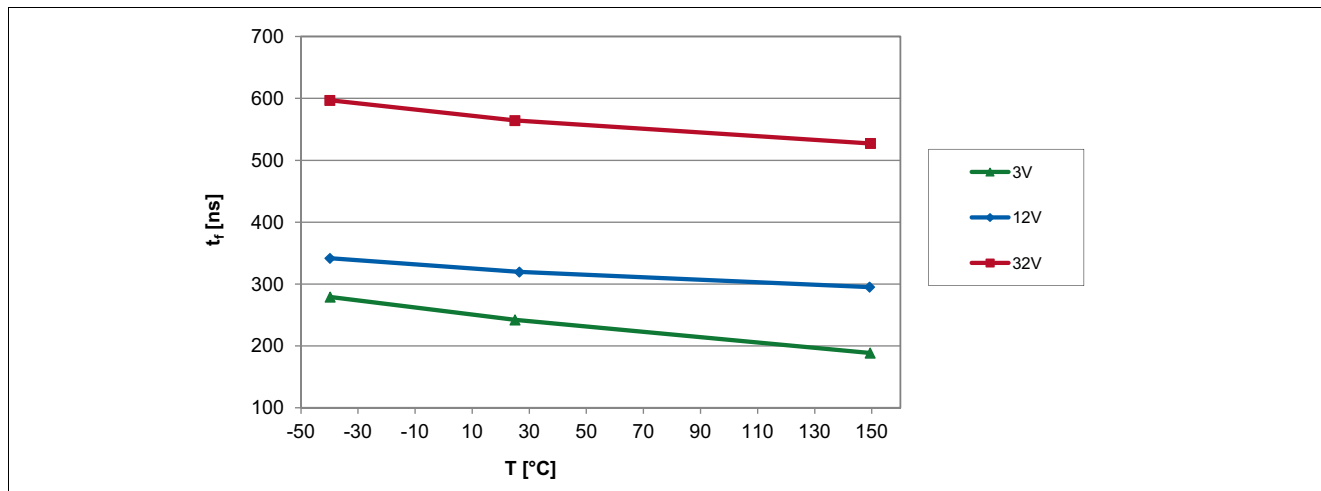


**Figure 6-5 Output Current Limit of the TLE4964-6M over Temperature**

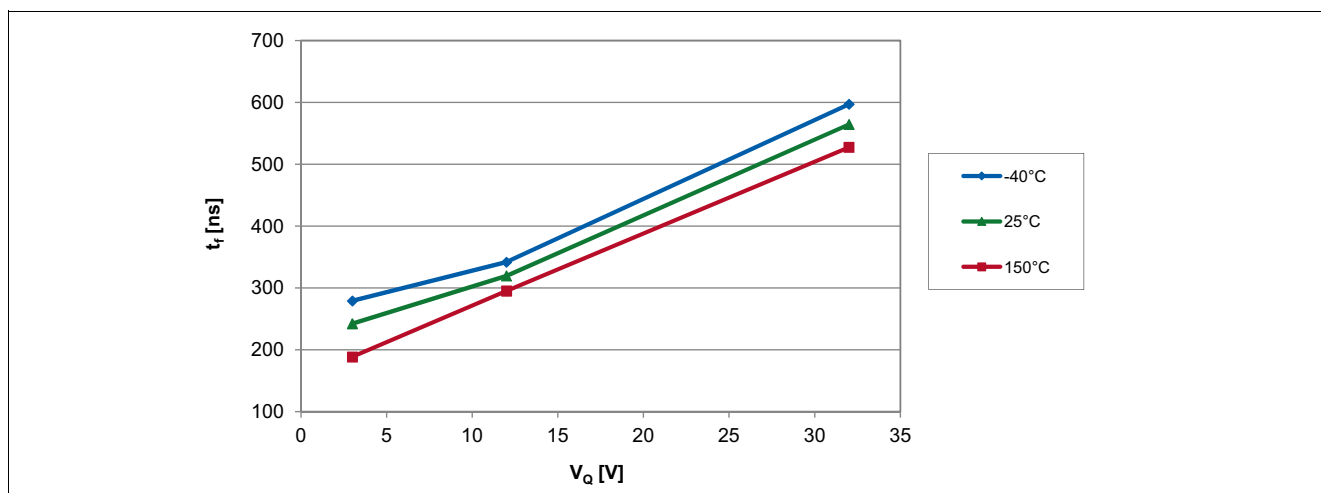


**Figure 6-6 Output Current Limit of the TLE4964-6M over applied Pull-up Voltage**

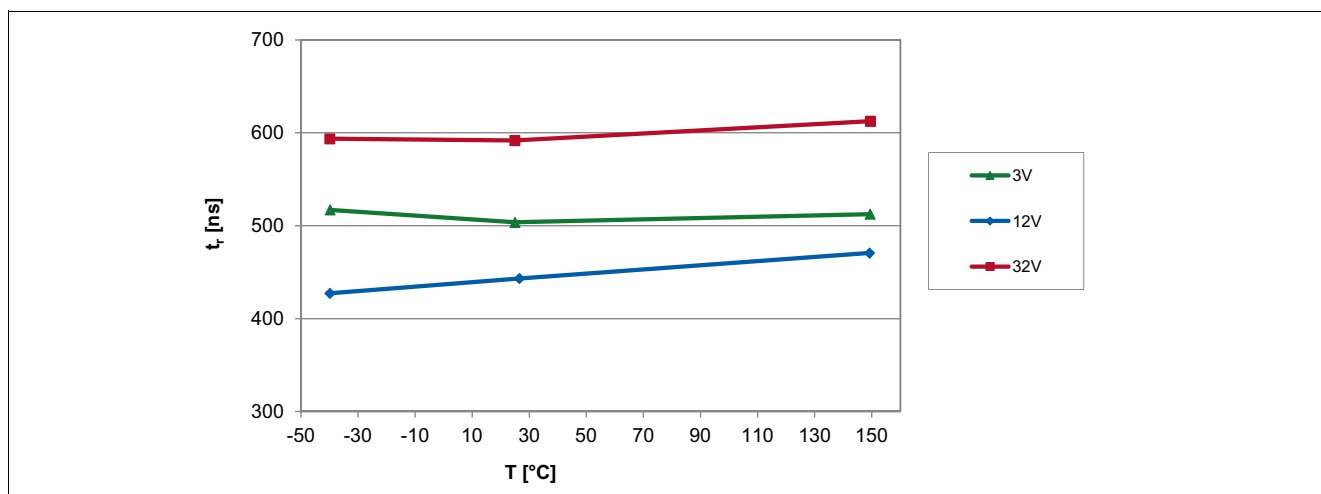
# Graphs of the Electrical Parameters



**Figure 6-7** Output Fall Time of the TLE4964-6M over Temperature



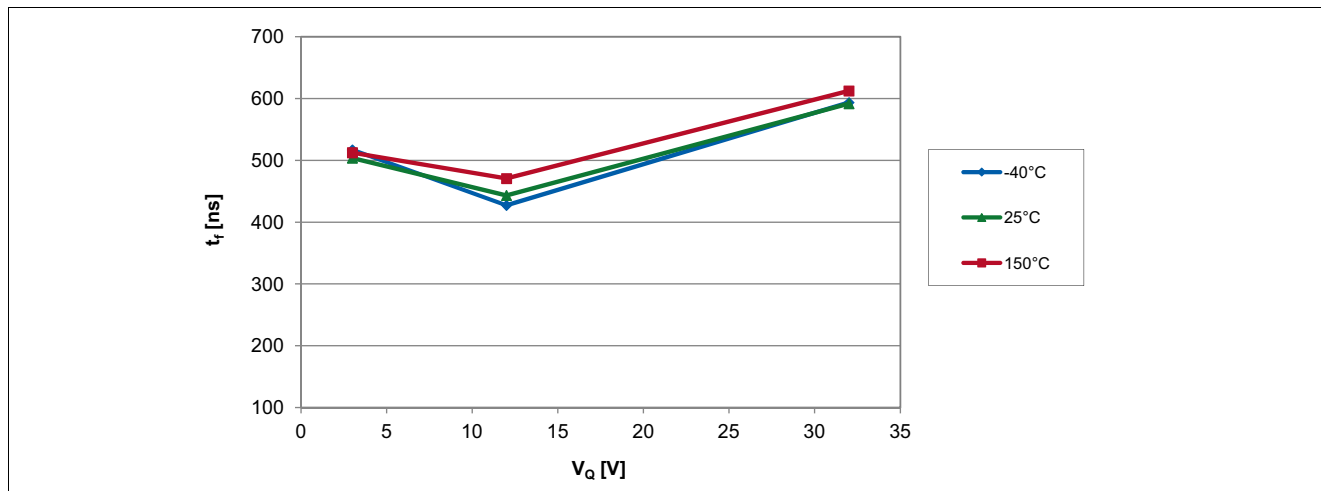
**Figure 6-8** Output Fall Time of the TLE4964-6M over applied Pull-up Voltage



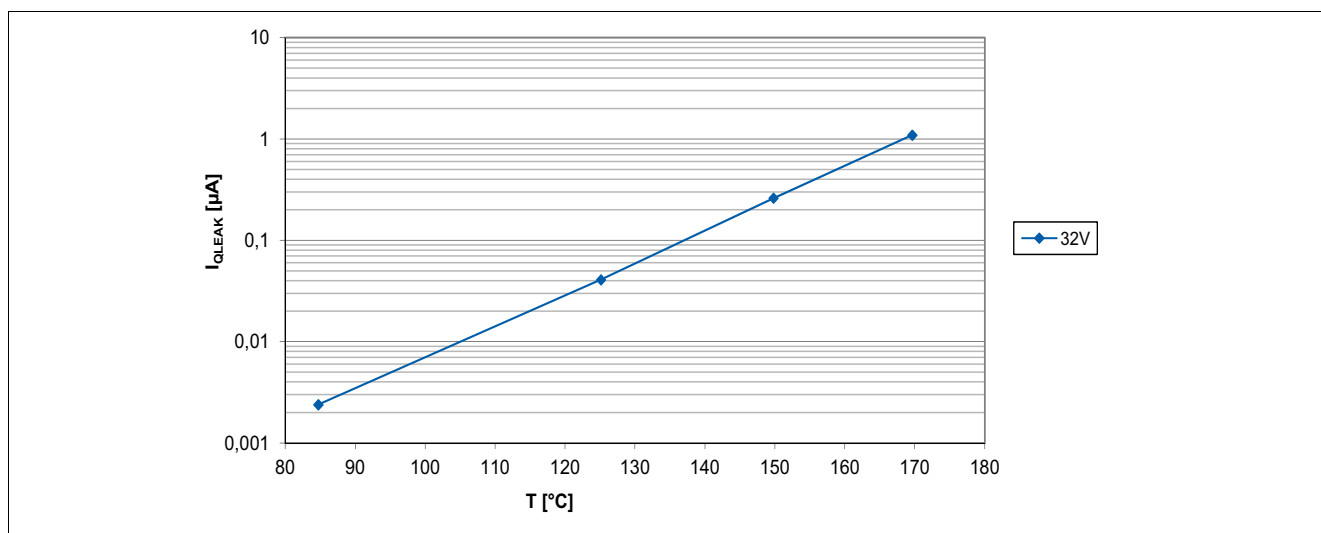
**Figure 6-9** Output Rise Time of the TLE4964-6M over Temperature



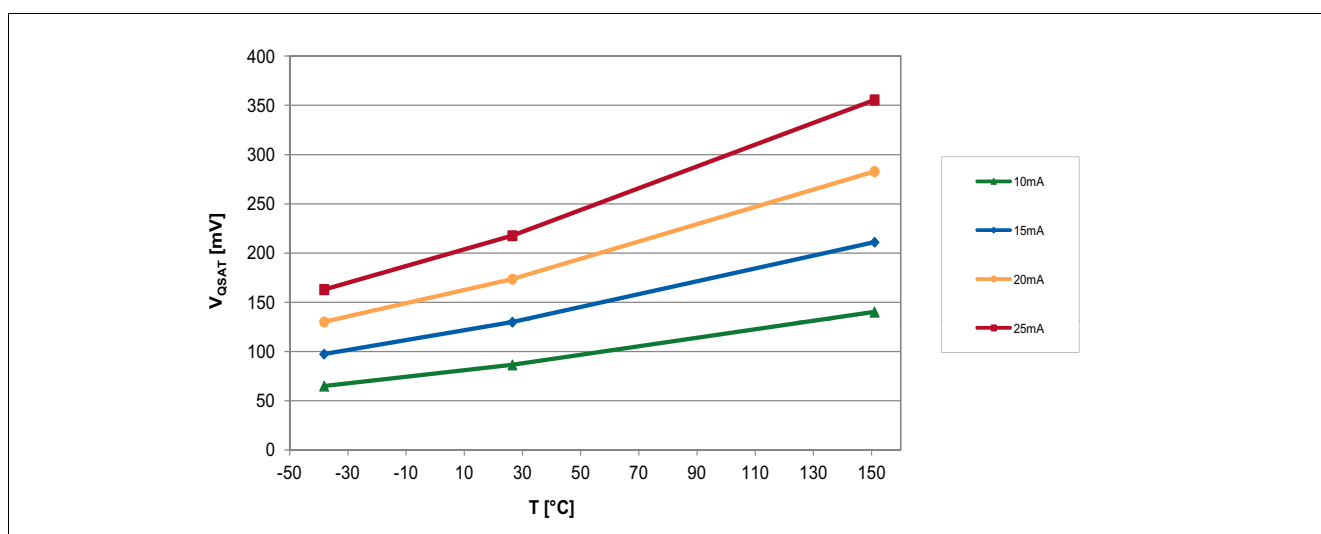
# Graphs of the Electrical Parameters



**Figure 6-10** Output Rise Time of the TLE4964-6M over applied Pull-up Voltage

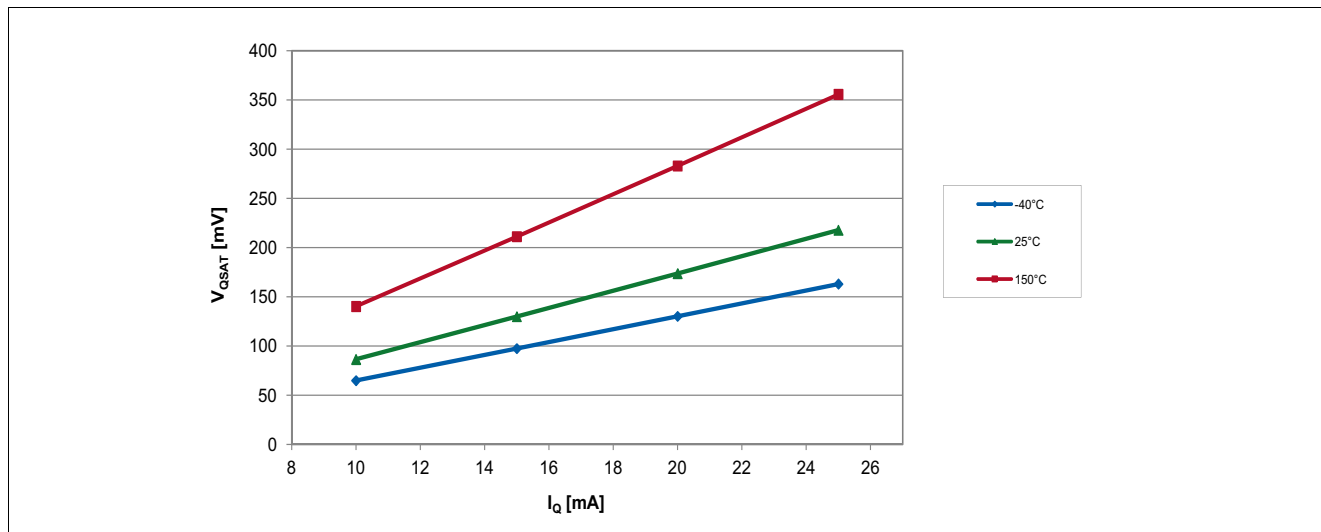


**Figure 6-11** Output Leakage Current of the TLE4964-6M over Temperature

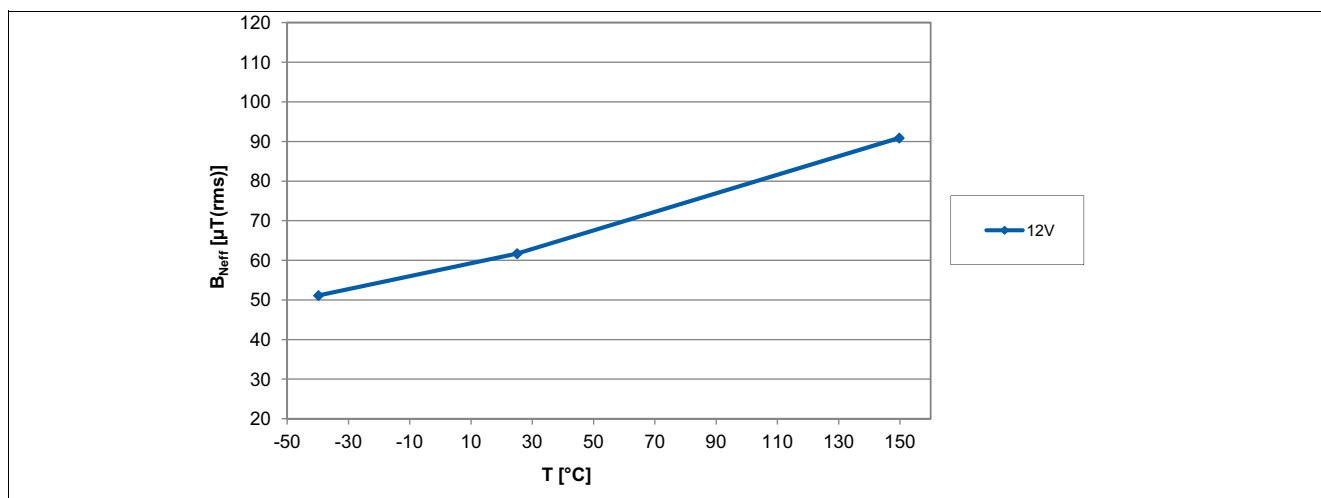


**Figure 6-12** Saturation Voltage of the TLE4964-6M over Temperature

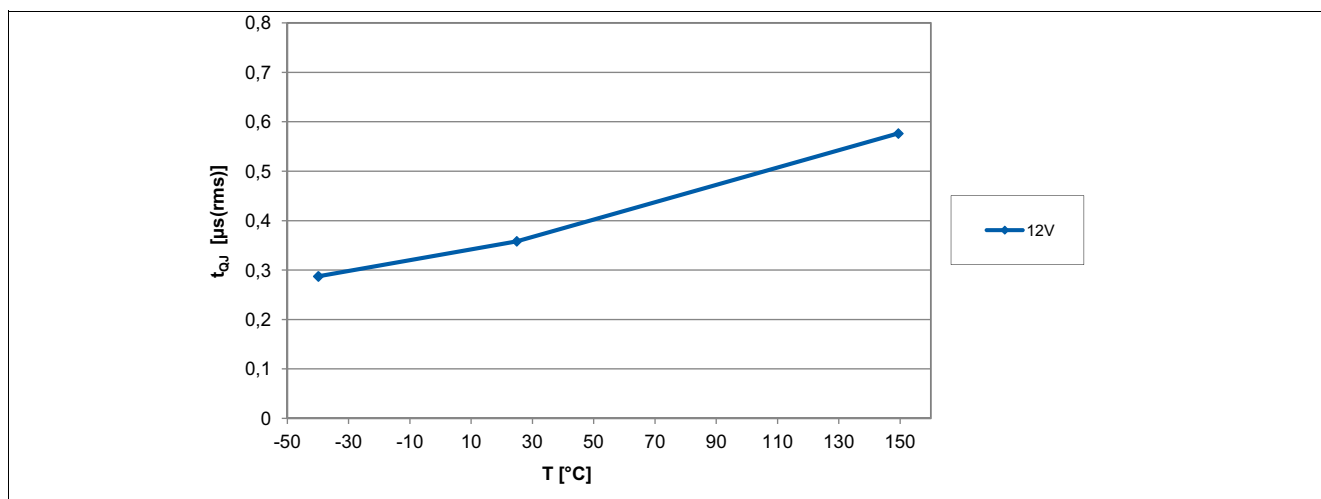
# Graphs of the Electrical Parameters



**Figure 6-13 Saturation Voltage of the TLE4964-6M over Output Current**



**Figure 6-14 Effective Noise of the TLE4964-6M Thresholds over Temperature**



**Figure 6-15 Output Signal Jitter of the TLE4964-6M over Temperature**

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