SLOS280D - JANUARY 2000 - REVISED NOVEMBER 2002

- Ideal for Notebook Computers, PDAs, and Other Small Portable Audio Devices
- 1 W Into 8-Ω From 5-V Supply
- 0.3 W Into 8-Ω From 3-V Supply
- Stereo Head Phone Drive
- Mono (BTL) Signal Created by Summing Left and Right Signals Internally
- Wide Power Supply Compatibility 2.5 V to 5.5 V
- Low Supply Current
 - 3.2 mA Typical at 5 V
 - 2.7 mA Typical at 3 V
- Shutdown Control . . . 1 μA Typical
- Shutdown Pin Is TTL Compatible
- –40°C to 85°C Operating Temperature Range
- Space-Saving, Thermally-Enhanced MSOP Packaging

description

The TPA0253 is a 1-W mono bridge-tied-load (BTL) amplifier designed to drive speakers with as low as $8-\Omega$ impedance. The mono signal is created by summing left and right inputs internally. The amplifier can be reconfigured on the fly to drive two stereo single-ended (SE) signals into headphones. This makes the device ideal for use in small notebook computers, PDAs, digital personal audio players, anyplace a mono speaker and stereo headphones are required. From a 5-V supply, the TPA0253 can deliver 1-W of power into an $8-\Omega$ speaker.

The gain of the input stage is set by the user-selected input resistor and a 50-k Ω internal feedback resistor (A_V = - R_F/R_I). The power stage is internally configured with a gain of -1.25 V/V in SE mode, and -2.5 V/V in BTL mode. Thus, the overall gain of the amplifier is 62.5 k Ω /R_I in SE mode and 125 k Ω /R_I in BTL mode. The input terminals are high-impedance CMOS inputs, and can be used as summing nodes.

The TPA0253 is available in the 10-pin thermally-enhanced MSOP package (DGQ) and operates over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

	PACKAGED DEVICES	MOOD
TA	MSOP† (DGQ)	MSOP SYMBOLIZATION
-40°C to 85°C	TPA0253DGQ	AEL

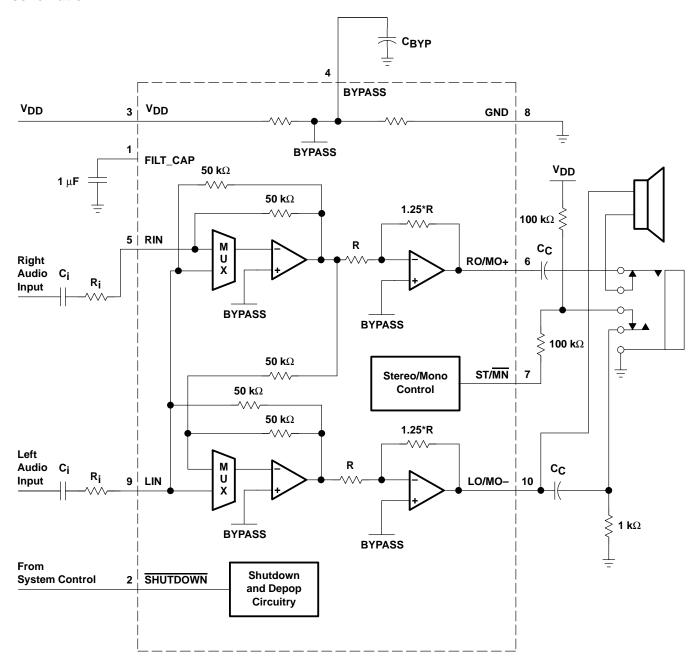
[†] The DGQ package are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0253DGQR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



schematic





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Terminal Functions

TERMINA	AL		DESCRIPTION								
NAME	NO.	1/0	DESCRIPTION								
BYPASS	4	ı	Midrail bias voltage								
FILT_CAP	1		Terminal used to filter power supply								
GND	8		Ground terminal								
LIN	9	ı	Left-channel input terminal								
LO/MO-	10	0	Left-output in SE mode and mono negative output in BTL mode.								
RIN	5	ı	Right-channel input terminal								
RO/MO+	6	0	Right-output in SE mode and mono positive output in BTL mode								
SHUTDOWN	2	ı	TTL-compatible shutdown terminal								
ST/MN	7	I	Selects between stereo and mono mode. When held high, the amplifier is in SE stereo mode; while held low, the amplifier is in BTL mono mode.								
V_{DD}	3	I	Positive power supply								

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{DD}	6 V
Input voltage range, V ₁	
Continuous total power dissipation	internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T _A (see Table 3)	40°C to 85°C
Operating junction temperature range, T _J	–40°C to 150°C
Storage temperature range, T _{stq}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seco	nds 260°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{\scriptsize A}} \leq 25^{\circ} \mbox{\scriptsize C}$	DERATING FACTOR	T _A = 70°C	T _A = 85°C
DGQ	2.14 W§	17.1 mW/°C	1.37 W	1.11 W

[‡] Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of that document.

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recommended operating conditions

			MIN	MAX	UNIT	
Supply voltage, V _{DD}			2.5	5.5	V	
	OT/1401	V _{DD} = 3 V	2.7			
High-level input voltage, VIH	ST/MN	V _{DD} = 5 V	4.5		V	
	SHUTDOWN					
	OT/MAN	V _{DD} = 3 V		1.65		
Low-level input voltage, V _{IL}	ST/MN	V _{DD} = 5 V		2.75	2.75 V	
	SHUTDOWN			0.8		
Operating free-air temperature, TA			-40	85	°C	

electrical characteristics at specified free-air temperature, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITION	S	MIN	TYP	MAX	UNIT	
IVool	Output offset voltage (measured differentially)	$R_L = 4 \Omega$, $ST/\overline{MN} = 0 V$, \overline{SHUTC}			30	mV		
PSRR	Power supply rejection ratio	$V_{DD} = 2.9 \text{ V to } 3.1 \text{ V}, \text{ BTL mo}$	de		65		dB	
		SHUTDOWN, V _{DD} = 3.3 V,	$V_I = V_{DD}$			1		
Ічні	High-level input current	ST/\overline{MN} , $V_{DD} = 3.3 \text{ V}$,	$V_I = V_{DD}$			1	μΑ	
	Landard Sandardan	SHUTDOWN, V _{DD} = 3.3 V,	V _I = 0 V			1	μΑ	
I L	Low-level input current	ST/\overline{MN} , $V_{DD} = 3.3 \text{ V}$,	V _I = 0 V			1		
Z _I	Input impedance				50		kΩ	
lDD	Supply current	$V_{DD} = 2.5 \text{ V}, \overline{\text{SHUTDOWN}} = 2.5 \text{ V}$	2 V		2.7	4	mA	
I _{DD(SD)}	Supply current, shutdown mode	SHUTDOWN = 0 V			1	10	μΑ	
R _F	Feedback resistor	$\frac{V_{DD} = 2.5 \text{ V}, R_L = 4 \Omega, ST/MN}{\text{SHUTDOWN}} = 2 \text{ V}$	= 1.375 V,	47	50	57	kΩ	

operating characteristics, V_{DD} = 3 V, T_{A} = 25°C, R_{L} = 8 Ω , f = 1 kHz (unless otherwise noted)

	PARAMETER	TE	EST CONDITIONS		MIN	TYP	MAX	UNIT	
		THD = 0.1%,	BTL mode,	TL mode, Gain = 14 dB		300			
PO	Output power, see Note 1	THD = 0.1% Gain = 1.9 dB	SE mode,	$R_L = 32 \Omega$		30		mW	
THD + N	Total harmonic distortion plus noise	P _O = 250 mW,	f = 20 Hz to 20 kHz			0.2%			
Вом	Maximum output power bandwidth	Gain = 1.9 dB,	THD = 2%	·		20		kHz	
	Outside stands as to a first as a set to	£ 4111-	0 0.47 5	BTL mode		46		j	
	Supple ripple rejection ratio	f = 1 kHz,	$C_{(BYP)} = 0.47 \mu F$	SE mode		68		dB	
V		0 047.5	f 00 H= t= 00 HH=	BTL mode	83			.,	
V _n	Noise output voltage	$C(BYP) = 0.47 \mu F,$	f = 20 Hz to 20 kHz	SE mode		33		μVRMS	

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.



electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
IVool	Output offset voltage (measured differentially)	$R_L = 4 \Omega$, $ST/\overline{MN} = 0 V$, \overline{SHUT}			30	mV	
PSRR	Power supply rejection ratio	$V_{DD} = 4.9 \text{ V to } 5.1 \text{ V}, \text{ BTL m}$	ode	, ,	62		dB
	High level input compart	SHUTDOWN, V _{DD} =5.5 V,	$V_I = V_{DD}$			1	4
Іні	High-level input current	ST/\overline{MN} , $V_{DD} = 5.5 V$,	$V_I = V_{DD}$,		1	μΑ
	Law law liam tangent	SHUTDOWN, V _{DD} = 5.5 V,	V _I = 0 V			1	•
11	Low-level input current	ST/\overline{MN} , $V_{DD} = 5.5 V$,	V _I = 0 V			1	μΑ
Z _I	Input impedance				50		kΩ
IDD	Supply current	SHUTDOWN = 2 V			3.2	4.8	mA
I _{DD(SD)}	Supply current, shutdown mode	SHUTDOWN = 0 V			1	10	μΑ

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω , f = 1 kHz (unless otherwise noted)

	PARAMETER	TI	EST CONDITIONS		MIN 7	ΓYP Ν	IAX	UNIT	
	Outside a success (see a Neda 4)	THD = 0.1%,	BTL mode	BTL mode				W	
PO	Output power (see Note 1)	THD = 0.1%,	SE mode,	R _L = 32 Ω		85		mW	
THD + N	Total harmonic distortion plus noise	P _O = 1 W,	f = 20 Hz to 20 kHz		0.33%				
ВОМ	Maximum output power bandwidth	Gain = 8 dB,	THD = 2%		,	20		kHz	
	Occasio de als sels effectivos		0 047 5	BTL mode		46		j	
	Supple ripple rejection ratio	f = 1 kHz,	$C_{(BYP)} = 0.47 \mu\text{F}$	SE mode		60		dB	
	Nie ie e eutrost veltere	0 047 5	£ 00 H= 40 00 HH=	BTL mode		85			
V _n	Noise output voltage	$C_{(BYP)} = 0.47 \mu\text{F},$	f = 20 Hz to 20 kHz	SE mode		34		μVRMS	

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.







6-Feb-2020

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TPA0253DGQ	ACTIVE	HVSSOP	DGQ	10	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AEL	Samples
TPA0253DGQG4	ACTIVE	HVSSOP	DGQ	10	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AEL	Samples
TPA0253DGQR	ACTIVE	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AEL	Samples
TPA0253DGQRG4	ACTIVE	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AEL	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

6-Feb-2020

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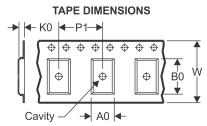
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PACKAGE MATERIALS INFORMATION

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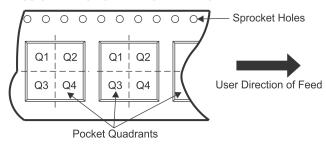
TAPE AND REEL INFORMATION





A0	
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA0253DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

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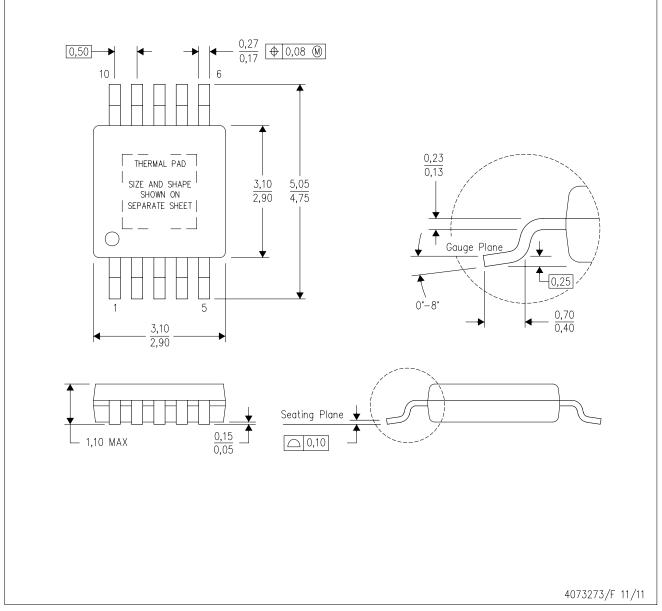


*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
I	TPA0253DGQR	HVSSOP	DGQ	10	2500	358.0	335.0	35.0

DGQ (S-PDSO-G10)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions. F. Falls within JEDEC MO-187 variation BA-T.

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DGQ (S-PDSO-G10)

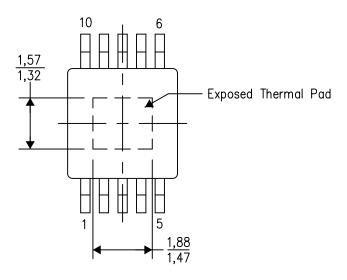
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

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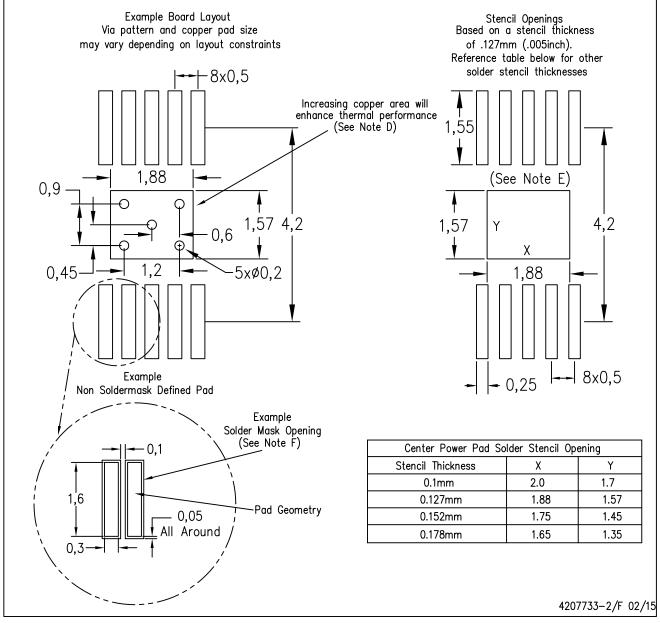
NOTE: A. All linear dimensions are in millimeters

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DGQ (S-PDSO-G10)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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