

# THC63LVDM83D-Z

## 24bit COLOR OPEN LDI(LVDS) TRANSMITTER

### General Description

The THC63LVDM83D-Z transmitter is designed to support pixel data transmission between Host and Flat Panel Display up to 1080p/WUXGA resolutions.

The THC63LVDM83D-Z converts 28bits of LVCMOS data into four OpenLDI(LVDS) data streams. The transmitter can be programmed for rising edge or falling edge clock through a dedicated pin. At a transmit clock frequency of 160MHz, 24bits of RGB data and 4bits of timing and control data (HSYNC, VSYNC, DE, CONT1) are transmitted at an effective rate of 1120Mbps per OpenLDI(LVDS) channel.

### Application

- Medium and Small Size Panel
- Tablet PC / Notebook PC
- Security Camera / Industrial Camera
- Multi Function Printer
- Industrial Equipment
- Medical Equipment Monitor
- Automotive

### Features

- Compatible with TIA/EIA-644 LVDS Standard
- 7:1 OpenLDI(LVDS) Transmitter
- Operating Temperature Range : -40 to +105°C
- No Special Start-up Sequence Required
- Spread Spectrum Clocking Tolerant up to 100kHz Frequency Modulation and +/-2.5% Deviations.
- Wide Dot Clock Range: 8 to 160MHz Suited for  
TV Signal : NTSC(12.27MHz) - 1080p(148.5MHz)  
PC Signal : QVGA(8MHz) - WUXGA(154MHz)
- 56pin TSSOP Package
- 1.2V to 3.3V LVCMOS inputs are supported.
- LVDS swing is reducible as 200mV by RS-pin to reduce EMI and power consumption.
- PLL requires no external components.
- Power Down Mode
- Input clock triggering edge is selectable by R/F-pin.
- EU RoHS Compliant

### Block Diagram

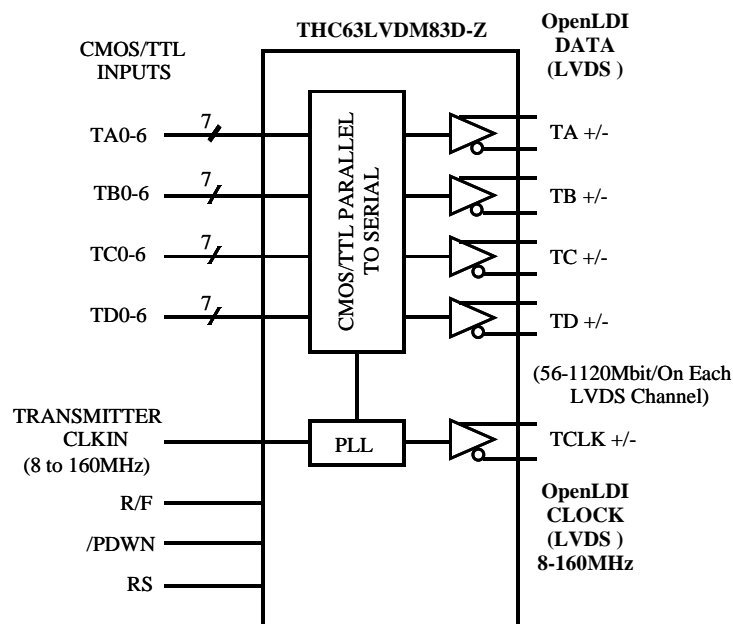
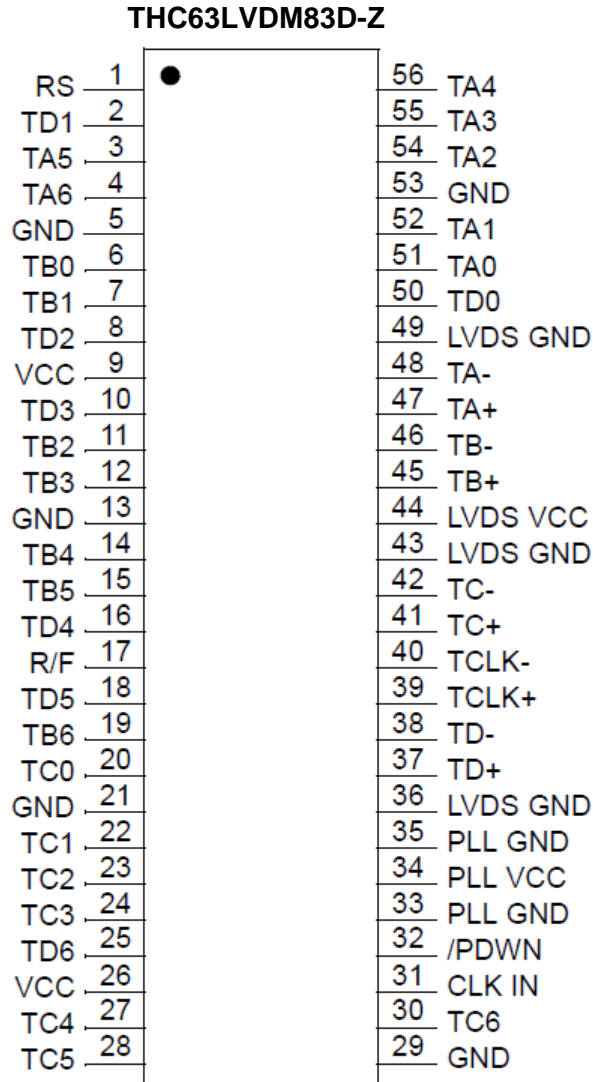


Figure 1. Block Diagram

## Pin Diagram



**Figure 2. Pin Diagram**

### Pin Description

| Pin Name                          | Pin #                      | Direction   | Type   | Description  |            |                           |                           |     |       |     |             |       |         |            |       |     |
|-----------------------------------|----------------------------|---|--------|--|------------|---------------------------|---------------------------|-----|-------|-----|-------------|-------|---------|------------|-------|-----|
| TA+, TA-                          | 47, 48                     | Output  | LVDS   | Open LDI(LVDS) Data Out  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| TB+, TB-                          | 45, 46                     |   |        |  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| TC+, TC-                          | 41, 42                     |   |        |  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| TD+, TD-                          | 37, 38                     |   |        |  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| TCLK+, TCLK-                      | 39, 40                     |   |        | Open LDI(LVDS) Clock Out   |            |                           |                           |     |       |     |             |       |         |            |       |     |
| TA0 ~ TA6                         | 51, 52, 54, 55, 56, 3, 4   | Input   | LVCMOS | Pixel Data Input   |            |                           |                           |     |       |     |             |       |         |            |       |     |
| TB0 ~ TB6                         | 6, 7, 11, 12, 14, 15, 19   |   |        |  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| TC0 ~ TC6                         | 20, 22, 23, 24, 27, 28, 30 |   |        |  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| TD0 ~ TD6                         | 50, 2, 8, 10, 16, 18, 25   |   |        |  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| /PDWN                             | 32                         |   |        | H : Normal Operation<br>L : Power Down (All outputs are Hi-Z)  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| RS                                | 1                          |   |        | LVDS Swing Mode, VREF Select See Fig.7, 8  |            |                           |                           |     |       |     |             |       |         |            |       |     |
|                                   |                            |   |        | <table><tr><td>RS</td><td>LVDS Swing</td><td>Small Swing Input Support</td></tr><tr><td>VCC</td><td>350mV</td><td>N/A</td></tr><tr><td>0.6V ~ 1.4V</td><td>350mV</td><td>RS=VREF</td></tr><tr><td>GND ~ 0.2V</td><td>200mV</td><td>N/A</td></tr></table> | RS         | LVDS Swing                | Small Swing Input Support | VCC | 350mV | N/A | 0.6V ~ 1.4V | 350mV | RS=VREF | GND ~ 0.2V | 200mV | N/A |
|                                   |                            |   |        | RS   | LVDS Swing | Small Swing Input Support |                           |     |       |     |             |       |         |            |       |     |
|                                   |                            |   |        | VCC  | 350mV      | N/A                       |                           |     |       |     |             |       |         |            |       |     |
|                                   |                            |   |        | 0.6V ~ 1.4V  | 350mV      | RS=VREF                   |                           |     |       |     |             |       |         |            |       |     |
| GND ~ 0.2V                        | 200mV                      | N/A   |        |  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| VREF : is Input Reference Voltage |                            |   |        |  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| R/F                               | 17                         | Input Clock Triggering Edge Select<br>H : Rising Edge<br>L : Falling Edge |        |  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| CLKIN                             | 31                         | Input Clock   |        |  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| VCC                               | 9, 26                      | Power   | -      | Power Supply Pins for LVCMOS inputs and digital circuit.   |            |                           |                           |     |       |     |             |       |         |            |       |     |
| GND                               | 5, 13, 21, 29, 53          |   |        | Ground Pins for LVCMOS Inputs and Digital Circuitry.   |            |                           |                           |     |       |     |             |       |         |            |       |     |
| LVDS VCC                          | 44                         |   |        | Power Supply Pins for LVDS Outputs.  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| LVDS GND                          | 36, 43 49                  |   |        | Ground Pins for LVDS Outputs.  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| PLL VCC                           | 34                         |   |        | Power Supply Pin for PLL Circuitry.  |            |                           |                           |     |       |     |             |       |         |            |       |     |
| PLL GND                           | 33, 35                     |   |        | Ground Supply Pin for PLL Circuitry.   |            |                           |                           |     |       |     |             |       |         |            |       |     |

**Table 1. Pin Description**

### Absolute Maximum Ratings

| Parameter                                   | Min  | Max       | Unit |
|---|------|-----------|------|
| All Supply Voltage (VCC, LVDS_VCC, PLL_VCC) | -0.3 | +4.0      | V    |
| LVC MOS Input Voltage                       | -0.3 | VCC + 0.3 | V    |
| LVDS Output Pin                             | -0.3 | VCC + 0.3 | V    |
| Output Current                              | -30  | 30        | mA   |
| Junction Temperature                        | -    | +125      | °C   |
| Storage Temperature                         | -55  | +150      | °C   |
| Reflow Peak Temperature                     | -    | +260      | °C   |
| Reflow Peak Temperature Time                | -    | 10        | sec  |
| Maximum Power Dissipation @+25°C            | -    | 1.8       | W    |

**Table 2. Absolute Maximum Ratings**

### Recommended Operating Conditions

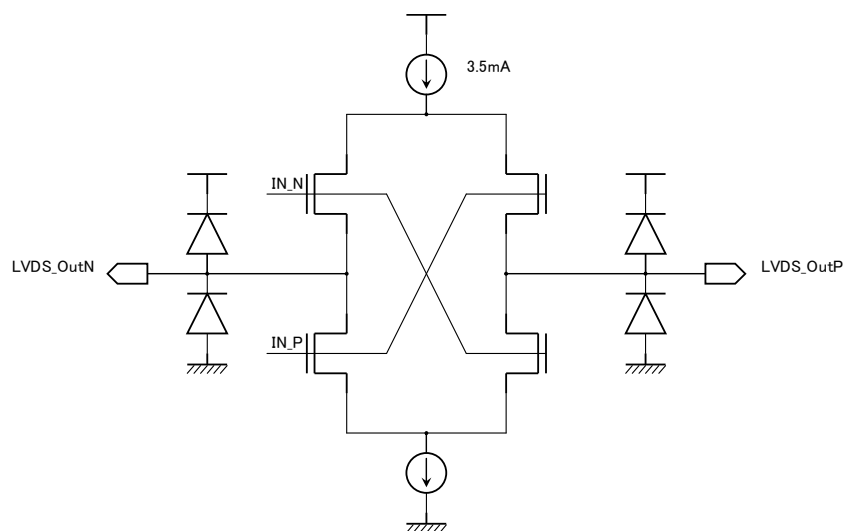
| Symbol                       | Parameter                     | Min | Typ. | Max  | Unit |
|------------------------------|-------------------------------|-----|------|------|------|
| VCC,<br>LVDS_VCC,<br>PLL_VCC | All Supply Voltage            | 3.0 | 3.3  | 3.6  | V    |
| T <sub>a</sub>               | Operating Ambient Temperature | -40 | 25   | +105 | °C   |
| f <sub>clk</sub>             | Clock Frequency               | 8   | -    | 160  | MHz  |

**Table 3. Recommended Operating Conditions**

“Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics Table 4, 5, 6, 7” specify conditions for device operation.

“Absolute Maximum Rating” value also includes behavior of overshooting and undershooting.

### Equivalent LVDS Output Schematic Diagram



**Figure 3. LVDS Output Schematic Diagram**

## Power Consumption

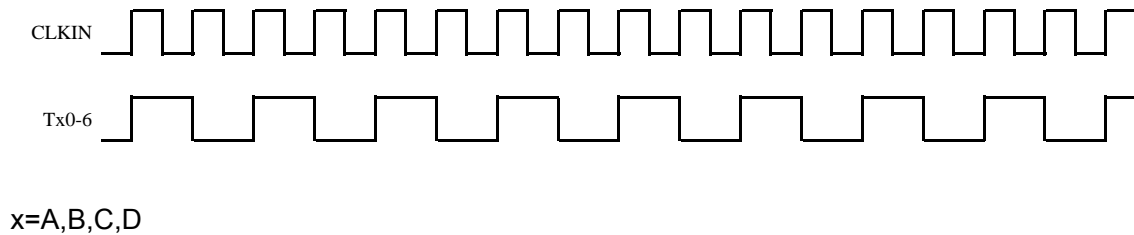
Over recommended operating supply and temperature range unless otherwise specified

| Symbol     | Parameter   | Conditions                        | Typ.* | Max | Unit |
|------------|---|-----------------------------------|-------|-----|------|
| $I_{TCCW}$ | LVDS Transmitter Operating Current Worst Case Pattern (Fig.4) | RL=100Ω, CL=5pF, f=85MHz, RS=VCC  | 48    | 67  | mA   |
|            |   | RL=100Ω, CL=5pF, f=135MHz, RS=VCC | 65    | 83  | mA   |
|            |   | RL=100Ω, CL=5pF, f=160MHz, RS=VCC | 73    | 92  | mA   |
|            |   | RL=100Ω, CL=5pF, f=85MHz, RS=GND  | 40    | 56  | mA   |
|            |   | RL=100Ω, CL=5pF, f=135MHz, RS=GND | 56    | 71  | mA   |
|            |   | RL=100Ω, CL=5pF, f=160MHz, RS=GND | 65    | 80  | mA   |
| $I_{TCCS}$ | LVDS Transmitter Power Down Current                           | /PDWN=L, All Inputs=L or H        | -     | 10  | μA   |

\*Typ. values are at the conditions of VCC=3.3V and Ta = +25°C

**Table 4. Power Consumption**

## Worst Case Pattern



**Figure 4. Worst Case Pattern**

## Electrical Characteristics

### LVC MOS DC Specifications

Over recommended operating supply and temperature range unless otherwise specified

| Symbol      | Parameter                            | Conditions                     | Min                 | Typ.*       | Max                 | Unit    |
|-------------|--------------------------------------|--------------------------------|---------------------|-------------|---------------------|---------|
| $V_{IH}$    | High Level Input Voltage             | RS=VCC or GND                  | 2.0                 | -           | VCC                 | V       |
| $V_{IL}$    | Low Level Input Voltage              | RS=VCC or GND                  | GND                 | -           | 0.8                 | V       |
| $V_{DDQ}^1$ | Small Swing Voltage                  | -                              | 1.2                 | -           | 2.8                 | V       |
| $V_{REF}$   | Input Reference Voltage              | Small Swing (RS= $V_{DDQ}/2$ ) | -                   | $V_{DDQ}/2$ | -                   |         |
| $V_{SH}^2$  | Small Swing High Level Input Voltage | $V_{REF} = V_{DDQ}/2$          | $V_{DDQ}/2 + 150mV$ | -           | -                   | V       |
| $V_{SL}^2$  | Small Swing Low Level Input Voltage  | $V_{REF} = V_{DDQ}/2$          | -                   | -           | $V_{DDQ}/2 - 150mV$ | V       |
| $I_{IN}$    | Input Current                        | $GND \leq V_{IN} \leq VCC$     | -                   | -           | $\pm 10$            | $\mu A$ |

\*Typ. values are at the conditions of VCC=3.3V and Ta = +25°C

Notes : <sup>1</sup>  $V_{DDQ}$  voltage defines the max voltage of small swing inputs at RS=VREF. It is not an actual input voltage.

<sup>2</sup> Small swing signals are applied to TA0-6, TB0-6, TC0-6, TD0-6 and CLKIN.

**Table 5. LV-CMOS DC Specifications**

### LVDS Transmitter DC Specifications

Over recommended operating supply and temperature range unless otherwise specified

| Symbol       | Parameter   | Conditions                        | Min   | Typ.* | Max      | Unit    |
|--------------|---|-----------------------------------|-------|-------|----------|---------|
| VOD          | Differential Output Voltage                       | Normal swing<br>RS=VCC<br>Ta=25°C | 250   | 350   | 450      | mV      |
|              |   | Reduced swing<br>RS=GND           | 110   | 200   | 300      | mV      |
| $\Delta VOD$ | Change in VOD between complementary output states | RL=100Ω                           | -     | -     | 35       | mV      |
| VOC          | Common Mode Voltage                               | RL=100Ω, Ta=25°C, RS=VCC          | 1.125 | 1.25  | 1.375    | V       |
| $\Delta VOC$ | Change in VOC between complementary output states | RL=100Ω                           | -     | -     | 35       | mV      |
| $I_{OS}$     | Output Short Circuit Current                      | $V_{OUT} = GND$ , RL=100Ω         | -     | -     | -24      | mA      |
| $I_{OZ}$     | Output TRI-STATE Current                          | /PDWN=GND, $V_{OUT} = GND$ to VCC | -     | -     | $\pm 10$ | $\mu A$ |

\*Typ. values are at the conditions of VCC=3.3V and Ta = +25°C

**Table 6. LVDS Transmitter DC Specifications**

## LVC MOS & LVDS Transmitter AC Specifications

Over recommended operating supply and temperature range unless otherwise specified

| Symbol     | Parameter  | Min            | Typ. | Max            | Unit |
|------------|--|----------------|------|----------------|------|
| $t_{TCIT}$ | CLK IN Transition Time                             | -              | -    | 5.0            | ns   |
| $t_{TCP}$  | CLK IN Period                                      | 6.25           | T    | 125            | ns   |
| $t_{TCH}$  | CLK IN High Time                                   | 0.35T          | 0.5T | 0.65T          | ns   |
| $t_{TCL}$  | CLK IN Low Time                                    | 0.35T          | 0.5T | 0.65T          | ns   |
| $t_{TCD}$  | CLK IN to TCLK+/- Delay                            | 3T             | -    | 3T+4           | ns   |
| $t_{TS}$   | LVC MOS Data Setup to CLK IN                       | 2.0            | -    | -              | ns   |
| $t_{TH}$   | LVC MOS Data Hold from CLK IN                      | 0.0            | -    | -              | ns   |
| $t_{LVT}$  | LVDS Transition Time                               | -              | 0.6  | 1.5            | ns   |
| $t_{sk}$   | Output Skew Accuracy(T=11.76ns)                    | -              | 120  | 275            | ps   |
|            | Output Skew Accuracy(T=11.76ns)<br>(3.2V≤VCC≤3.6V) | -              | 120  | 250            | ps   |
|            | Output Skew Accuracy(T=7.4ns)                      | -              | 120  | 250            | ps   |
| $t_{Top1}$ | Output Data Position0 (T=6.25ns ~ 20ns)            | - $t_{sk}$     | 0.0  | + $t_{sk}$     | ns   |
| $t_{Top0}$ | Output Data Position1 (T=6.25ns ~ 20ns)            | T/7- $t_{sk}$  | T/7  | T/7+ $t_{sk}$  | ns   |
| $t_{Top6}$ | Output Data Position2 (T=6.25ns ~ 20ns)            | 2T/7- $t_{sk}$ | 2T/7 | 2T/7+ $t_{sk}$ | ns   |
| $t_{Top5}$ | Output Data Position3 (T=6.25ns ~ 20ns)            | 3T/7- $t_{sk}$ | 3T/7 | 3T/7+ $t_{sk}$ | ns   |
| $t_{Top4}$ | Output Data Position4 (T=6.25ns ~ 20ns)            | 4T/7- $t_{sk}$ | 4T/7 | 4T/7+ $t_{sk}$ | ns   |
| $t_{Top3}$ | Output Data Position5 (T=6.25ns ~ 20ns)            | 5T/7- $t_{sk}$ | 5T/7 | 5T/7+ $t_{sk}$ | ns   |
| $t_{Top2}$ | Output Data Position6 (T=6.25ns ~ 20ns)            | 6T/7- $t_{sk}$ | 6T/7 | 6T/7+ $t_{sk}$ | ns   |
| $t_{TPLL}$ | Phase Lock Loop Set                                | -              | -    | 1.0            | ms   |

\*Typ. values are at the conditions of VCC=3.3V and Ta = +25°C

Table 7. LVC MOS & LVDS Transmitter AC Specifications

### LVC MOS Input

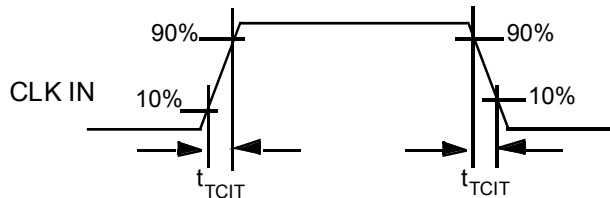
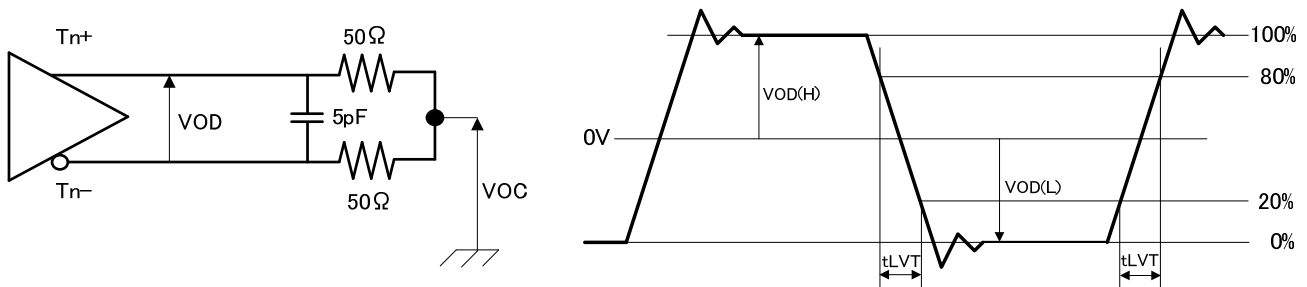


Figure 5. CLKIN Transmission Time

### OpenLDI(LVDS) Output

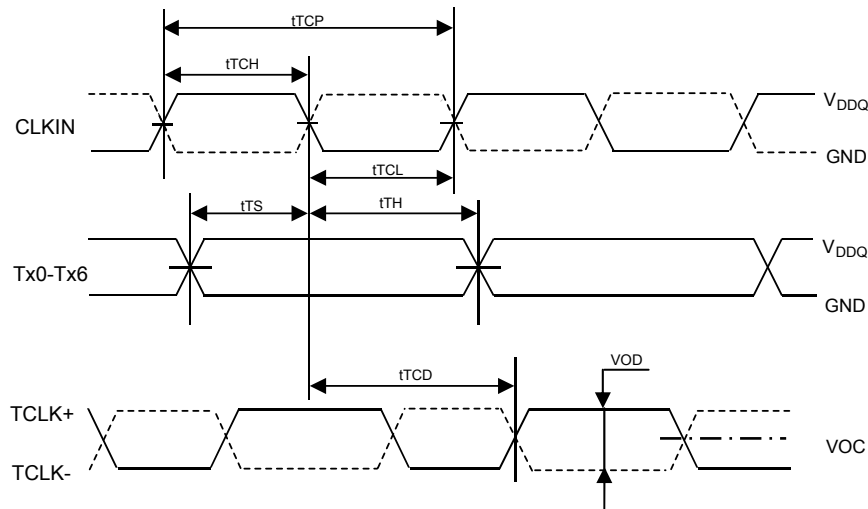


### LVDS Output Load

Figure 6. LVDS Output Load and Transmission Time

## AC Timing Diagrams

### LVCMOS Inputs



| RS          | VOD   |
|-------------|-------|
| VCC         | 350mV |
| 0.6V ~ 1.4V |       |
| GND ~ 0.2V  | 200mV |

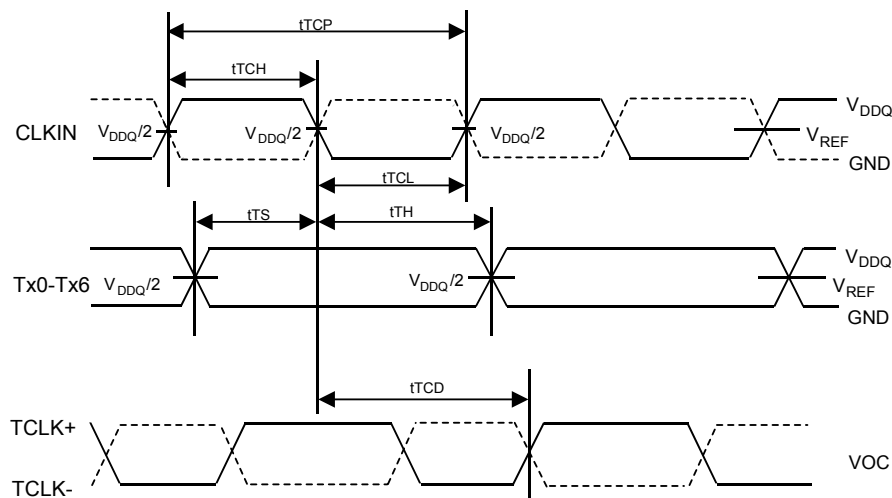
Note :

CLKIN : Solid line denotes the setting of R/F=GND

Dashed line denotes the setting of R/F = VCC

**Figure 7. LVCOMS Inputs and LVDS Clock Output Timing 1**

### Small Swing Inputs



| RS          | VREF   |
|-------------|--------|
| VCC         | --     |
| 0.6V ~ 1.4V | VDDQ/2 |
| GND ~ 0.2V  | --     |

Note :

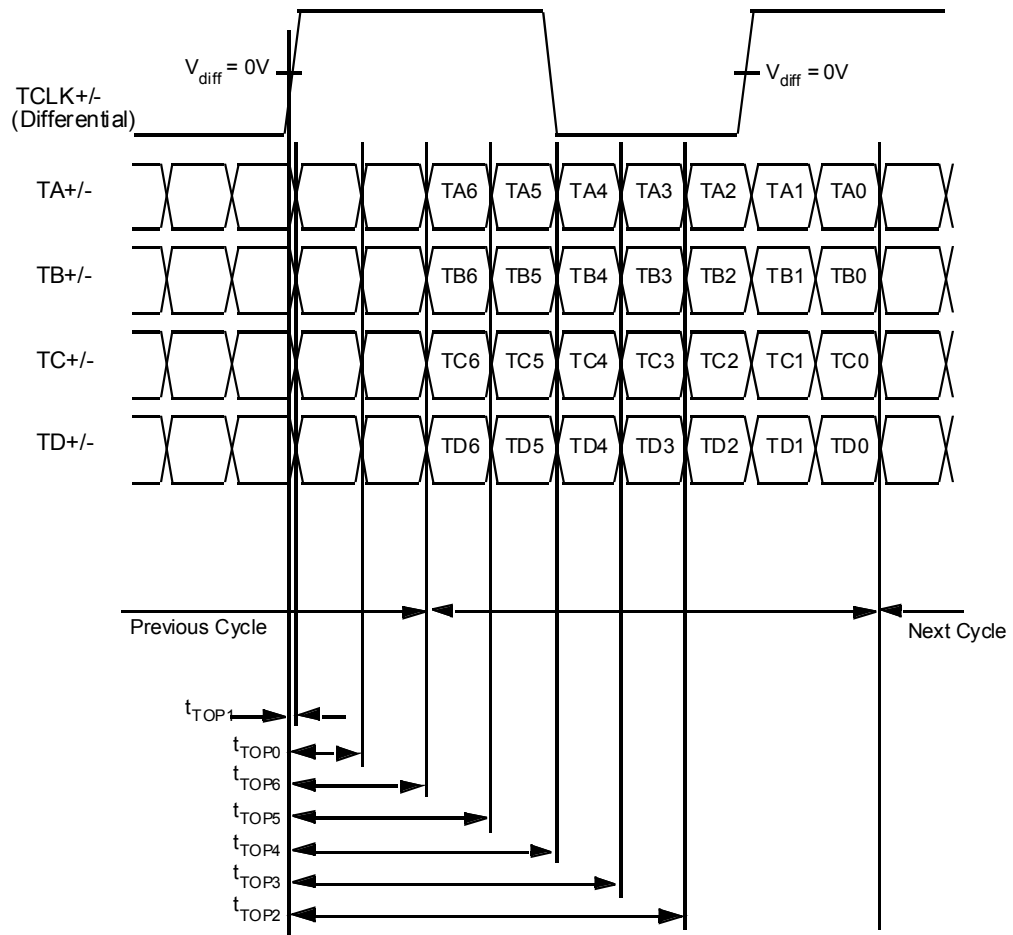
CLKIN : Solid line denotes the setting of R/F=GND

Dashed line denotes the setting of R/F = VCC

**Figure 8. LVCMOS Inputs and LVDS Output Timing 2**

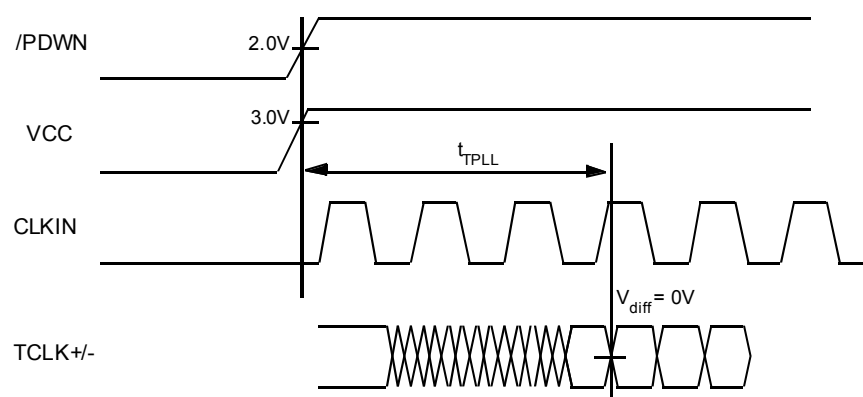


## OpenLDI(LVDS) Output Data Position



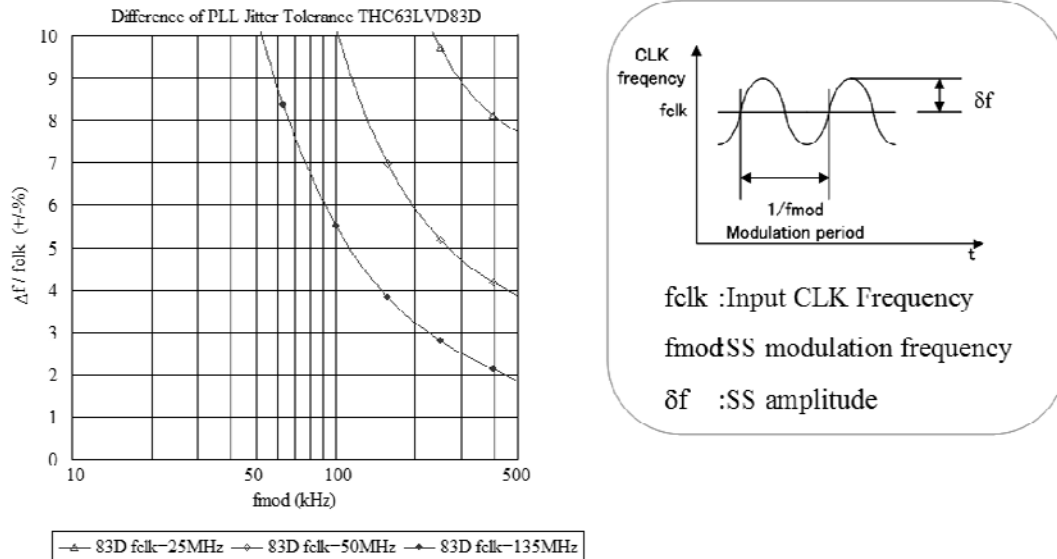
**Figure 9. LVDS Output Data Position**

## Phase Lock Loop Set Time



**Figure 10. PLL Lock Loop Set Time**

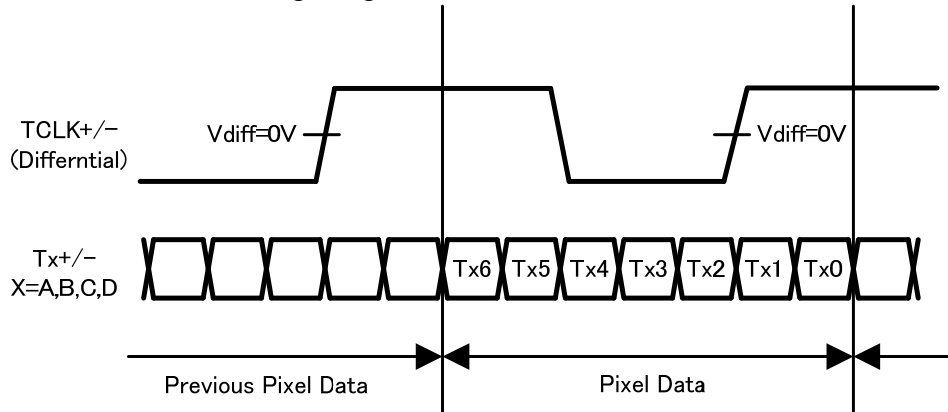
## Spread Spectrum Clocking Tolerant



**Figure 11. Spread Spectrum Clocking Tolerant**

The graph indicates the range that the IC works normally under SS clock input operation. The results are measured with a typical sample on condition of +25°C and 3.3V, therefore these values are for reference and do not guarantee the performance of a product under other circumstance.

## OpenLDI(LVDS) Data Timing Diagram



**Figure 12. LVDS Data Timing Diagram**

## THC63LVDM83D-Z Pixel Data Mapping for JEIDA Format (6bit, 8bit Application)

|     | 6bit  | 8bit  |
|-----|-------|-------|
| TA0 | R2    | R2    |
| TA1 | R3    | R3    |
| TA2 | R4    | R4    |
| TA3 | R5    | R5    |
| TA4 | R6    | R6    |
| TA5 | R7    | R7    |
| TA6 | G2    | G2    |
| TB0 | G3    | G3    |
| TB1 | G4    | G4    |
| TB2 | G5    | G5    |
| TB3 | G6    | G6    |
| TB4 | G7    | G7    |
| TB5 | B2    | B2    |
| TB6 | B3    | B3    |
| TC0 | B4    | B4    |
| TC1 | B5    | B5    |
| TC2 | B6    | B6    |
| TC3 | B7    | B7    |
| TC4 | Hsync | Hsync |
| TC5 | Vsync | Vsync |
| TC6 | DE    | DE    |
| TD0 | -     | R0    |
| TD1 | -     | R1    |
| TD2 | -     | G0    |
| TD3 | -     | G1    |
| TD4 | -     | B0    |
| TD5 | -     | B1    |
| TD6 | -     | N/A   |

Note : Use TA to TC channels and open TD channel for 6bit application.

**Table 8. Data Mapping for JEIDA Format**

THC63LVDM83D-Z Pixel Data Mapping for VESA Format (6bit, 8bit Application)

|     | 6bit  | 8bit  |
|-----|-------|-------|
| TA0 | R0    | R0    |
| TA1 | R1    | R1    |
| TA2 | R2    | R2    |
| TA3 | R3    | R3    |
| TA4 | R4    | R4    |
| TA5 | R5    | R5    |
| TA6 | G0    | G0    |
| TB0 | G1    | G1    |
| TB1 | G2    | G2    |
| TB2 | G3    | G3    |
| TB3 | G4    | G4    |
| TB4 | G5    | G5    |
| TB5 | B0    | B0    |
| TB6 | B1    | B1    |
| TC0 | B2    | B2    |
| TC1 | B3    | B3    |
| TC2 | B4    | B4    |
| TC3 | B5    | B5    |
| TC4 | Hsync | Hsync |
| TC5 | Vsync | Vsync |
| TC6 | DE    | DE    |
| TD0 | -     | R6    |
| TD1 | -     | R7    |
| TD2 | -     | G6    |
| TD3 | -     | G7    |
| TD4 | -     | B6    |
| TD5 | -     | B7    |
| TD6 | -     | N/A   |

Note : Use TA to TC channels and open TD channel for 6bit application.

**Table 9. Data Mapping for VESA Format**

## Normal Connection

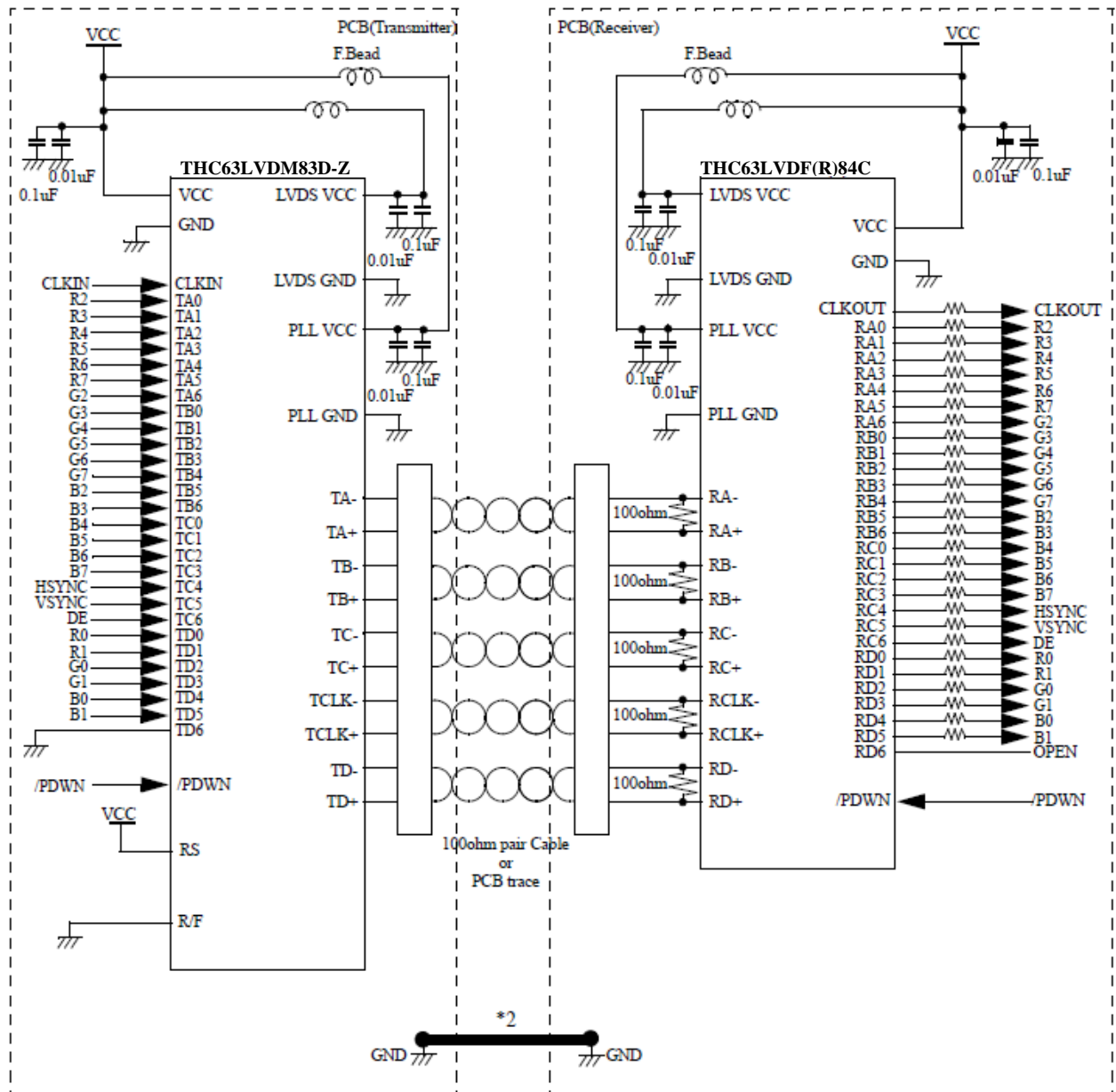


Figure 13. Typical Connection Diagram

## Notes

### 1) Cable Connection and Disconnection

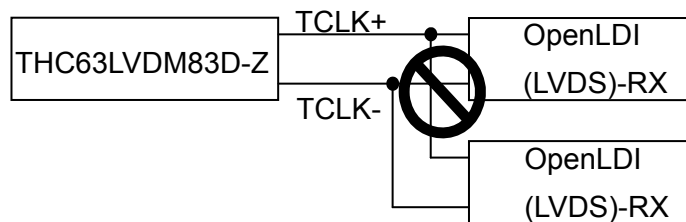
Do not connect and disconnect the OpenLDI(LVDS) cable, when the power is supplied to the system.

### 2) GND Connection

Connect each GND of the PCB which THC63LVDM83D-Z and OpenLDI(LVDS)-Rx on it. It is better for EMI reduction to place GND cable as close to OpenLDI(LVDS) cable as possible.

### 3) Multi Drop Connection

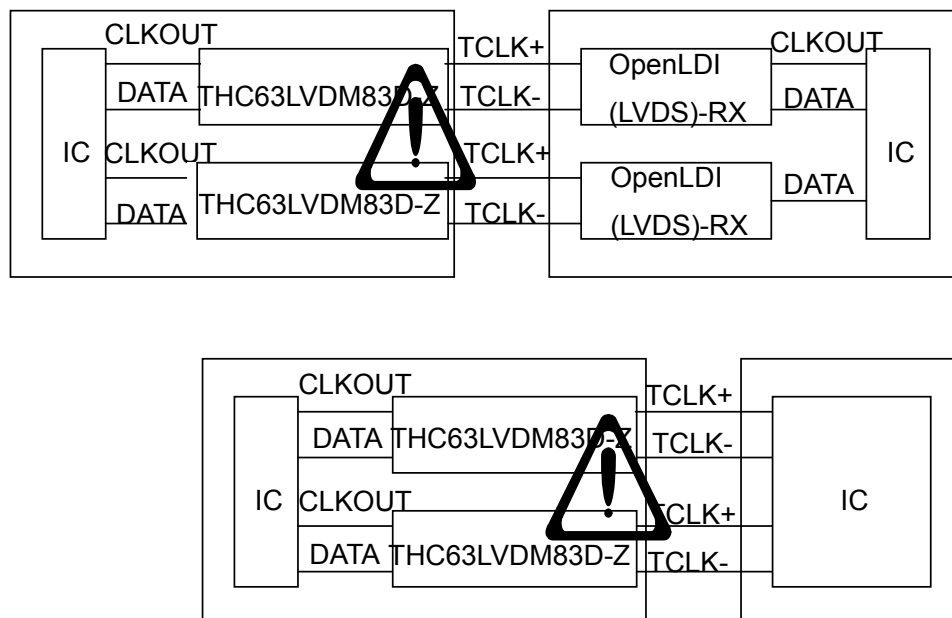
Multi drop connection is not recommended.



**Figure 14. Multi Drop Connection**

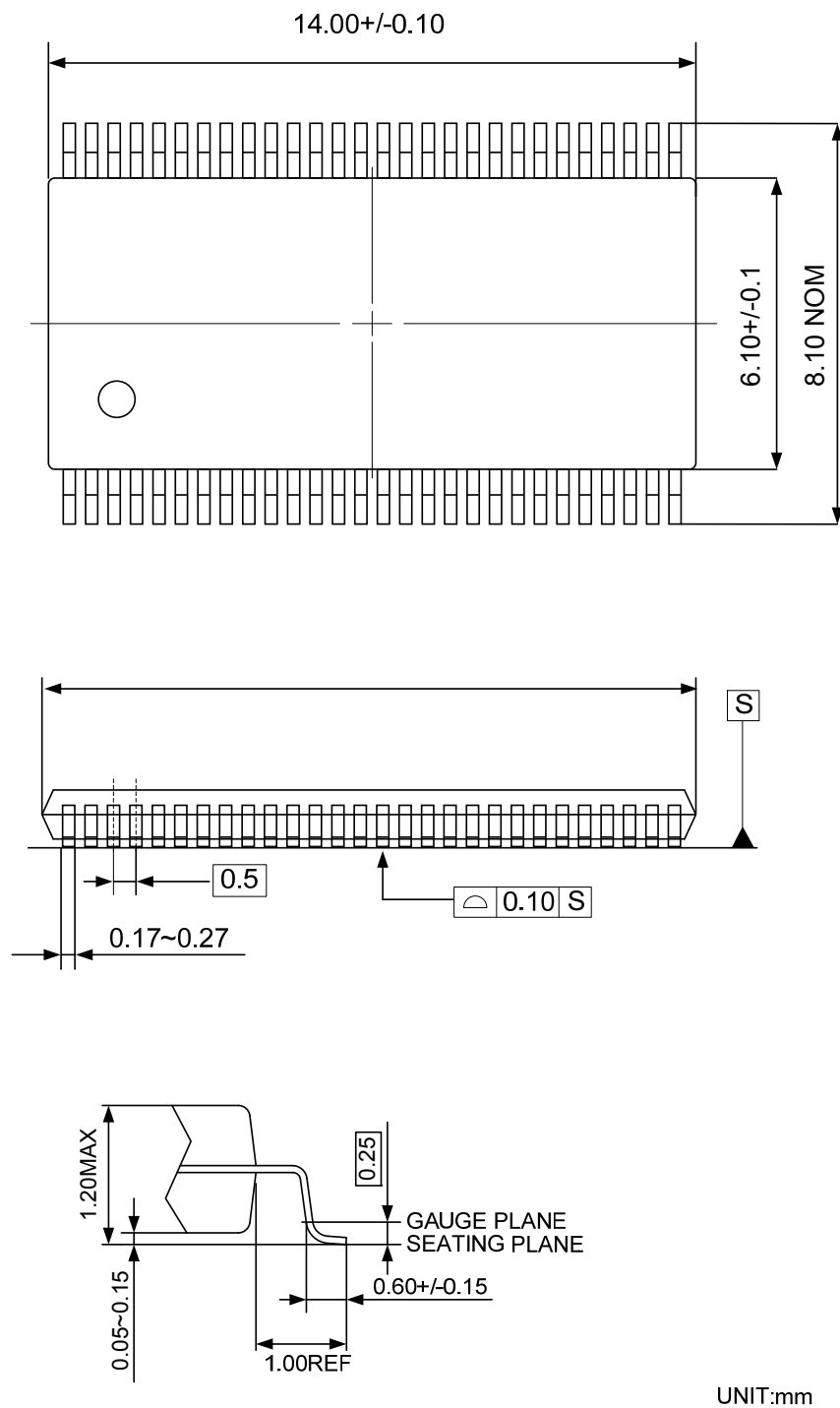
### 4) Asynchronous use

Asynchronous using such as following systems is not recommended.



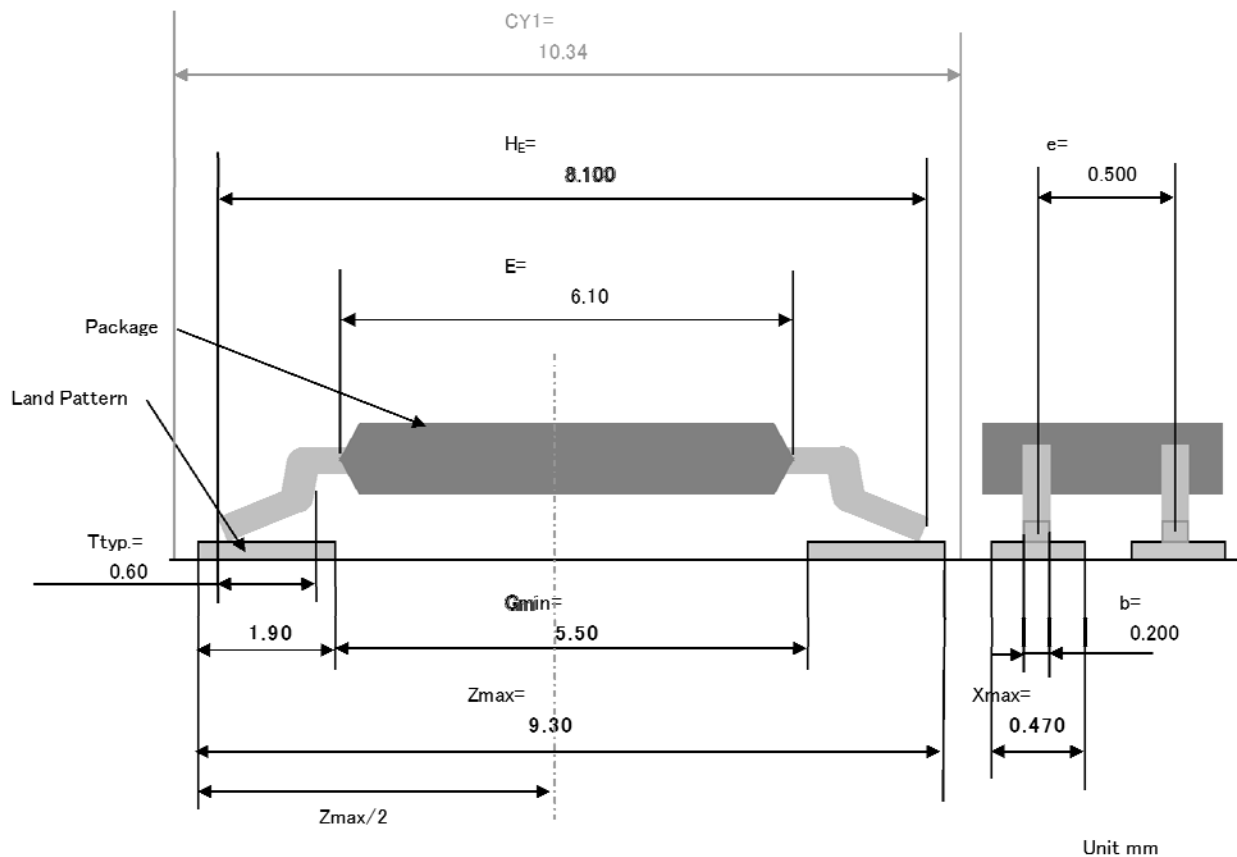
**Figure 15. Asynchronous Use**

## Package



**Figure 16. Package Diagram**

## Reference Land Pattern



**Figure 17. Reference of Land Pattern**

The recommendation mounting method of THine device is reflow soldering.  
The reference pattern is using the calculation result on condition of reflow soldering.

### Notes

This land pattern design is a calculated value based on JEITA ET-7501.

Please take into consideration in an actual substrate design about enough the ease of mounting, the intensity of connection, the density of mounting, and the solder paste used, etc... The optimal land pattern size changes with these parameters. Please use the value shown by the land pattern as reference data.



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## **Notices and Requests**

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.
5. Product Application
  - 5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
  - 5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of ISO/TS16949 ("the Specified Product") in this data sheet. THine Electronics, Inc. ("THine") accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.
  - 5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.
6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.
9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.
10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

***THine Electronics, Inc.***

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# Mouser Electronics

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