

Click [here](#) for production status of specific part numbers.

## MAXM17633/MAXM17634/ MAXM17635

## 4.5V to 36V, 2A Himalaya uSLIC Step-Down Power Modules

### General Description

The Himalaya series of voltage regulator ICs and power modules enable cooler, smaller, and simpler power supply solutions. The MAXM17633, MAXM17634, and MAXM17635 are a family of high-frequency synchronous step-down DC-DC converter modules with integrated controller, MOSFETs, compensation components, and inductor, that operate over a wide input voltage range. The modules operate from 4.5V to 36V input and deliver up to 2A output current. MAXM17633 and MAXM17634 are fixed 3.3V and 5V output modules, respectively. The MAXM17635 is an adjustable-output voltage (0.9V to 12V) module. The modules significantly reduce design complexity, manufacturing risks, and offer a true plug-and-play power supply solution, reducing time to market.

The MAXM17633/MAXM17634/MAXM17635 modules employ peak-current-mode control architecture. To reduce input inrush current, the devices offer a programmable soft-start time.

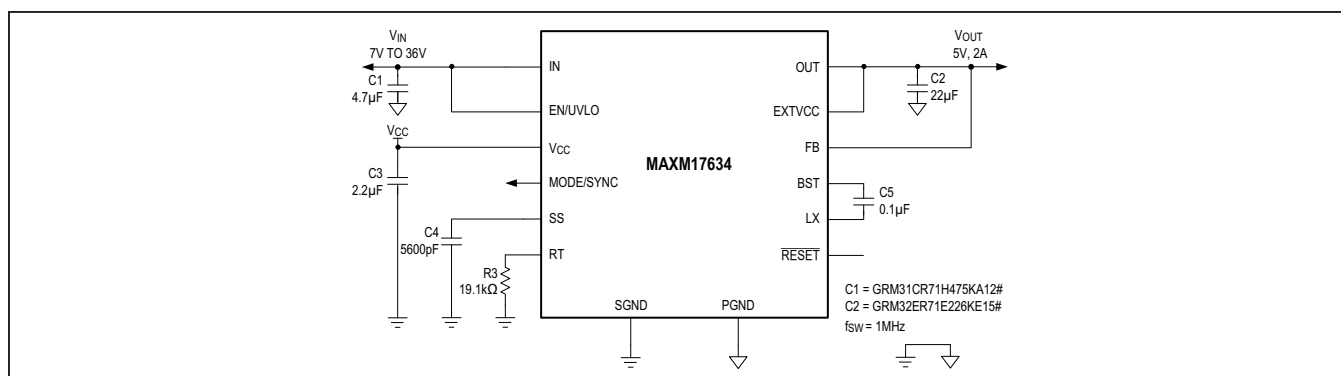
The MAXM17633/MAXM17634/MAXM17635 modules are available in a low profile, compact 24-pin, 4mm x 4mm x 1.75mm, uSLIC™ package.

### Applications

- Industrial Control Power Supplies
- General-Purpose Point-of-Load
- Distributed Supply Regulation
- Base Station Power Supplies
- Programmable Logic Controller
- High Voltage Single-Board Systems

**Ordering Information** appears at end of data sheet.

### Typical Application Circuit



uSLIC is a trademark of Maxim Integrated Products, Inc.

### Benefits and Features

- Easy to Use
  - Wide 4.5V to 36V Input
  - Adjustable 0.9V to 12V Output (MAXM17635)
  - Fixed 3.3V and 5V Output Versions (MAXM17633 and MAXM17634)
  - 400kHz to 2.2MHz Adjustable Frequency with External Clock Synchronization
  - $\pm 1.2\%$  Feedback Accuracy
  - Up to 2A Output Current
  - Internally Compensated
  - All Ceramic Capacitors
- High Efficiency
  - Selectable PWM, PFM, or DCM Mode of Operation
  - Shutdown Current as Low as 2.8µA (typ)
- Flexible Design
  - Programmable Soft-Start and Prebias Startup
  - Open-Drain Power Good Output (RESET Pin)
  - Programmable EN/UVLO Threshold
- Robust Operation
  - Hiccup Overcurrent Protection
  - Overtemperature Protection
  - $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Ambient Operating Temperature/  
 $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$  Junction Temperature
- Rugged
  - Complies with CISPR22(EN55022) Class B Conducted and Radiated Emissions
  - Passes Drop, Shock, and Vibration Standards: JESD22-B103, B104, B111

# MAXM17633/MAXM17634/ MAXM17635

## 4.5V to 36V, 2A Himalaya uSLIC Step-Down Power Modules

### Absolute Maximum Ratings

IN to PGND .....-0.3V to +40V  
EN/UVLO to SGND .....-0.3V to ( $V_{IN} + 0.3V$ )  
LX, OUT to PGND .....-0.3V to ( $V_{IN} + 0.3V$ )  
EXTVCC to SGND .....-5.5V to +6.5V  
BST to PGND .....-0.3V to +46.5V  
BST to LX .....-0.3V to +6.5V  
BST to  $V_{CC}$  .....-0.3V to +40V  
FB to SGND (MAXM17633 and MAXM17634) ....-5.5V to +6.5V  
FB to SGND (MAXM17635) .....-0.3V to +6.5V

SS, MODE/SYNC,  $\overline{\text{RESET}}$ ,  $V_{CC}$ , RT to SGND ..-0.3V to +6.5V  
PGND to SGND .....-0.3V to +0.3V  
Output Short-Circuit Duration .....Continuous  
Operating Temperature Range (Note 1)..... -40°C to +125°C  
Junction Temperature ..... -40°C to +150°C  
Storage Temperature Range ..... -65°C to +150°C  
Lead Temperature (soldering, 10s) .....+260°C  
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Package Information

PACKAGE TYPE: 24-PIN uSLIC	
Package Code	M244A4+1
Outline Number	<a href="#">21-100342</a>
Land Pattern Number	<a href="#">90-100115</a>
THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2)	
Junction to Ambient ( $\theta_{JA}$ )	25°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

**Note 1:** Junction temperature greater than +125°C degrades operating lifetimes.

**Note 2:** Package thermal resistance is measured on an evaluation board with natural convection.

### Electrical Characteristics

( $V_{IN} = V_{EN/UVLO} = 24V$ ,  $R_{RT} = \text{Unconnected}$ ,  $C_{VCC} = 2.2\mu F$ ,  $V_{SGND} = V_{PGND} = V_{MODE/SYNC} = V_{EXTVCC} = 0V$ ;  $V_{FB} = 3.67V$  (MAXM17633),  $V_{FB} = 5.5V$  (MAXM17634),  $V_{FB} = 1V$  (MAXM17635), LX = SS =  $\overline{\text{RESET}} = \text{OPEN}$ ,  $V_{BST}$  to  $V_{LX} = 5V$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ . All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY ( $V_{IN}$ )						
Input Voltage Range	$V_{IN}$		4.5		36	V
Input Shutdown Current	$I_{IN-SH}$	$V_{EN/UVLO} = 0V$ (shutdown mode)		2.8	4.5	$\mu A$
Input Quiescent Current	$I_{Q\_PFM}$	$R_{RT} = 19.1k\Omega$ , MODE/SYNC = OPEN, $V_{EXTVCC} = 5V$		110		$\mu A$
	$I_{Q\_DCM}$	$R_{RT} = 19.1k\Omega$ , MODE/SYNC = $V_{CC}$ , $V_{EXTVCC} = 5V$		710		
	$I_{Q\_PWM}$	$R_{RT} = 19.1k\Omega$ , MODE/SYNC = SGND, $V_{EXTVCC} = 5V$		13		mA

MAXM17633/MAXM17634/  
MAXM17635

4.5V to 36V, 2A Himalaya uSLIC  
Step-Down Power Modules

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE/UVLO (EN/UVLO)						
EN Threshold	V <sub>ENR</sub>	V <sub>EN/UVLO</sub> rising	1.19	1.215	1.26	V
	V <sub>ENF</sub>	V <sub>EN/UVLO</sub> falling	1.068	1.09	1.131	
EN Input Leakage Current	I <sub>EN</sub>	V <sub>EN/UVLO</sub> = 0V, T <sub>A</sub> = +25°C	-50	0	+50	nA
V <sub>CC</sub> (LDO)						
V <sub>CC</sub> Output Voltage Range	V <sub>CC</sub>	1mA ≤ I <sub>VCC</sub> ≤ 25mA	4.75	5	5.25	V
		6V ≤ V <sub>IN</sub> ≤ 36V, I <sub>VCC</sub> = 1mA	4.75	5	5.25	
V <sub>CC</sub> Current Limit	I <sub>VCC-MAX</sub>	V <sub>CC</sub> = 4.5V, V <sub>IN</sub> = 7.5V	30			mA
V <sub>CC</sub> Dropout	V <sub>CC-DO</sub>	V <sub>IN</sub> = 4.5V, I <sub>VCC</sub> = 10mA			0.3	V
V <sub>CC</sub> UVLO	V <sub>VCC_UVR</sub>	V <sub>VCC</sub> rising	4.05	4.2	4.3	V
	V <sub>VCC_UVF</sub>	V <sub>VCC</sub> falling	3.65	3.8	3.9	
EXTVCC						
EXTVCC Switchover Threshold		V <sub>EXTVCC</sub> rising	4.56	4.7	4.84	V
		V <sub>EXTVCC</sub> falling	4.30	4.43	4.60	
SOFT-START (SS)						
Charging Current	I <sub>SS</sub>		4.7	5	5.3	μA
FEEDBACK (FB)						
FB Regulation Voltage	V <sub>FB-REG</sub>	MODE/SYNC = SGND or MODE/SYNC = V <sub>CC</sub> for MAXM17633	3.256	3.3	3.334	V
		MODE/SYNC = SGND or MODE/SYNC = V <sub>CC</sub> for MAXM17634	4.94	5	5.06	
		MODE/SYNC = SGND or MODE/SYNC = V <sub>CC</sub> for MAXM17635	0.888	0.9	0.912	
		MODE/SYNC = OPEN for MAXM17633	3.256	3.36	3.44	
		MODE/SYNC = OPEN for MAXM17634	4.94	5.09	5.21	
		MODE/SYNC = OPEN for MAXM17635	0.888	0.915	0.938	
FB Leakage Current	I <sub>FB</sub>	For MAXM17633		23.2		μA
		For MAXM17634		23.2		
		For MAXM17635, T <sub>A</sub> = +25°C	-50		+50	nA
MODE/SYNC						
MODE Threshold	V <sub>M-DCM</sub>	MODE/SYNC = V <sub>CC</sub> (DCM mode)	V <sub>CC</sub> - 0.65			V
	V <sub>M-PFM</sub>	MODE/SYNC = OPEN (PFM mode)	V <sub>CC</sub> /2			
	V <sub>M-PWM</sub>	MODE/SYNC = SGND (PWM mode)	0.75			

## Electrical Characteristics (continued)

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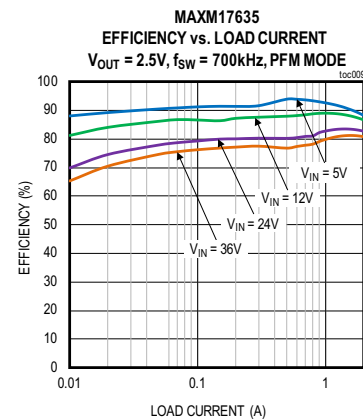
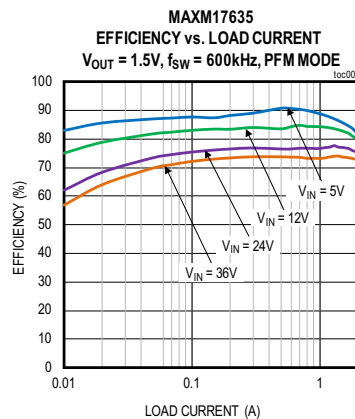
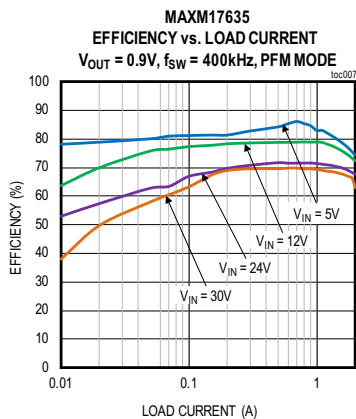
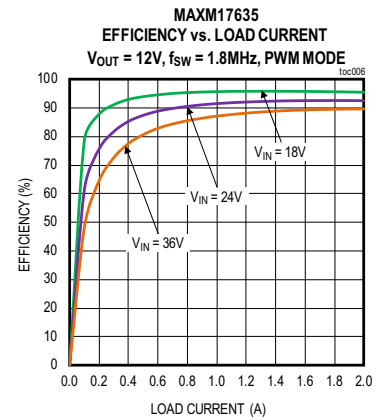
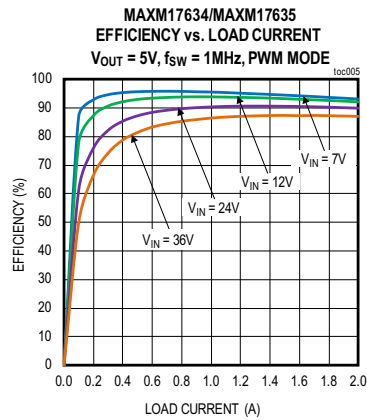
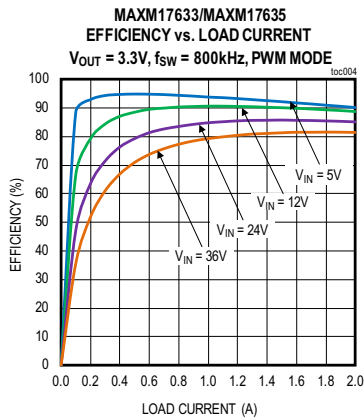
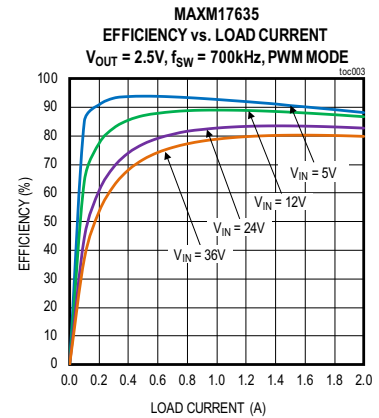
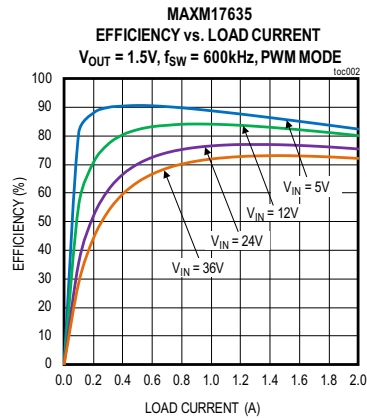
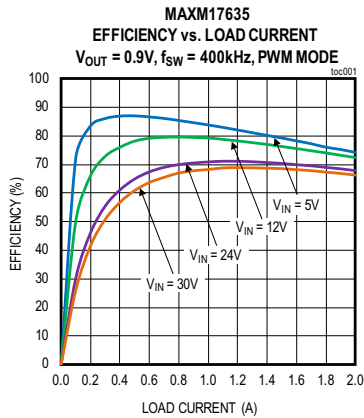
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Frequency Capture Range	f <sub>SYNC</sub>	f <sub>SW</sub> set by R <sub>RT</sub>	1.1 x f <sub>SW</sub>		1.4 x f <sub>SW</sub>	kHz
SYNC Pulse Width			50			ns
SYNC Threshold	V <sub>IH</sub>		2.1			V
	V <sub>IL</sub>			0.8		
RT						
Switching Frequency	f <sub>SW</sub>	R <sub>RT</sub> = 50.8kΩ	380	400	420	kHz
		R <sub>RT</sub> = 40.2kΩ	475	500	525	
		R <sub>RT</sub> = OPEN	460	500	540	
		R <sub>RT</sub> = 8.06kΩ	1950	2200	2450	
V <sub>FB</sub> Undervoltage Trip Level to Cause Hiccup	V <sub>FB-HICF</sub>		61.5	64.4	67.5	%
HICCUP Timeout		(Note 4)		32768		Cycles
Minimum On-Time	t <sub>ON(MIN)</sub>			52	80	ns
Minimum Off-Time	t <sub>OFF(MIN)</sub>		140		160	ns
RESET						
RESET Output Level Low	V <sub>RESETL</sub>	I <sub>RESET</sub> = 10mA			400	mV
RESET Output Leakage Current	I <sub>RESETLKG</sub>	T <sub>A</sub> = T <sub>J</sub> = 25°C, V <sub>RESET</sub> = 5.5V	-100		+100	nA
FB Threshold for RESET Rising	V <sub>FB-OKR</sub>	V <sub>FB</sub> Rising	93.8	95	97.8	%
FB Threshold for RESET Falling	V <sub>FB-OKF</sub>	V <sub>FB</sub> Falling	90.5	92	94.6	%
RESET Delay after FB Reaches Rising Threshold				1024		Cycles
THERMAL SHUTDOWN (TEMP)						
Thermal Shutdown Threshold		Temperature rising		165		°C
Thermal Shutdown Hysteresis				10		°C

**Note 3:** Electrical specifications are production tested at  $T_A = +25^\circ C$ . Specifications over the entire operating temperature range are guaranteed by design and characterization.

**Note 4:** See the [Overcurrent Protection/Hiccup Mode](#) section for more details.

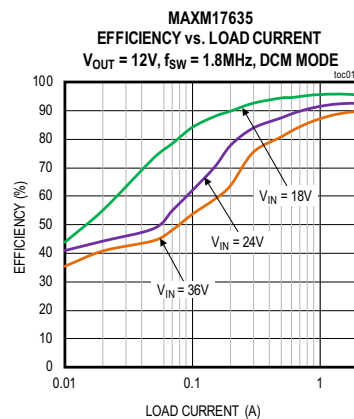
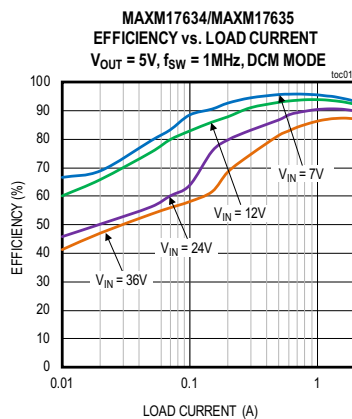
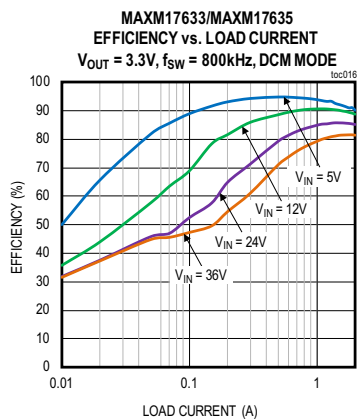
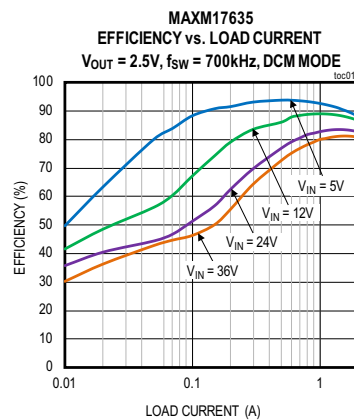
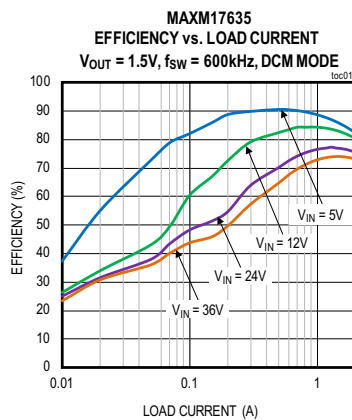
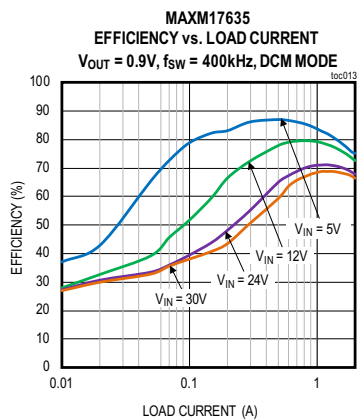
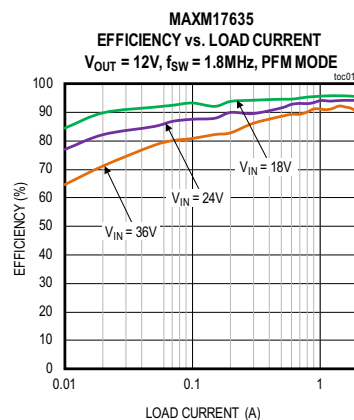
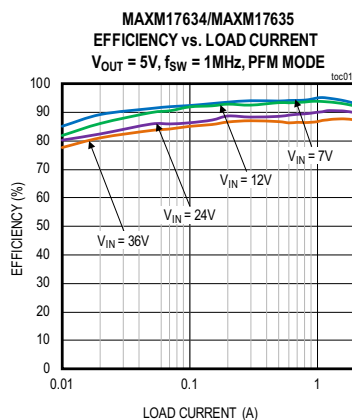
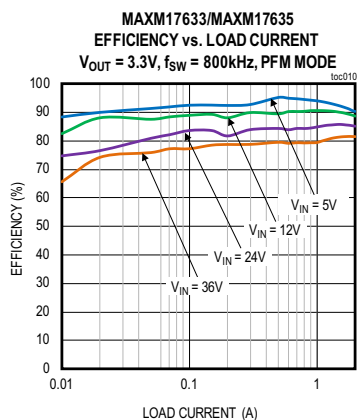
## Typical Operating Characteristics

( $V_{EN}/UVLO = V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{INTVCC} = 2.2\mu F$ ,  $C_{BST} = 0.1\mu F$ ,  $C_{SS} = 5600pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications are as in [Table 1](#), unless otherwise noted.)



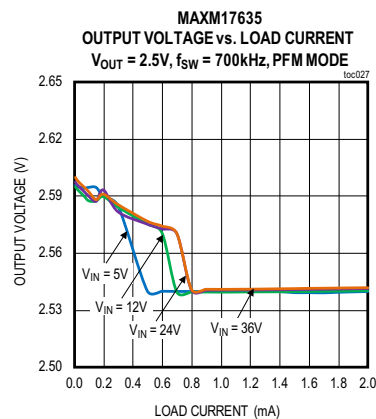
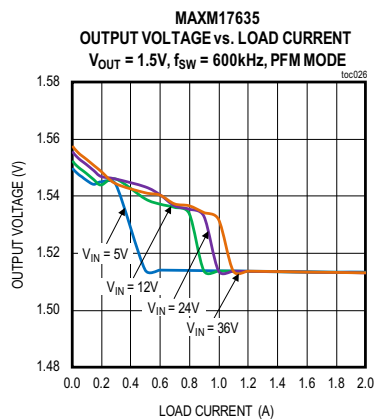
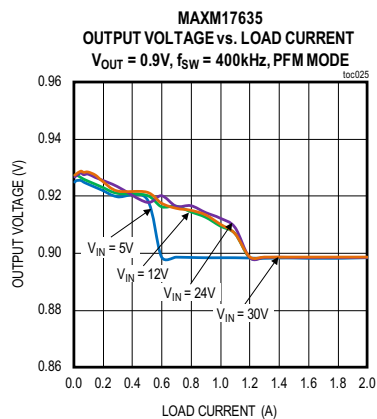
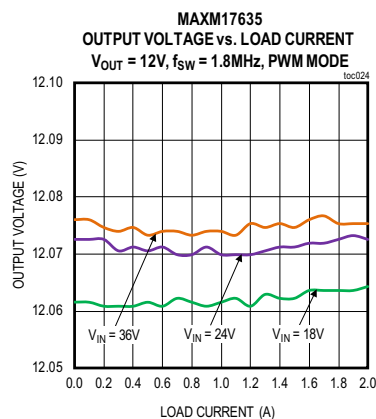
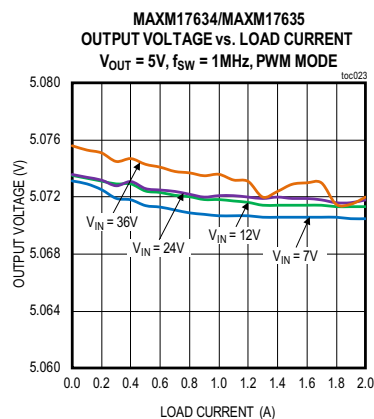
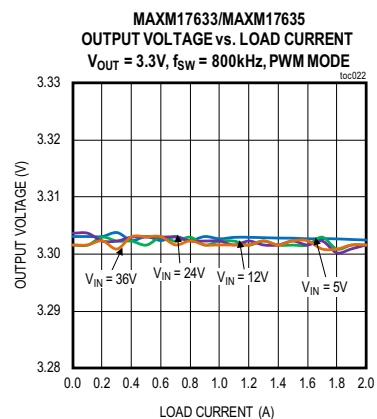
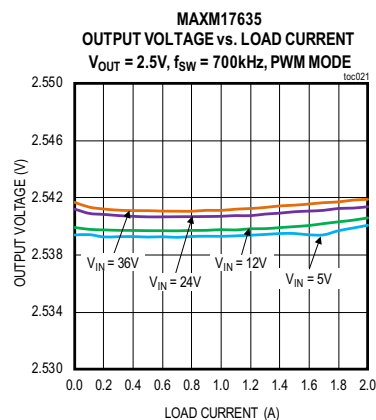
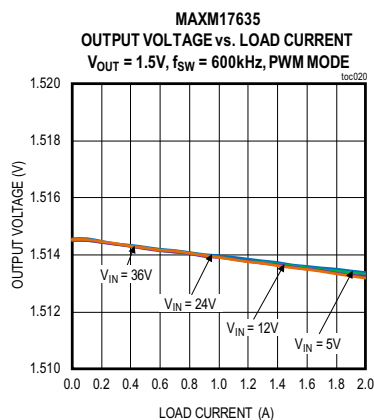
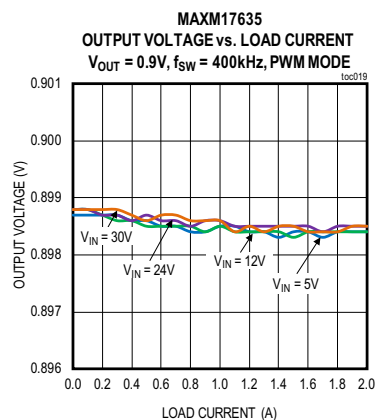
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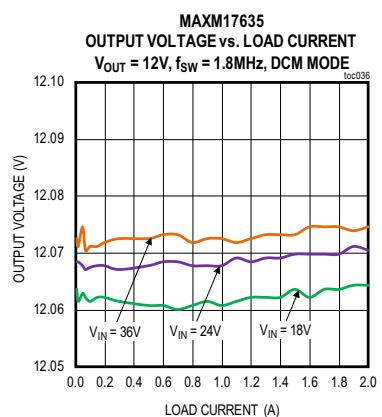
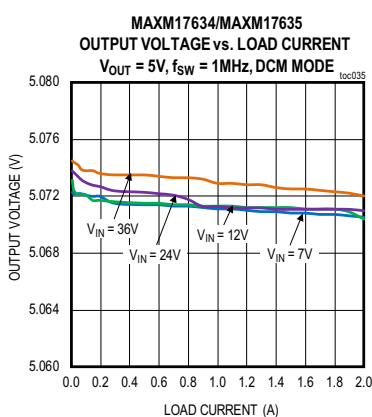
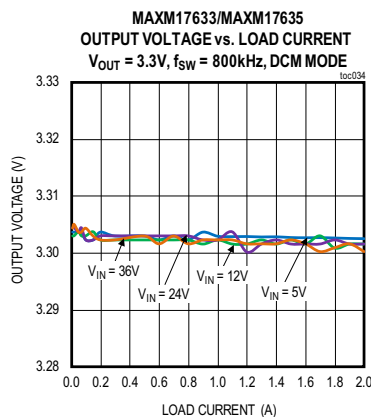
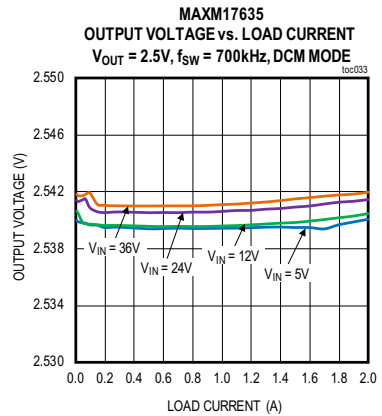
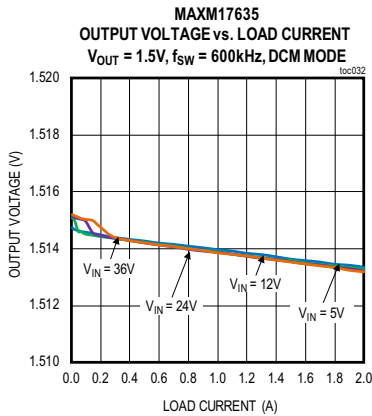
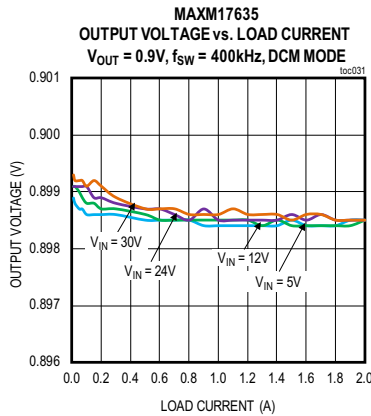
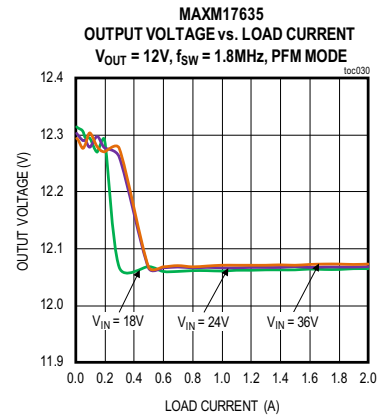
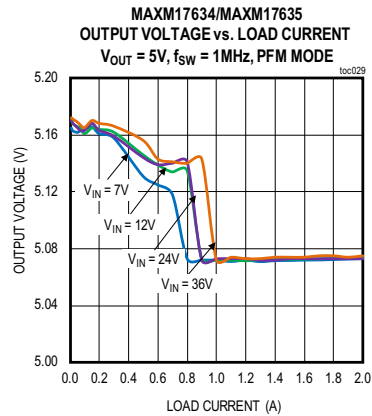
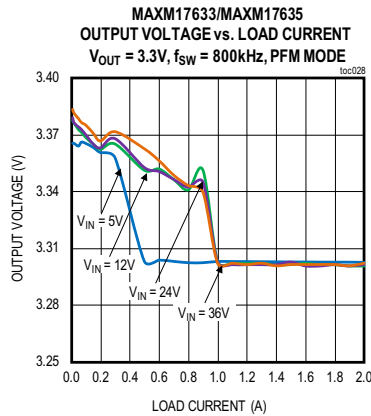
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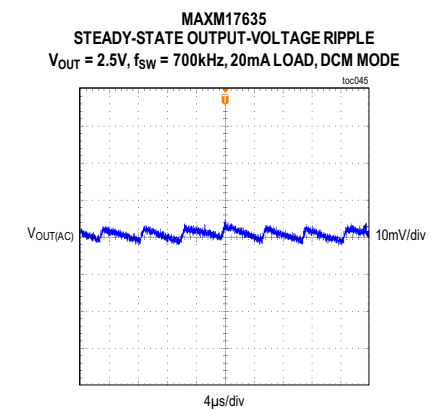
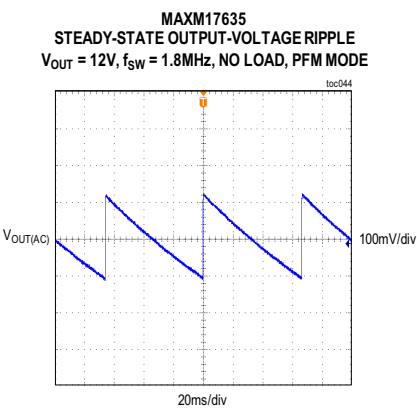
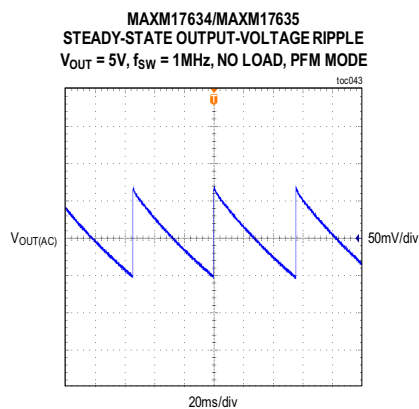
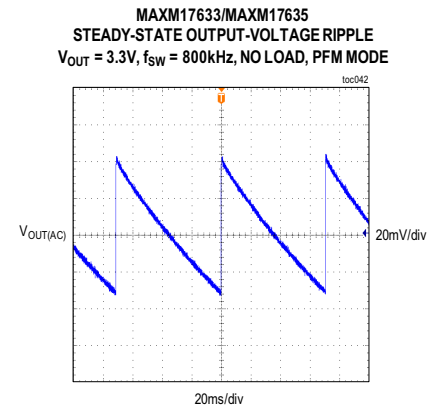
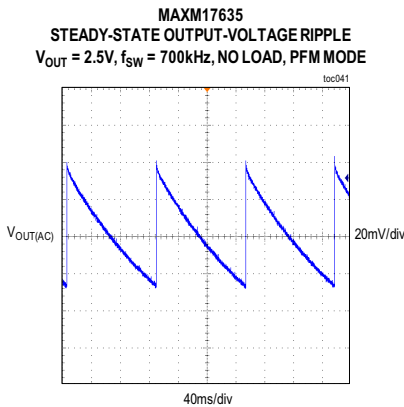
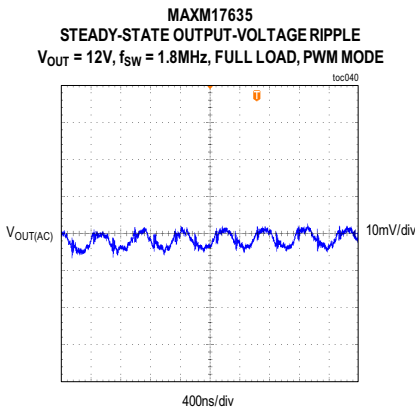
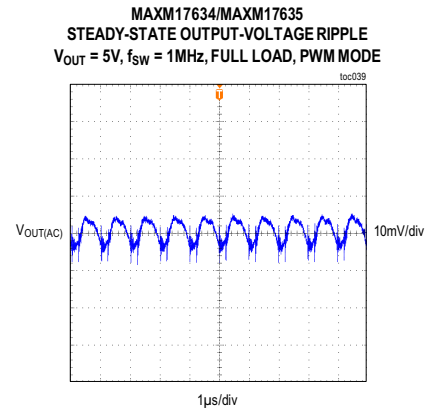
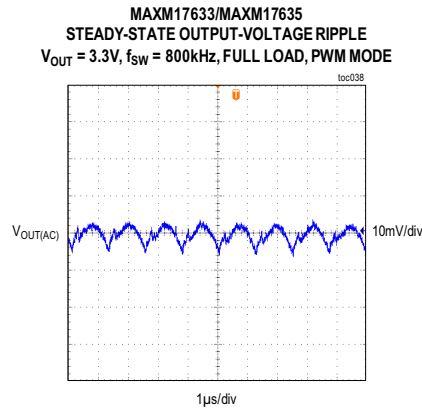
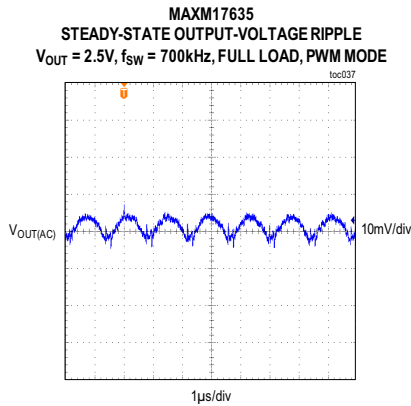
( $V_{EN}/UVLO = V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{INTVCC} = 2.2\mu F$ ,  $C_{BST} = 0.1\mu F$ ,  $C_{SS} = 5600pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications are as in [Table 1](#), unless otherwise noted.)





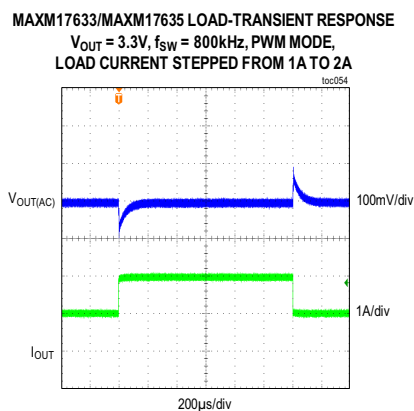
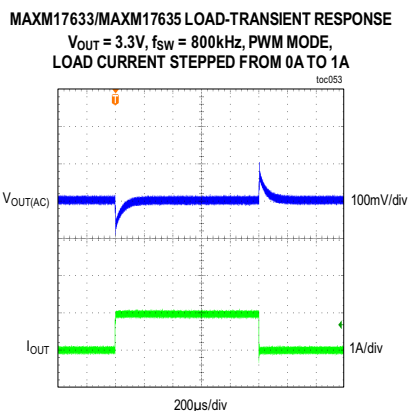
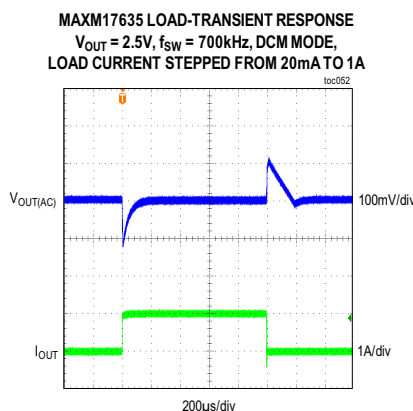
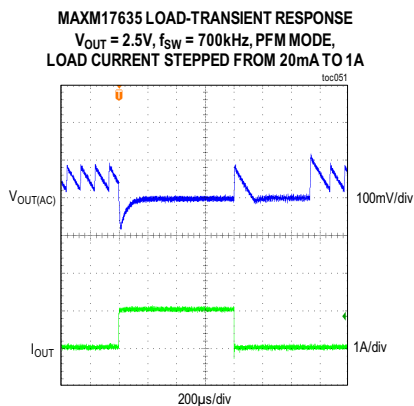
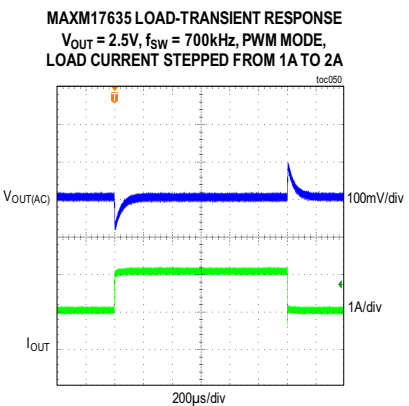
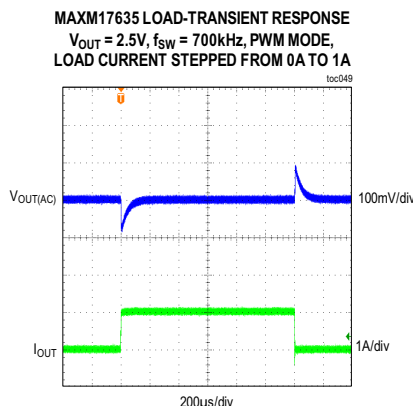
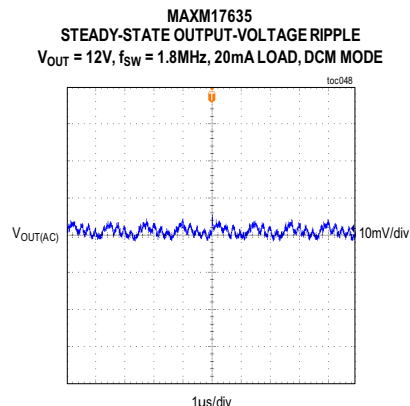
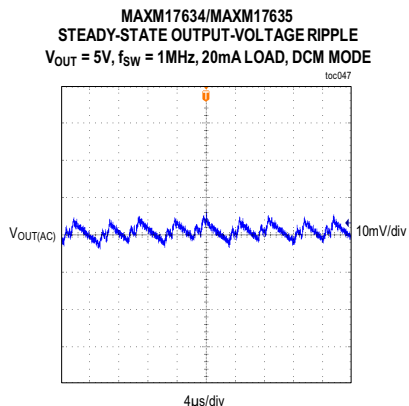
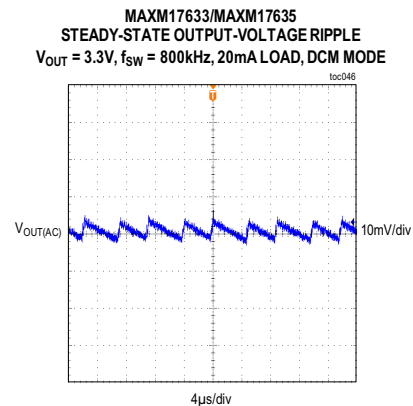
## Typical Operating Characteristics (continued)

( $V_{EN/UVLO} = V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{INTVCC} = 2.2\mu F$ ,  $C_{BST} = 0.1\mu F$ ,  $C_{SS} = 5600pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications are as in [Table 1](#), unless otherwise noted.)



## Typical Operating Characteristics (continued)

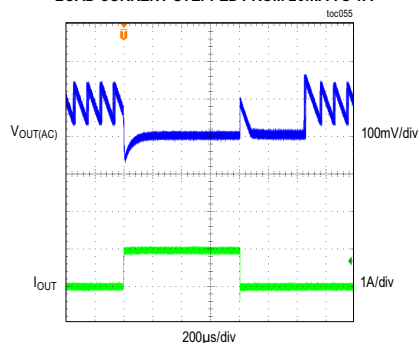
( $V_{EN/UVLO} = V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{INTVCC} = 2.2\mu F$ ,  $C_{BST} = 0.1\mu F$ ,  $C_{SS} = 5600pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications are as in [Table 1](#), unless otherwise noted.)



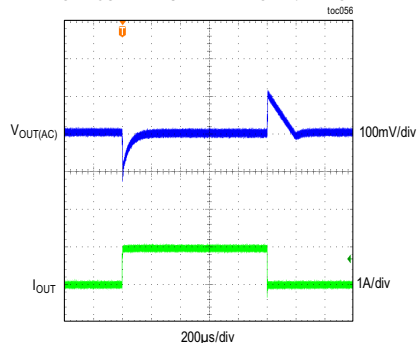
## Typical Operating Characteristics (continued)

( $V_{EN/UVLO} = V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{INTVCC} = 2.2\mu F$ ,  $C_{BST} = 0.1\mu F$ ,  $C_{SS} = 5600pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications are as in [Table 1](#), unless otherwise noted.)

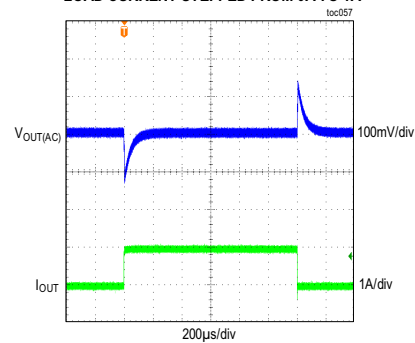
**MAXM17633/MAXM17635 LOAD-TRANSIENT RESPONSE**  
 $V_{OUT} = 3.3V$ ,  $f_{SW} = 800kHz$ , PFM MODE,  
LOAD CURRENT STEPPED FROM 20mA TO 1A



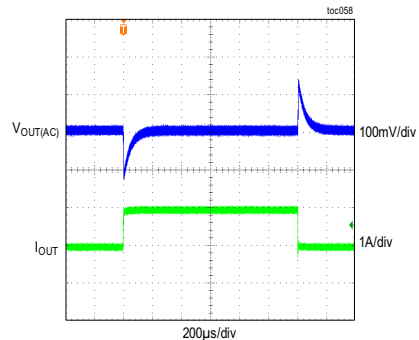
**MAXM17633/MAXM17635 LOAD-TRANSIENT RESPONSE**  
 $V_{OUT} = 3.3V$ ,  $f_{SW} = 800kHz$ , DCM MODE,  
LOAD CURRENT STEPPED FROM 20mA TO 1A



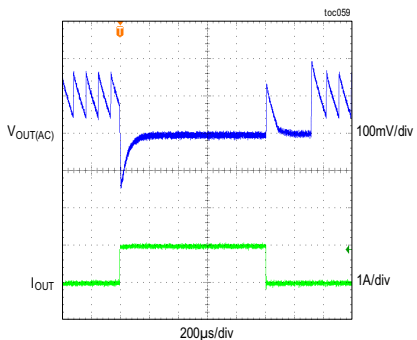
**MAXM17634/MAXM17635 LOAD-TRANSIENT RESPONSE**  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , PWM MODE,  
LOAD CURRENT STEPPED FROM 0A TO 1A



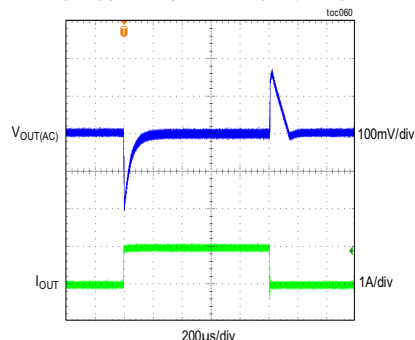
**MAXM17634/MAXM17635 LOAD-TRANSIENT RESPONSE**  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , PWM MODE,  
LOAD CURRENT STEPPED FROM 1A TO 2A



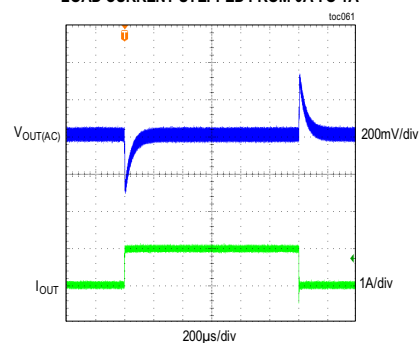
**MAXM17634/MAXM17635 LOAD-TRANSIENT RESPONSE**  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , PFM MODE,  
LOAD CURRENT STEPPED FROM 20mA TO 1A



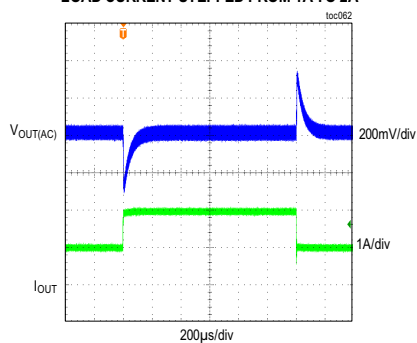
**MAXM17634/MAXM17635 LOAD-TRANSIENT RESPONSE**  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , DCM MODE,  
LOAD CURRENT STEPPED FROM 20mA TO 1A



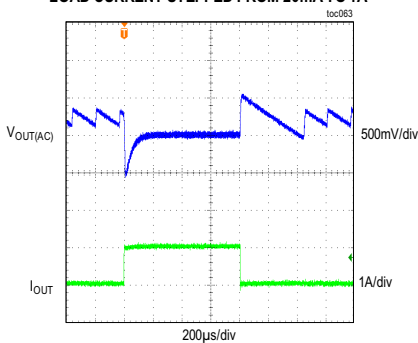
**MAXM17635 LOAD-TRANSIENT RESPONSE**  
 $V_{OUT} = 12V$ ,  $f_{SW} = 1.8MHz$ , PWM MODE,  
LOAD CURRENT STEPPED FROM 0A TO 1A



**MAXM17635 LOAD-TRANSIENT RESPONSE**  
 $V_{OUT} = 12V$ ,  $f_{SW} = 1.8MHz$ , PWM MODE,  
LOAD CURRENT STEPPED FROM 1A TO 2A



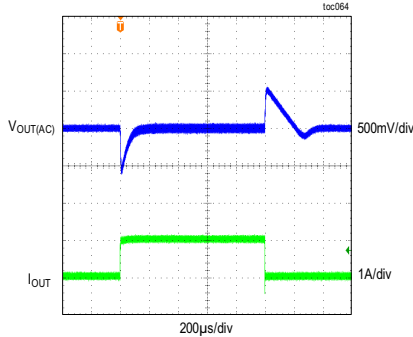
**MAXM17635 LOAD-TRANSIENT RESPONSE**  
 $V_{OUT} = 12V$ ,  $f_{SW} = 1.8MHz$ , PFM MODE,  
LOAD CURRENT STEPPED FROM 20mA TO 1A



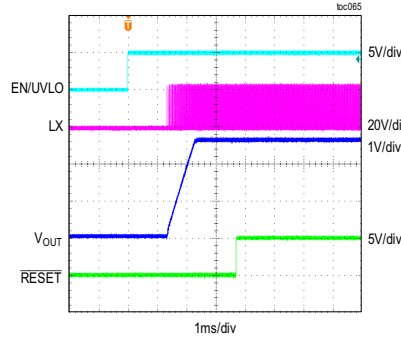
## Typical Operating Characteristics (continued)

( $V_{EN/UVLO} = V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{INTVCC} = 2.2\mu F$ ,  $C_{BST} = 0.1\mu F$ ,  $C_{SS} = 5600pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications are as in [Table 1](#), unless otherwise noted.)

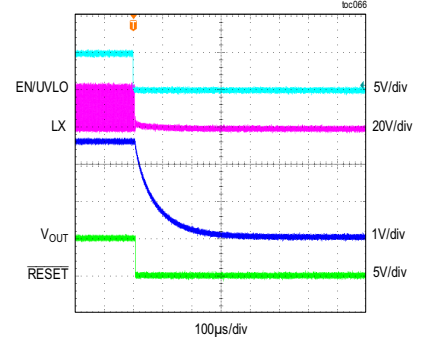
**MAXM17635 LOAD-TRANSIENT RESPONSE**  
 $V_{OUT} = 12V$ ,  $f_{SW} = 1.8MHz$ , DCM MODE,  
LOAD CURRENT STEPPED FROM 20mA TO 1A



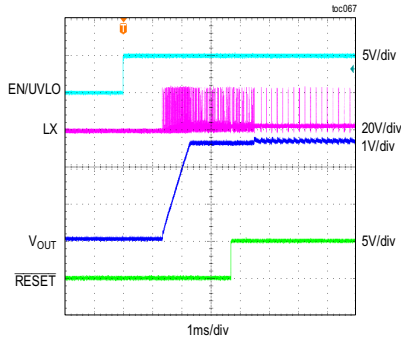
**MAXM17635 STARTUP THROUGH ENABLE**  
 $V_{OUT} = 2.5V$ ,  $f_{SW} = 700kHz$ , FULL LOAD, PWM MODE



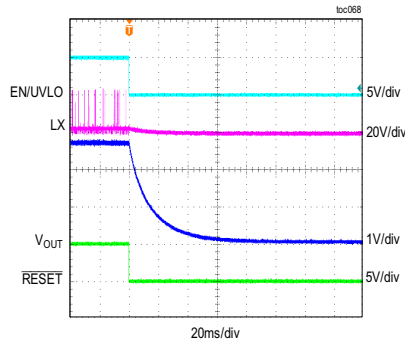
**MAXM17635 SHUTDOWN THROUGH ENABLE**  
 $V_{OUT} = 2.5V$ ,  $f_{SW} = 700kHz$ , FULL LOAD, PWM MODE



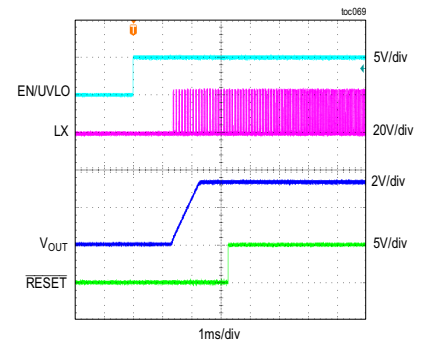
**MAXM17635 STARTUP THROUGH ENABLE**  
 $V_{OUT} = 2.5V$ ,  $f_{SW} = 700kHz$ , 20mA LOAD, PFM MODE



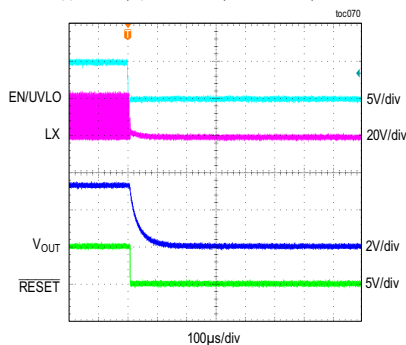
**MAXM17635 SHUTDOWN THROUGH ENABLE**  
 $V_{OUT} = 2.5V$ ,  $f_{SW} = 700kHz$ , 20mA LOAD, PFM MODE



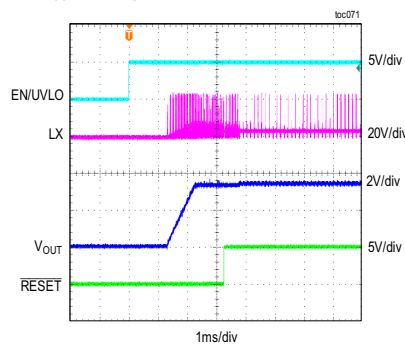
**MAXM17633/MAXM17635 STARTUP THROUGH ENABLE**  
 $V_{OUT} = 3.3V$ ,  $f_{SW} = 800kHz$ , FULL LOAD, PWM MODE



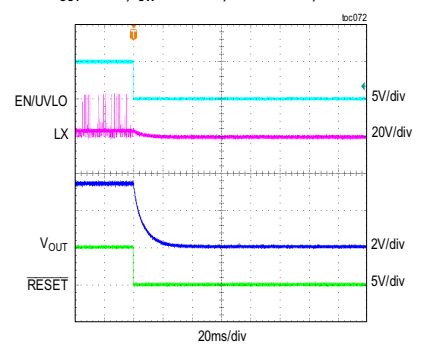
**MAXM17633/MAXM17635 SHUTDOWN THROUGH ENABLE**  
 $V_{OUT} = 3.3V$ ,  $f_{SW} = 800kHz$ , FULL LOAD, PWM MODE



**MAXM17633/MAXM17635 STARTUP THROUGH ENABLE**  
 $V_{OUT} = 3.3V$ ,  $f_{SW} = 800kHz$ , 20mA LOAD, PFM MODE



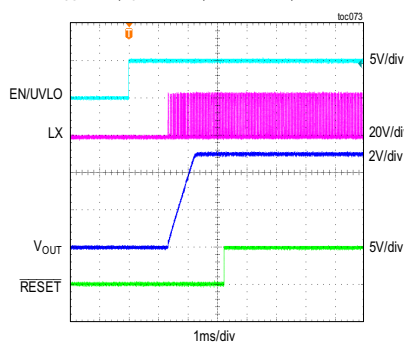
**MAXM17633/MAXM17635 SHUTDOWN THROUGH ENABLE**  
 $V_{OUT} = 3.3V$ ,  $f_{SW} = 800kHz$ , 20mA LOAD, PFM MODE



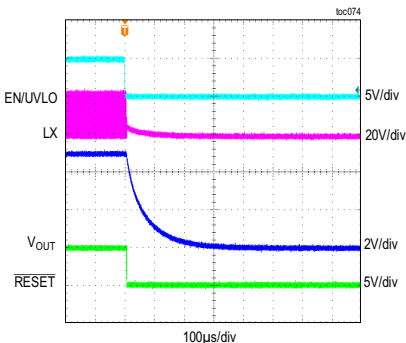
## Typical Operating Characteristics (continued)

( $V_{EN/UVLO} = V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{INTVCC} = 2.2\mu F$ ,  $C_{BST} = 0.1\mu F$ ,  $C_{SS} = 5600pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications are as in [Table 1](#), unless otherwise noted.)

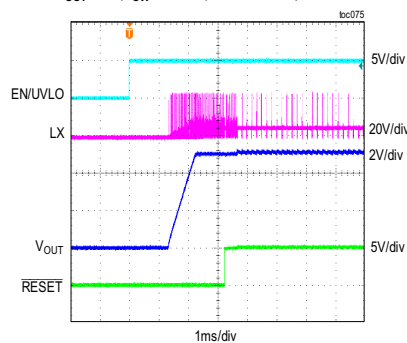
**MAXM17634/MAXM17635 STARTUP THROUGH ENABLE**  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , FULL LOAD, PWM MODE



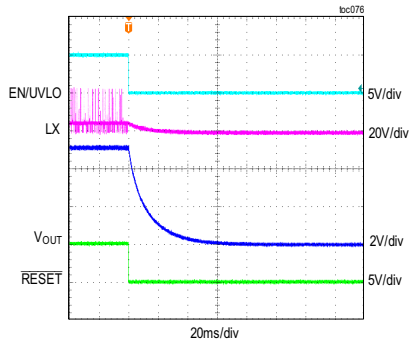
**MAXM17634/MAXM17635 SHUTDOWN THROUGH ENABLE**  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , FULL LOAD, PWM MODE



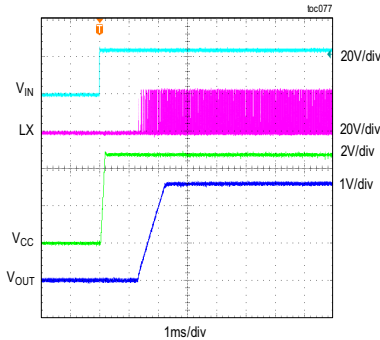
**MAXM17634/MAXM17635 STARTUP THROUGH ENABLE**  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , 20mA LOAD, PFM MODE



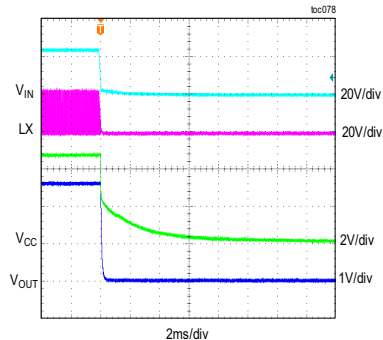
**MAXM17634/MAXM17635 SHUTDOWN THROUGH ENABLE**  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , 20mA LOAD, PFM MODE



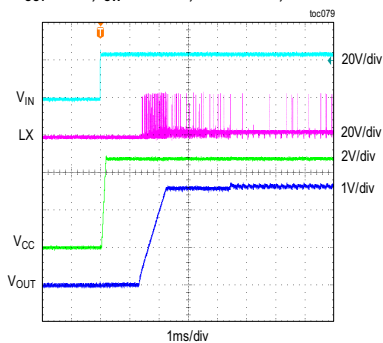
**MAXM17635 STARTUP THROUGH IN**  
 $V_{OUT} = 2.5V$ ,  $f_{SW} = 700kHz$ , FULL LOAD, PWM MODE



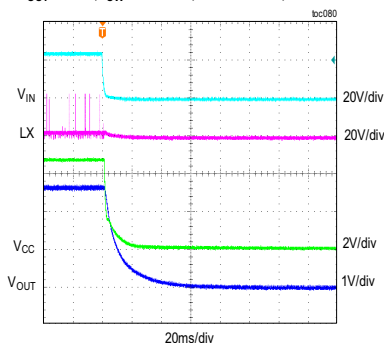
**MAXM17635 SHUTDOWN THROUGH IN**  
 $V_{OUT} = 2.5V$ ,  $f_{SW} = 700kHz$ , FULL LOAD, PWM MODE



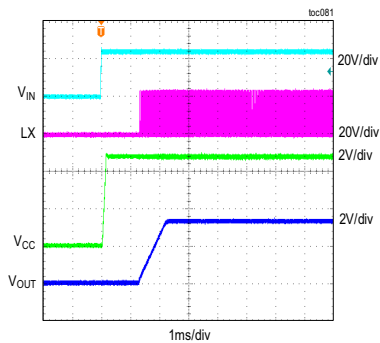
**MAXM17635 STARTUP THROUGH IN**  
 $V_{OUT} = 2.5V$ ,  $f_{SW} = 700kHz$ , 20mA LOAD, PFM MODE



**MAXM17635 SHUTDOWN THROUGH IN**  
 $V_{OUT} = 2.5V$ ,  $f_{SW} = 700kHz$ , 20mA LOAD, PFM MODE



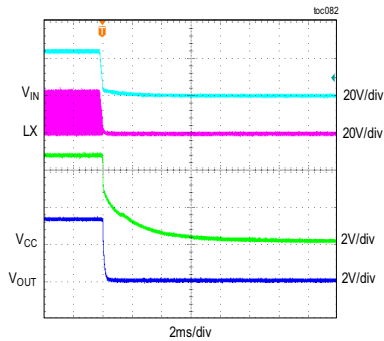
**MAXM17633/MAXM17635 STARTUP THROUGH IN**  
 $V_{OUT} = 3.3V$ ,  $f_{SW} = 800kHz$ , FULL LOAD, PWM MODE



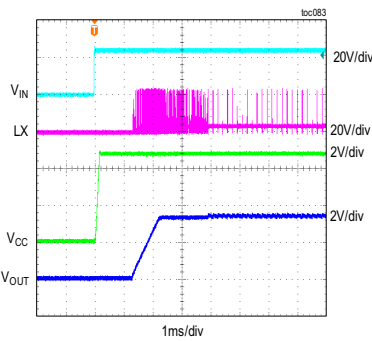
## Typical Operating Characteristics (continued)

( $V_{EN}/V_{VLO} = V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{INTVCC} = 2.2\mu F$ ,  $C_{BST} = 0.1\mu F$ ,  $C_{SS} = 5600pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications are as in [Table 1](#), unless otherwise noted.)

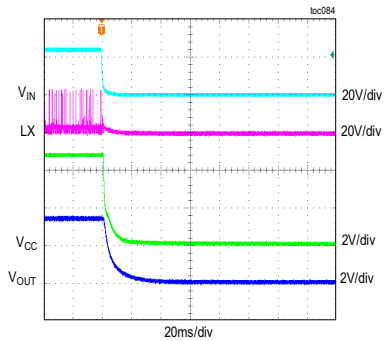
MAXM17633/MAXM17635 SHUTDOWN THROUGH IN  
 $V_{OUT} = 3.3V$ ,  $f_{SW} = 800kHz$ , FULL LOAD, PWM MODE



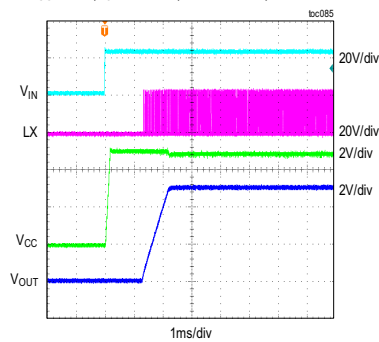
MAXM17633/MAXM17635 STARTUP THROUGH IN  
 $V_{OUT} = 3.3V$ ,  $f_{SW} = 800kHz$ , 20mA LOAD, PFM MODE



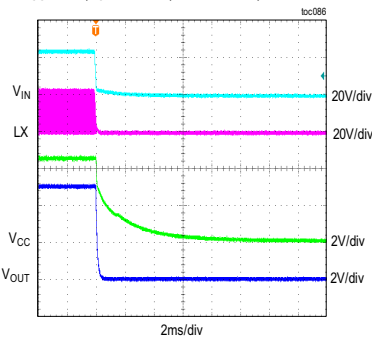
MAXM17633/MAXM17635 SHUTDOWN THROUGH IN  
 $V_{OUT} = 3.3V$ ,  $f_{SW} = 800kHz$ , 20mA LOAD, PFM MODE



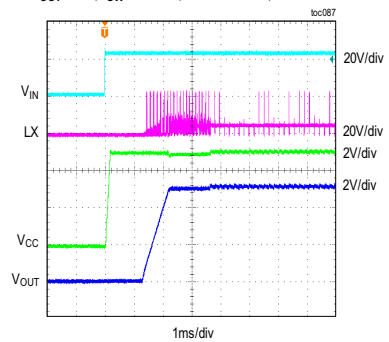
MAXM17634/MAXM17635 STARTUP THROUGH IN  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , FULL LOAD, PWM MODE



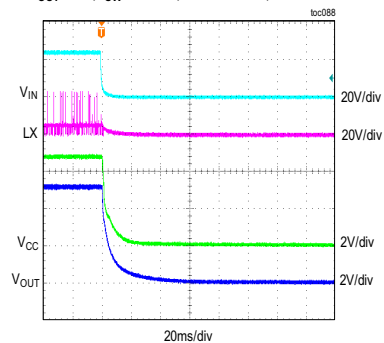
MAXM17634/MAXM17635 SHUTDOWN THROUGH IN  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , FULL LOAD, PWM MODE



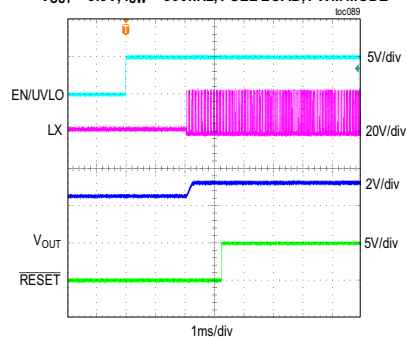
MAXM17634/MAXM17635 STARTUP THROUGH IN  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , 20mA LOAD, PFM MODE



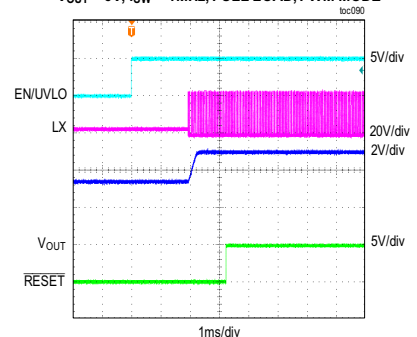
MAXM17634/MAXM17635 SHUTDOWN THROUGH IN  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , 20mA LOAD, PFM MODE



MAXM17633/MAXM17635  
STARTUP THROUGH ENABLE (2.5V PREBIAS)  
 $V_{OUT} = 3.3V$ ,  $f_{SW} = 800kHz$ , FULL LOAD, PWM MODE

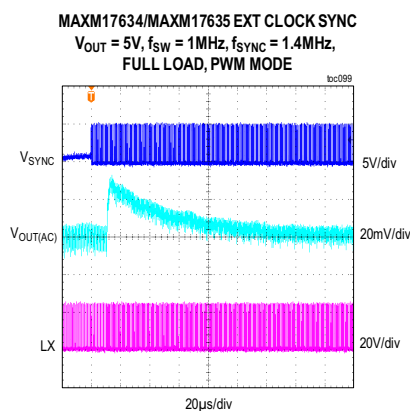
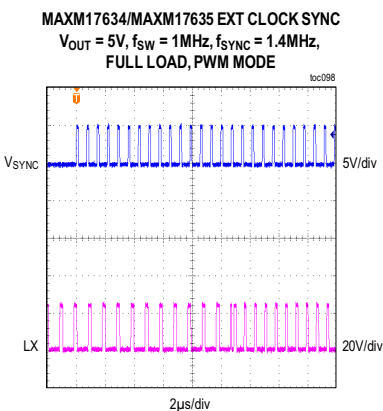
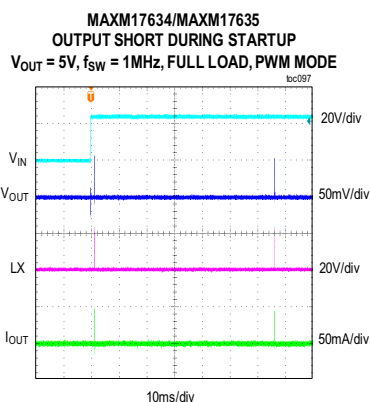
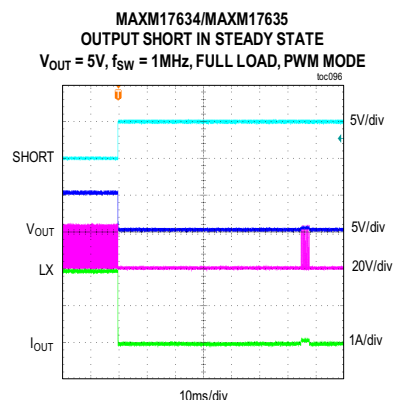
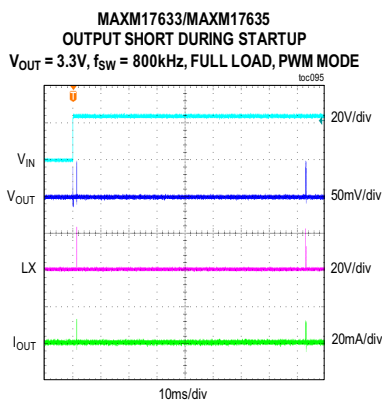
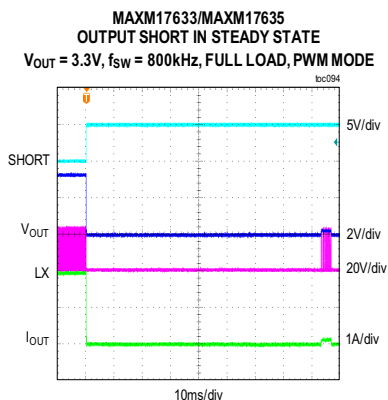
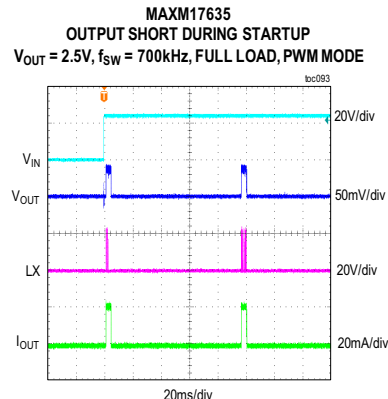
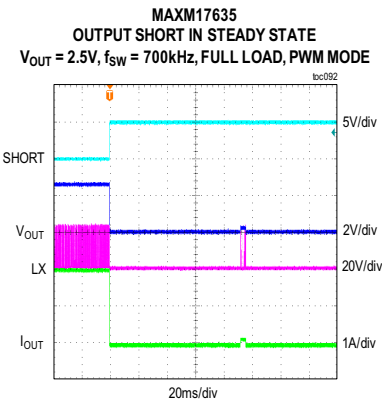
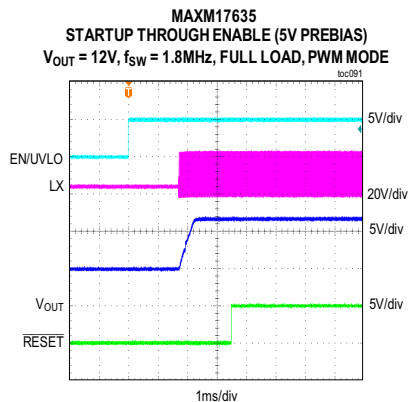


MAXM17634/MAXM17635  
STARTUP THROUGH ENABLE (3.3V PREBIAS)  
 $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$ , FULL LOAD, PWM MODE



## Typical Operating Characteristics (continued)

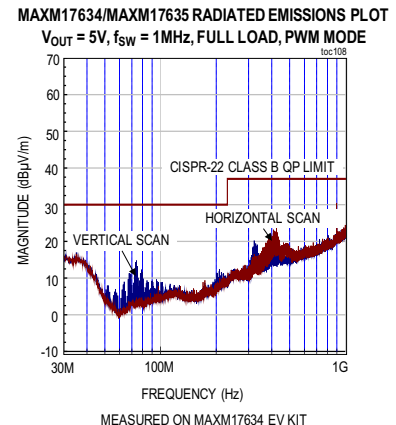
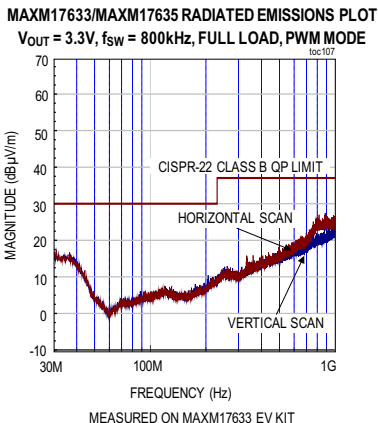
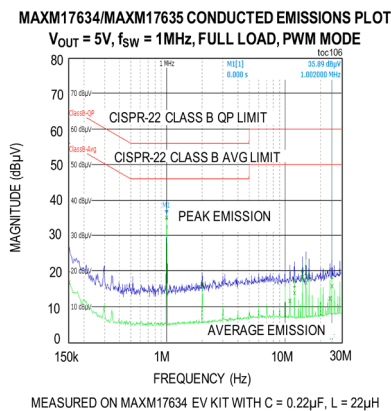
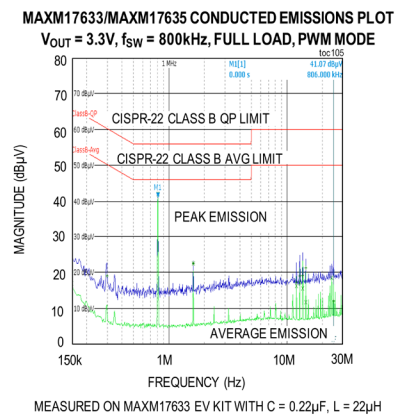
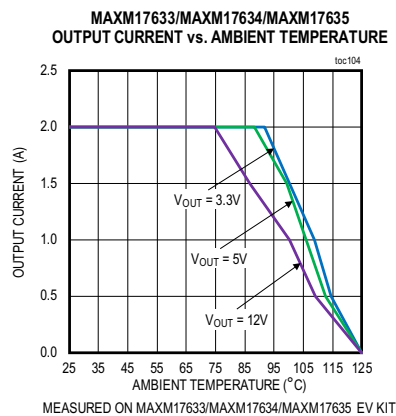
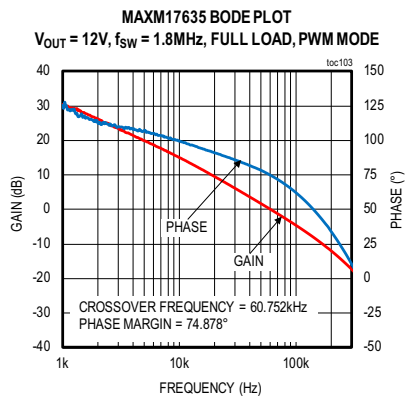
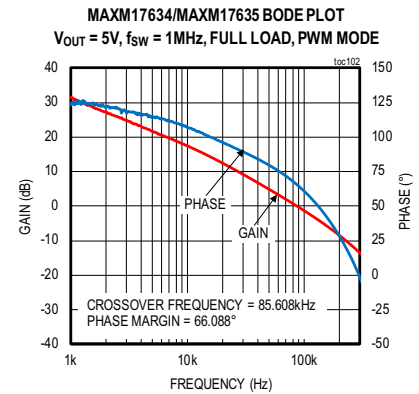
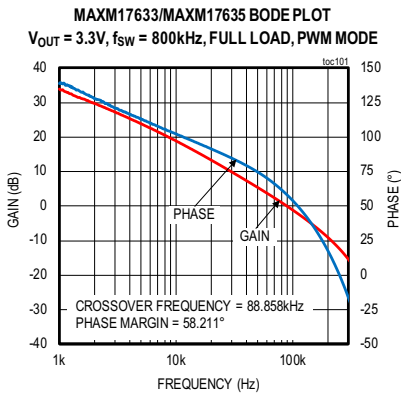
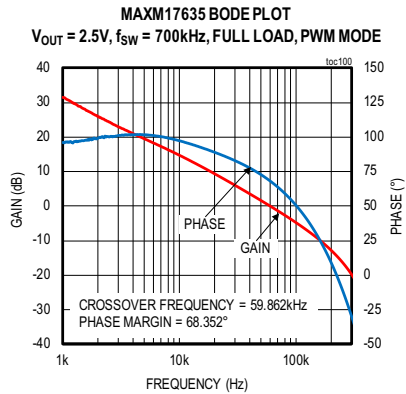
( $V_{EN/UVLO} = V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{INTVCC} = 2.2\mu F$ ,  $C_{BST} = 0.1\mu F$ ,  $C_{SS} = 5600pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications are as in [Table 1](#), unless otherwise noted.)





## Typical Operating Characteristics (continued)

( $V_{EN}/UVLO = V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{INTVCC} = 2.2\mu F$ ,  $C_{BST} = 0.1\mu F$ ,  $C_{SS} = 5600pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications are as in [Table 1](#), unless otherwise noted.)

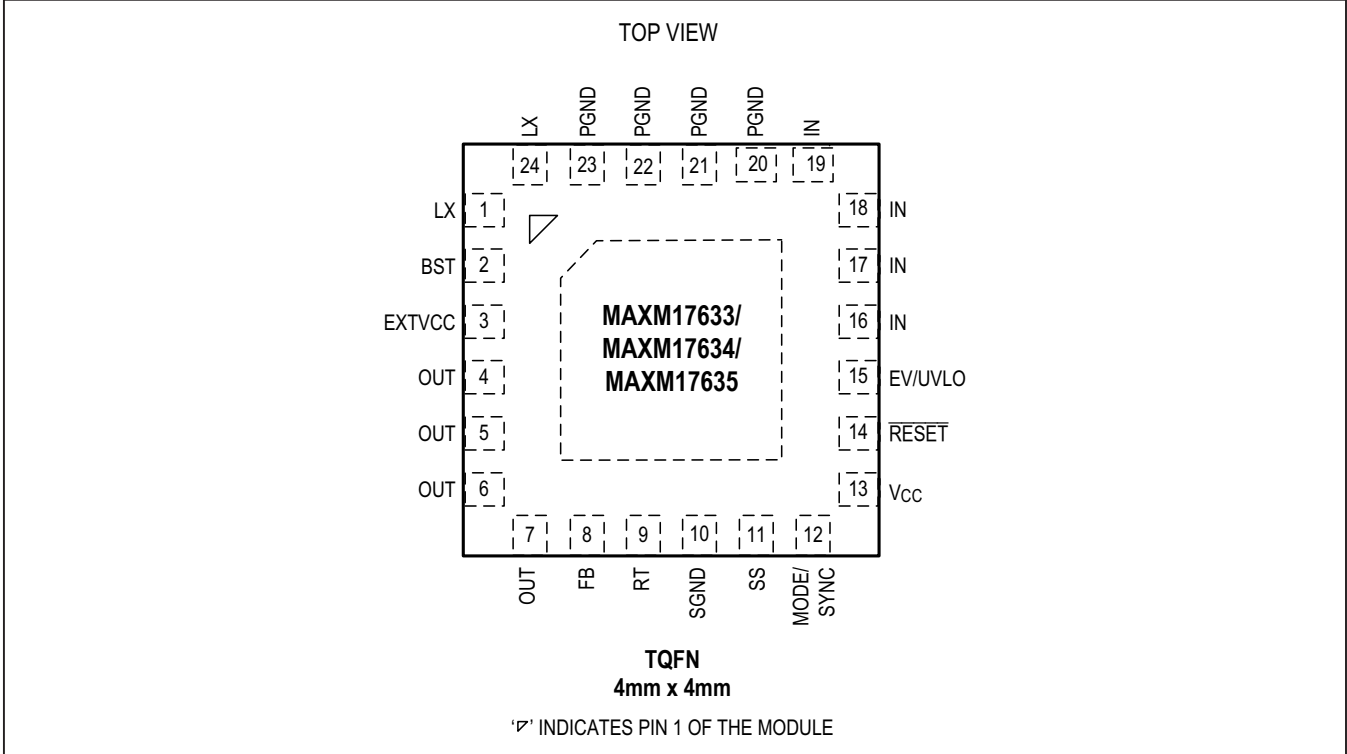




MAXM17633/MAXM17634/  
MAXM17635

4.5V to 36V, 2A Himalaya uSLIC  
Step-Down Power Modules

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 24	LX	Switching Node Pins.
2	BST	Bootstrap Flying Capacitor. Connect a 0.1μF ceramic capacitor between BST and LX.
3	EXTVCC	External Power Supply Input. Reduces the Internal-LDO Loss. Connect it to OUT when it is programmed for 5V output. When EXTVCC is not used, connect it to SGND.
4-7	OUT	Module Output Pins. Connect the output capacitor C <sub>OUT</sub> from OUT to PGND.
8	FB	Output Feedback Connection. Connect FB to the output-voltage node (OUT) for MAXM17633 and MAXM17634. Connect FB to the center of the external resistor-divider from OUT to SGND for MAXM17635 to set the output voltage.
9	RT	Programmable Switching Frequency Input. Connect a resistor from RT to SGND to set the switching frequency of the module between 400kHz and 2.2MHz. Leave RT open for the default 500kHz frequency. See the <a href="#">Setting the Switching Frequency (RT)</a> section for more details.
10	SGND	Signal Ground Pin.
11	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.

## Pin Description (continued)

PIN	NAME	FUNCTION
12	MODE/SYNC	MODE/SYNC Pin. Configures the module to operate in PWM, PFM, or DCM mode of operation. Leave MODE/SYNC unconnected for PFM operation (pulse skipping at light loads). Connect MODE/SYNC to SGND for constant-frequency PWM operation at all loads. Connect MODE/SYNC to V <sub>CC</sub> for DCM operation at light loads. The module can be synchronized to an external clock using this pin. See the <a href="#">Mode Selection and External Synchronization (MODE/SYNC)</a> section for more details.
13	V <sub>CC</sub>	5V LDO Output of the module. Bypass V <sub>CC</sub> with a 2.2μF ceramic capacitor to SGND.
14	RESET	Open-Drain RESET Output. The RESET output is driven low if FB drops below 92% of its set value. RESET goes high 1024 cycles after FB rises above 95% of its set value.
15	EN/UVLO	Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the output. Connect EN/UVLO to the center of the resistor-divider between IN and SGND to set the input voltage at which the part turns on. Connect EN/UVLO to the IN pin for always-on operation. Pull EN/UVLO low for disabling the module.
16-19	IN	Power-Supply Input Pins. 4.5V to 36V input-supply range. Decouple to PGND with a capacitor; place the capacitor close to the IN and PGND pins.
20-23	PGND	Power Ground Pins. Connect externally to the power ground plane. Refer to the <i>MAXM17633 Evaluation Kit data sheet</i> for a layout example.
—	EP	Exposed Pad. Connect EP to the PGND pins of module. Also, connect EP to a large PGND plane with several thermal vias for the best thermal performance. Refer to the <i>MAXM17633 EV Kit data sheet</i> for an example of the correct method for EP connection and thermal vias.

**MAXM17633/MAXM17634/MAXM17635**

The diagram shows the internal architecture of the MAXM17633, MAXM17634, and MAXM17635 converters. Key components include:

- Inputs:** BST, EN/UVLO, RT, MODE/SYNC, EXTVCC, Vcc, SS, FB, RESET.
- Internal Blocks:**
  - OSCILLATOR:** Receives RT and provides a clock to the PWM/PM/HICCUP LOGIC.
  - MODE SELECTION:** Receives MODE/SYNC and provides a signal to the PWM/PM/HICCUP LOGIC.
  - PWM/PM/HICCUP LOGIC:** The central control block that manages the switching and regulation.
  - LDO:** Receives EXTVCC and provides a regulated output to the internal circuitry.
  - THERMAL SHUTDOWN:** Monitors the device temperature and provides a shutdown signal to the PWM/PM/HICCUP LOGIC.
  - SLOPE COMPENSATION:** Provides a signal to the PWM/PM/HICCUP LOGIC to ensure stability.
  - CURRENT SENSE:** Monitors the output current and provides a signal to the PWM/PM/HICCUP LOGIC.
  - ERROR AMPLIFIER/LOOP COMPENSATION:** Receives feedback from the FB pin and provides a signal to the PWM/PM/HICCUP LOGIC.
  - SOFT-START LOGIC:** Receives a signal from the SS pin and provides a signal to the PWM/PM/HICCUP LOGIC.
  - RESET LOGIC:** Receives ENOK and FB signals and provides a reset signal to the PWM/PM/HICCUP LOGIC.
- Outputs:** ENOK, HICCUP, OUT, PGND, SGND.

**Switching and Feedback Network:**

- The output stage consists of a MOSFET switching the load (LX) from the BST input.
- The output filter inductor (3.3μH) is connected between the LX and OUT pins.
- The feedback network includes resistors R1 and R2, and switches S1, S2, and S3, connected to the FB pin.

**Pin Connections:**

- BST:** Bootstrap input.
- EN/UVLO:** Enable/Under Voltage Lockout input.
- RT:** Resistor Timing input.
- MODE/SYNC:** Mode Selection/Synchronization input.
- EXTVCC:** External VCC input.
- Vcc:** Main power supply input.
- SS:** Soft-Start input.
- FB:** Feedback input.
- RESET:** Reset input.
- OUT:** Output voltage.
- PGND:** Power Ground.
- SGND:** Signal Ground.

**Component Values:**

- 3.3μH: Output filter inductor.
- R1: 176.6kΩ, R2: 38.8kΩ for MAXM17634.
- R1: 103.4kΩ, R2: 38.8kΩ for MAXM17633.

**Switching States:**

- S1: CLOSED; S2, S3: OPEN for MAXM17635.
- S1: OPEN; S2, S3: CLOSED for MAXM17633/MAXM17634.

## Detailed Description

The MAXM17633, MAXM17634, and MAXM17635 are a family of high-frequency synchronous step-down DC-DC converter modules, with integrated controller, MOSFETs, compensation components, and inductor that operate over a wide input voltage range. The modules deliver an output current of up to 2A. The MAXM17633 and MAXM17634 are fixed 3.3V and 5V output modules, respectively. The MAXM17635 is an adjustable-output voltage (0.9V to 12V) module. When EN/UVLO and the  $V_{CC}$  threshold are ascertained, an internal power-up sequence ramps up the error-amplifier reference, resulting in an output-voltage soft-start.

The FB pin monitors the output voltage through a resistor divider. The  $\overline{\text{RESET}}$  pin transitions to a high-impedance state 1024 clock cycles after the output voltage reaches 95% of regulation. The modules select either PFM or forced-PWM or DCM mode depending on the state of the MODE/SYNC pin at power-up. By pulling the EN/UVLO pin low, the modules enter shutdown mode and consume only 2.8 $\mu$ A (typ) of standby current.

The modules employ peak-current-mode control architecture. An internal error amplifier compares the feedback voltage to a fixed reference voltage and generates an error voltage. The error voltage is compared to the sum of the current-sense voltage and slope-compensation voltage by a PWM comparator to set the on-time. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the internal inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor in the module releases the stored energy as its current ramps down and provides current to the output.

## Mode Selection and External Synchronization (MODE/SYNC)

The modules support PWM, PFM, and DCM modes of operation. The modules enter the required mode of operation based on the setting of the MODE/SYNC pin as detected within 1.5ms after  $V_{CC}$  and EN/UVLO voltages exceed their respective rising thresholds ( $V_{CC\_UVR}$ ,  $V_{ENR}$ ). If the state of the MODE/SYNC pin is open, the modules operate in PFM mode at light loads. If the state of the MODE/SYNC pin is low (lower than  $V_{M\_PWM}$ ), the modules operate in constant-frequency PWM mode at all loads. If the state of the MODE/SYNC pin is high

(higher than  $V_{M\_DCM}$ ), the modules operate in constant-frequency DCM mode at light loads. State changes on the MODE/SYNC pin are ignored during normal operation.

The internal oscillator of the modules can be synchronized to an external clock signal through the MODE/SYNC pin when the part is programmed to DCM or PWM mode of operation. SYNC is not supported in PFM mode. The internal oscillator frequency changes to an external clock frequency when 16 external clock rising edges are detected on the MODE/SYNC pin. The external clock frequency must be between  $1.1 \times f_{SW}$  and  $1.4 \times f_{SW}$ , where  $f_{SW}$  is the switching frequency programmed by the resistor connected between the RT pin to SGND. The external clock pulse width should be greater than 50ns and the off time duration should be greater than 160ns. See the *Mode Sync* section in the [Electrical Characteristics](#) table for details.

## PWM Mode Operation

In PWM mode, the internal inductor current is allowed to go negative. PWM operation is useful in frequency sensitive applications and provides fixed switching frequency operation at all loads. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM and DCM modes of operation.

## PFM Mode Operation

PFM mode of operation disables negative internal inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the module output current is forced to a fixed peak of  $I_{PFM}$  (1.17A typ) every clock cycle until the output rises to 102.3% of the set nominal output voltage. Once the output reaches 102.3% of the set nominal output voltage, both the high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101.1% of the set nominal output voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101.1% of the set nominal output voltage, the module comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the set nominal output voltage. The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. The disadvantage is that the output-voltage ripple is higher compared to PWM or DCM modes of operation and switching frequency is not constant at light loads.

## DCM Mode Operation

DCM mode of operation features constant frequency operation down to lighter loads than PFM mode, by disabling negative internal inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes. The output voltage ripple in DCM mode is comparable to PWM mode and relatively lower compared to PFM mode.

## Linear Regulator (V<sub>CC</sub> and EXTVCC)

The modules have an internal low dropout (LDO) regulator that powers V<sub>CC</sub> from IN. This LDO is enabled during power-up or when EN/UVLO is above 0.75V (typ). An internal switch connects the EXTVCC to V<sub>CC</sub>. The switch is open during power-up. If V<sub>CC</sub> is above its UVLO threshold and if EXTVCC is greater than 4.7V (typ) then, the internal LDO is disabled and V<sub>CC</sub> is powered from EXTVCC. Powering V<sub>CC</sub> from EXTVCC increases efficiency at higher input voltages. Typical V<sub>CC</sub> output voltage is 5V. Bypass V<sub>CC</sub> to SGND with a 2.2μF low-ESR ceramic capacitor. V<sub>CC</sub> powers the internal blocks and the low-side MOSFET driver, and recharges the external bootstrap capacitor.

The modules employ an undervoltage lockout circuit that forces the converter off when V<sub>CC</sub> falls below V<sub>CC-UVF</sub> (3.8 typ). The modules can be immediately enabled again when V<sub>CC</sub> > V<sub>CC-UVR</sub> (4.2 typ). The 400mV UVLO hysteresis prevents chattering on power-up/power-down.

In applications where the module output is connected to the EXTVCC pin, if the output is shorted to ground then the transfer from EXTVCC to internal LDO happens seamlessly without any impact on the normal functionality. Connect the EXTVCC pin to SGND when not in use.

## Enable/Undervoltage Lockout (EN/UVLO), Soft-Start (SS)

When EN/UVLO voltage is above 1.215V (typ), the internal error-amplifier reference voltage of the module starts to ramp up. The duration of the soft-start ramp is programmable through the choice of an external capacitor put at the SS pin, allowing a smooth increase of the output voltage. Driving EN/UVLO low disables both power MOSFETs, as well as other internal circuitry, and reduces IN quiescent current to below 2.8μA (typ). EN/UVLO can be used as an input-voltage UVLO adjustment input. An external voltage-divider between IN and EN/UVLO to SGND adjusts the input voltage at which the device turns on or turns off. If input UVLO programming is not desired, connect EN/UVLO to IN (see the [Electrical Characteristics](#) table for EN/UVLO rising and falling threshold voltages).

## RESET Output

The modules include an open-drain RESET pin to monitor the status of output voltage. The RESET pin requires an external pullup resistor. RESET goes high impedance with a delay of 1024 switching cycles after the regulator output voltage increases above 95% of its nominal set value and goes low when the output voltage falls below 92% of its nominal set value. RESET also goes low during thermal shutdown or when the EN/UVLO pin goes below the falling threshold.

## Prebiased Output

The modules are capable of soft-start into a prebiased output, without discharging the output capacitor in all modes. Such a feature is useful in applications where digital integrated circuits with multiple rails are powered.

## Overcurrent Protection/Hiccup Mode

The modules are provided with a robust overcurrent protection (OCP) scheme that protects the modules under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of I<sub>PEAK-LIMIT</sub> (3.55A typ). A runaway current limit on the high-side switch current at the I<sub>RUNAWAY-LIMIT</sub> (4.43A typ) protects the device under high input voltage, output short-circuit conditions when there is insufficient output voltage available to restore the module current that was built up during the on period of the module. One occurrence of the runaway current limit triggers a hiccup mode. In addition, due to any fault, if the feedback voltage drops below 64% of the nominal value any time after soft-start is completed, the hiccup mode is activated. In hiccup mode, the modules are protected by suspending switching for a hiccup timeout period of 32,768 clock cycles of half the switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under overload condition, if feedback voltage does not exceed 64% of the nominal value, the modules continue to switch at half the programmed switching frequency for the time duration of the programmed soft-start time and 1024 clock cycles. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

The MAXM17633/34/35 are designed to support a maximum load current of 2A. The inductor ripple current is calculated as follows:

$$\Delta I = \left[ \frac{V_{IN} - V_{OUT} - 0.233 \times I_{OUT}}{L \times f_{SW}} \right] \times \left[ \frac{V_{OUT} + 0.188 \times I_{OUT}}{V_{IN} - 0.045 \times I_{OUT}} \right]$$

where:

$V_{OUT}$  = Steady-state output voltage

$V_{IN}$  = Operating input voltage for given  $V_{OUT}$

$f_{SW}$  = Switching frequency in MHz

$L$  = Power module output inductance ( $3.3\mu\text{H} \pm 20\%$ )

$I_{OUT}$  = Output (load) current

The following condition should be satisfied at the desired load current,  $I_{OUT}$ :

$$I_{OUT} + \frac{\Delta I}{2} < 3.1$$

### Thermal Overload Protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds  $+165^{\circ}\text{C}$ , an on-chip thermal sensor shuts down the device, turns off the internal power MOSFETs, allowing the device to cool down. The thermal sensor turns the device on after the junction temperature cools by  $10^{\circ}\text{C}$ .

## Applications Information

### Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage setting is calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + (0.188 \times I_{OUT})}{1 - (t_{OFF(MIN)} \times f_{SW})} + 0.045 \times I_{OUT}$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{t_{ON(MIN)} \times f_{SW}}$$

Also, for duty cycle  $> 0.5$ ,

$$V_{IN(MIN)} > 4.25 \times V_{OUT} + 0.65 \times I_{OUT} - 33.48 \times f_{SW}$$

where:

$V_{OUT}$  = Steady-state output voltage,

$I_{OUT}$  = Load current,

$t_{OFF(MIN)}$  = Minimum OFF time (160ns),

$t_{ON(MIN)}$  = Minimum ON time (80ns).

$f_{SW}$  = Switching frequency in MHz.

### Selection of Input capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the switching of the module.

The input capacitor RMS current requirement ( $I_{RMS}$ ) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where,  $I_{OUT(MAX)}$  is the maximum load current.  $I_{RMS}$  has a maximum value when the input voltage equals twice the output voltage ( $V_{IN} = 2 \times V_{OUT}$ ), so

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}$$

Choose an input capacitor that exhibits less than  $+10^{\circ}\text{C}$  temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = I_{OUT(MAX)} \times D \times \frac{(1-D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

$D$  = Duty ratio of the converter

$f_{SW}$  = Switching frequency

$\Delta V_{IN}$  = Allowable input voltage ripple

$\eta$  = Efficiency

In applications where the source is located away and distant from the device input, an appropriate electrolytic capacitor should be added to provide necessary damping of potential oscillations caused by the inductance of the input power path and input ceramic capacitor.

### Selection of Output capacitor

Small ceramic X7R-grade capacitors are sufficient and recommended for output-voltage generation. The output capacitor has two functions. It provides smooth output voltage and, stores sufficient energy to support the output voltage under load transient conditions stabilizing the internal control loop of the module. Usually the output capacitor is sized to support a load step of 50% of the maximum output current in the application, such that the output-voltage deviation is less than 3%. Required output capacitance can be calculated from the following equation:

$$C_{OUT} = \frac{5.5}{f_C \times V_{OUT}}$$



where:

$C_{OUT}$  = Output capacitance in  $\mu\text{F}$

$V_{OUT}$  = Output voltage

$f_C$  = Desired crossover frequency.  $f_C$  is chosen to be the lowest value between  $1/10^{\text{th}}$  of the switching frequency and 80kHz.

Derating of ceramic capacitors with DC-voltage at appropriate AC voltage (equal to the steady-state output voltage ripple) must be considered while selecting the output capacitor.

### Selection of SS capacitor

The modules implement adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance ( $C_{SEL}$ ) and the output voltage ( $V_{OUT}$ ) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time ( $t_{SS}$ ) is related to the capacitor connected at SS ( $C_{SS}$ ) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to SGND. Note that, during start-up, modules operate at half the programmed switching frequency until the output voltage reaches 66.7% of set output nominal voltage.

### Setting the Input Undervoltage-Lockout Level

The modules offer an adjustable input undervoltage lock-out level. Set the voltage at which the module turns on with a resistive voltage-divider connected from IN to GND (see Figure 1). Connect the center node of the divider to EN/UVLO.

Choose  $R_U$  to be 3.3M $\Omega$  (max), and then calculate  $R_B$  as follows:

$$R_B = \frac{R_U \times 1.215}{(V_{INU} - 1.215)}$$

where  $V_{INU}$  is the voltage at which the module is required to turn on. See Table 1 to set the proper  $V_{INU}$  voltage greater than or equal to the minimum input voltage for each desired output voltage.

If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1k $\Omega$  is recommended to be placed between the signal source output and the EN/UVLO pin, to reduce voltage ringing on the line.

### Setting the Output Voltage

Set the output voltage with a resistive voltage-divider connected from the output-voltage node (OUT) to SGND (see Figure 2). Connect the center node of the divider to the FB pin for MAXM17635. Connect the output-voltage node (OUT) directly to the FB pin for MAXM17633 and MAXM17634. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R1 from the output to the FB pin as follows:

$$R1 = \frac{270}{f_C \times C_{OUT}}$$

where R1 is in k $\Omega$ , crossover frequency  $f_C$  is in Hz, and the derated value of the output capacitor  $C_{OUT}$  is in F. Calculate resistor R2 connected from the FB pin to SGND as follows:

$$R2 = \frac{R1 \times 0.9}{(V_{OUT} - 0.9)}$$

R2 is in k $\Omega$ .

Select an appropriate  $f_C$  and  $C_{OUT}$  so that the parallel combination of R2 and R1 is less than 50k $\Omega$ .

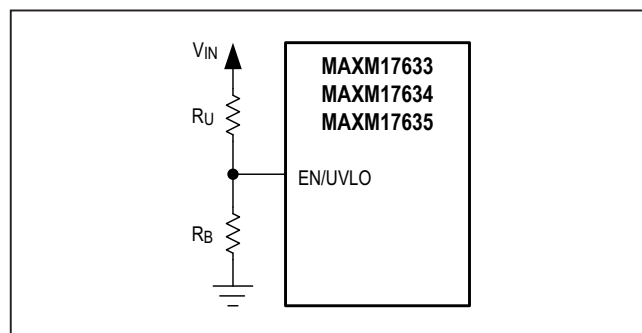


Figure 1. Setting the EN/UVLO Network

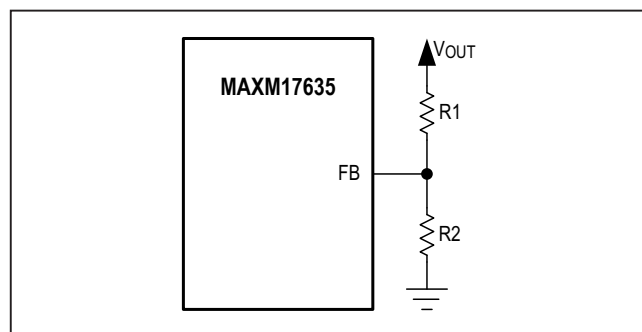


Figure 2. Setting the Output Voltage

### Setting the Switching Frequency (RT)

The switching frequency of the module can be programmed from 400kHz to 2.2MHz by using a resistor connected from the RT pin to SGND. The switching frequency ( $f_{SW}$ ) is related to the resistor ( $R_{RT}$ ) connected at the RT pin by the following equation:

$$R_{RT} \cong \frac{21000}{f_{SW}} - 1.7$$

Where  $R_{RT}$  is in k $\Omega$  and  $f_{SW}$  is in kHz. Leaving the RT pin open enables the device to operate at the default switching frequency of 500kHz. See [Table 1](#) for  $R_{RT}$  resistor values for a few common switching frequencies.

### Power Dissipation

The power dissipation inside the module leads to an increase in the junction temperature of the modules. The power loss inside the modules at full load can be estimated as follows:

$$P_{LOSS} = P_{OUT} \times \left[ \frac{1}{\eta} - 1 \right],$$

Where  $\eta$  is the efficiency of the module at the desired operating conditions. See [Typical Operating Characteristics](#) for efficiency, or measure the efficiency to determine total power dissipation. An EE-SIM model is available for the MAXM17633/MAXM17634/MAXM17635, to simulate efficiency and power loss. The junction temperature  $T_J$  of the module can be estimated at any given maximum ambient temperature  $T_A$  from the following equation:

$$T_J = T_A + [\theta_{JA} \times P_{LOSS}]$$

For the MAXM17633/MAXM17634/MAXM17635 evaluation board, the thermal resistance from junction to ambient ( $\theta_{JA}$ ) is 25°C/W. Operating the module at junction temperatures greater than +125°C degrades operating lifetimes.

**Table 1. Selection of Components**

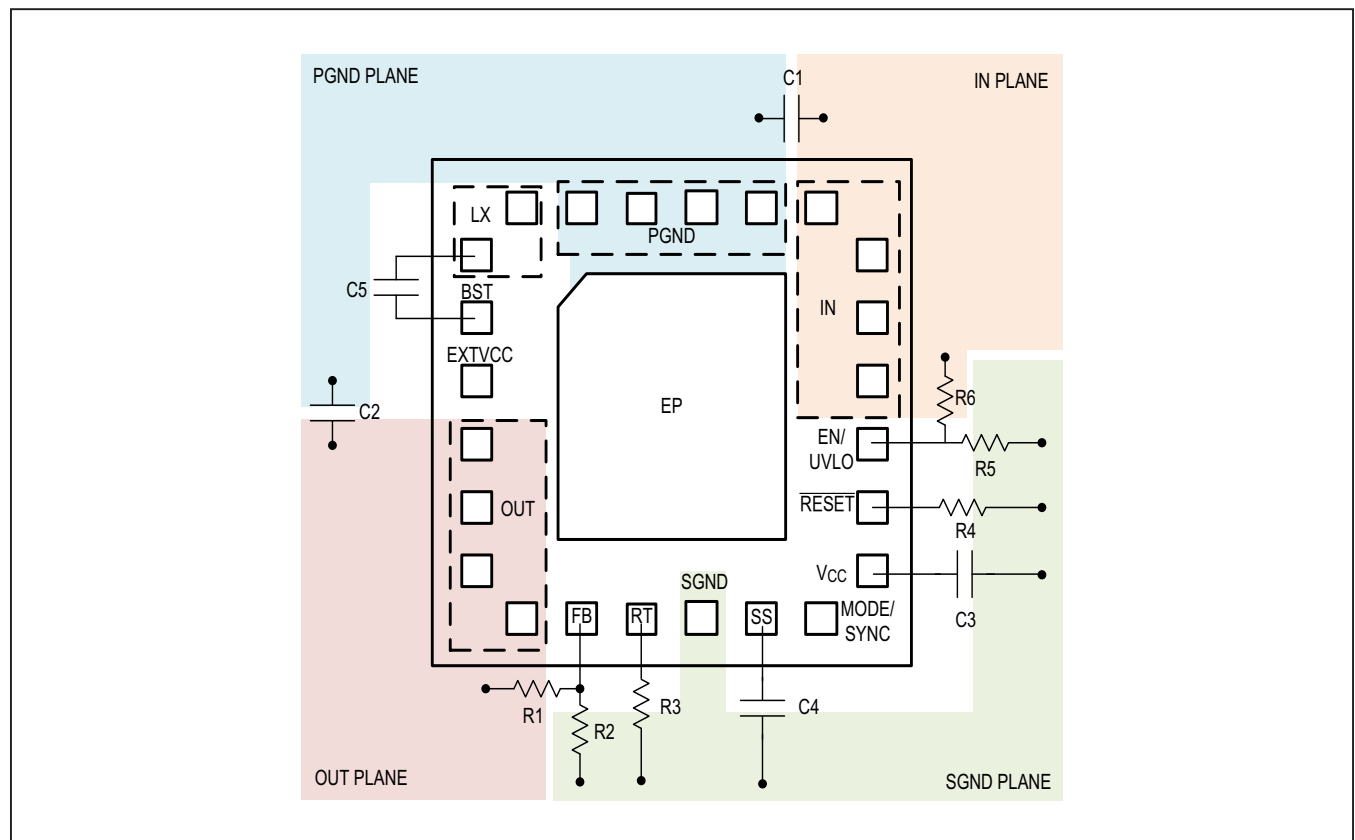
PART NO.	V <sub>INMIN</sub> (V)	V <sub>INMAX</sub> (V)	V <sub>OUT</sub> (V)	f <sub>SW</sub> (kHz)	C <sub>IN</sub>	C <sub>OUT</sub>	R1 (k $\Omega$ )	R2 (k $\Omega$ )	R <sub>RT</sub> (k $\Omega$ )
MAXM17633	4.5	36	3.3	800	1 x 4.7 $\mu$ F 1206 50V GRM31CR71H475KA12#	1 x 47 $\mu$ F 1210 10V GRM32ER71A476KE15#	SHORT	OPEN	24.3
MAXM17634	7	36	5	1000	1x 4.7 $\mu$ F 1206 50V GRM31CR71H475KA12#	1 x 22 $\mu$ F 1210 25V GRM32ER71E226KE15#	SHORT	OPEN	19.1
MAXM17635	4.5	30	0.9	400	2x 4.7 $\mu$ F 1206 50V GRM31CR71H475KA12#	5 x 47 $\mu$ F 1210 10V GRM32ER71A476KE15#	39.2	OPEN	51.1
	4.5	36	1.2	600	2x 4.7 $\mu$ F 1206 50V GRM31CR71H475KA12#	2x 47 $\mu$ F, 10V, 1x 22 $\mu$ F 25V, 1210 GRM32ER71A476KE15#, GRM32ER71E226KE15#	51.1	150	33.2
	4.5	36	1.5	600	2x 4.7 $\mu$ F 1206 50V GRM31CR71H475KA12#	2 x 47 $\mu$ F 1210 10V GRM32ER71A476KE15#	64.9	95.3	33.2
	4.5	36	1.8	600	2x 4.7 $\mu$ F 1206 50V GRM31CR71H475KA12#	1 x 47 $\mu$ F, 10V, 1 x 22 $\mu$ F 25V, 1210 GRM32ER71A476KE15# GRM32ER71E226KE15#	86.6	86.6	33.2
	4.5	36	2.5	700	1 x 4.7 $\mu$ F 1206 50V GRM31CR71H475KA12#	1 x 47 $\mu$ F 1210 10V GRM32ER71A476KE15#	118	64.9	28.3
	4.5	36	3.3	800	1 x 4.7 $\mu$ F 1206 50V GRM31CR71H475KA12#	1 x 47 $\mu$ F 1210 10V GRM32ER71A476KE15#	110	41.2	24.3
	7	36	5	1000	1 x 4.7 $\mu$ F 1206 50V GRM31CR71H475KA12#	1 x 22 $\mu$ F 1210 25V GRM32ER71E226KE15#	215	46.4	19.1
	18	36	12	1800	1 x 2.2 $\mu$ F 1206 50V C3216X7R1H225K160AE	1 x 10 $\mu$ F 1210 50V GRM32ER71H106KA12#	453	36.5	10



Careful PCB layout is critical to achieve low switching losses and clean, stable operation.

- Keep the input capacitors as close as possible to the IN and PGND pins.
- Keep the output capacitors as close as possible to the OUT and PGND pins.

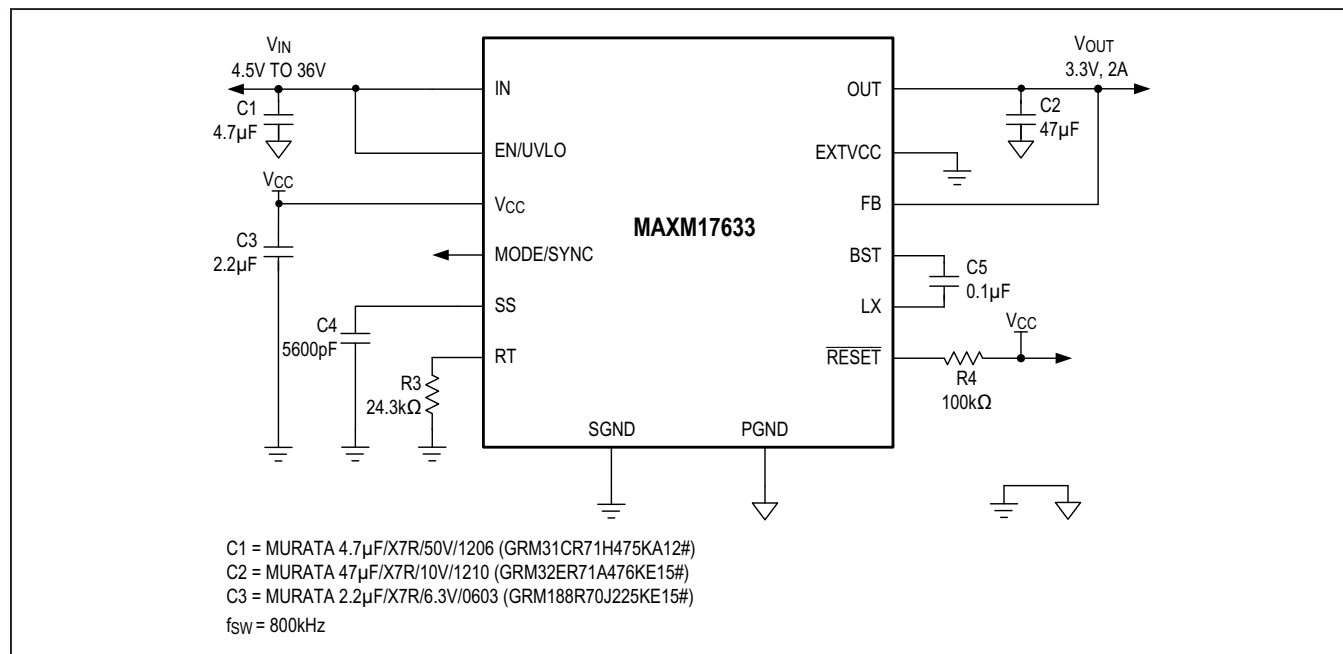
- Keep the resistive feedback divider as close as possible to the FB pin.
- Connect all of the PGND connections to as large as copper plane area as possible on the top and bottom layers.
- Use multiple vias to connect internal PGND planes to the top layer PGND plane.
- Refer to the MAXM17633/MAXM17634/MAXM17635 EV kit layout for first pass success.



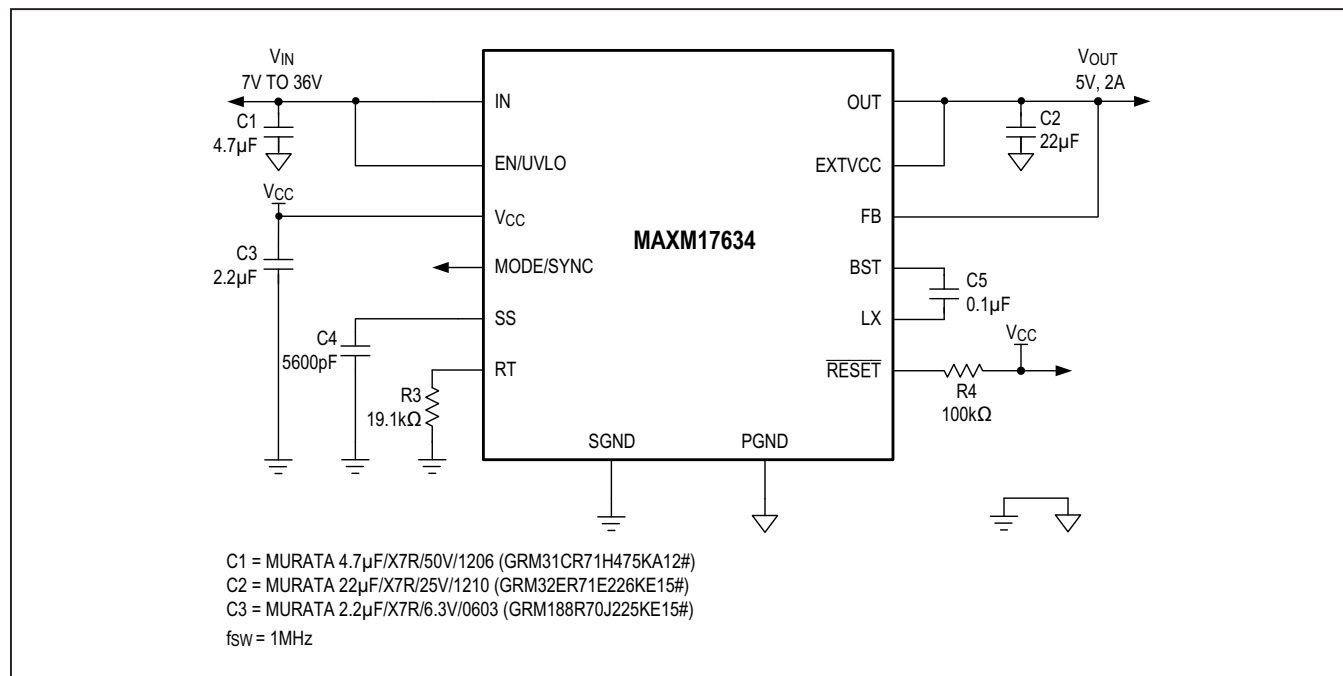
*Figure 3. Layout Guidelines*

## Typical Application Circuits

### Typical Application Circuit—Fixed 3.3V Output

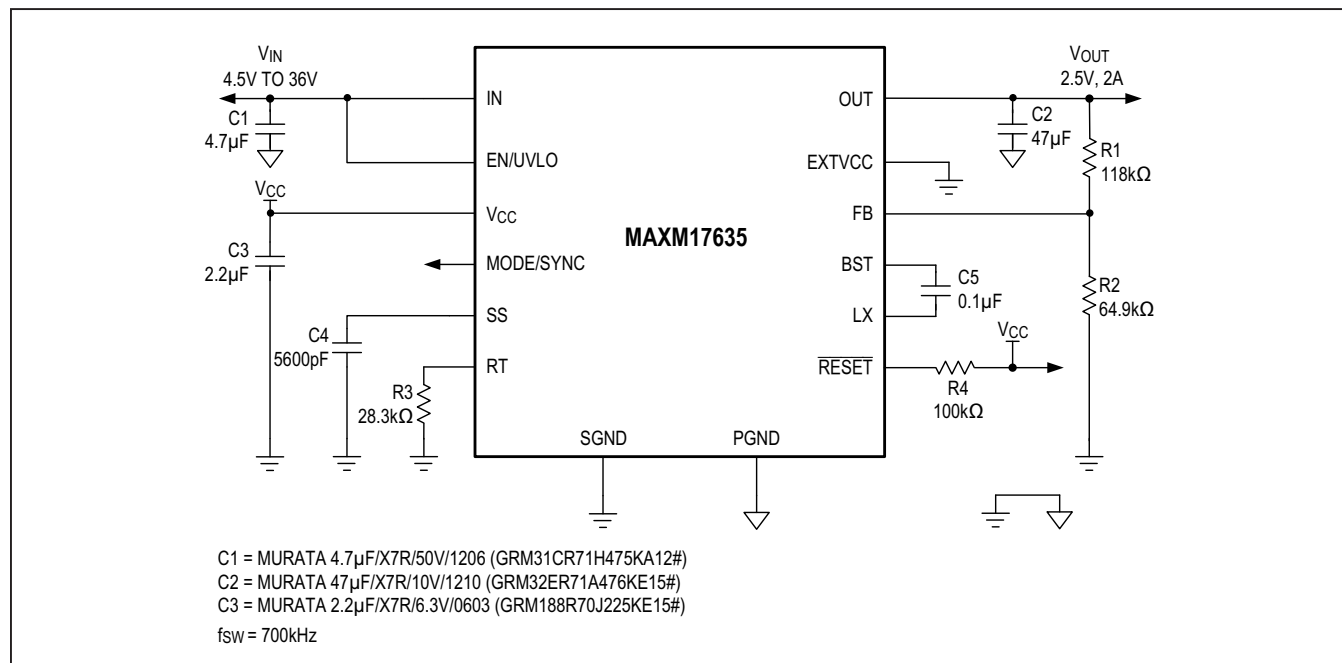


### Typical Application Circuit—Fixed 5V Output

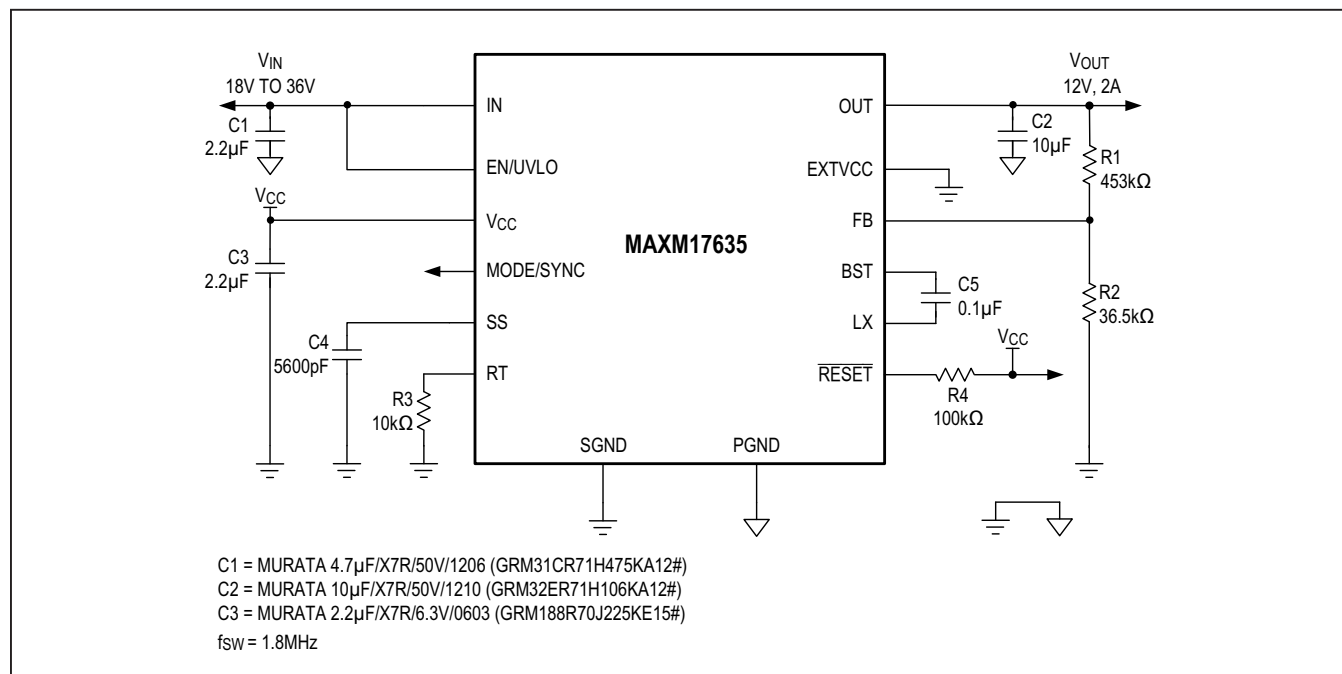


## Typical Application Circuits (continued)

### Typical Application Circuit—Adjustable 2.5V Output



### Typical Application Circuit—Adjustable 12V Output



MAXM17633/MAXM17634/  
MAXM17635

4.5V to 36V, 2A Himalaya uSLIC  
Step-Down Power Modules

## Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	V <sub>OUT</sub>
MAXM17633AMG+	-40°C to +125°C	24-pin 4mm x 4mm x 1.75mm uSLIC package	Fixed 3.3V
MAXM17633AMG+T	-40°C to +125°C	24-pin 4mm x 4mm x 1.75mm uSLIC package	Fixed 3.3V
MAXM17634AMG+	-40°C to +125°C	24-pin 4mm x 4mm x 1.75mm uSLIC package	Fixed 5V
MAXM17634AMG+T	-40°C to +125°C	24-pin 4mm x 4mm x 1.75mm uSLIC package	Fixed 5V
MAXM17635AMG+	-40°C to +125°C	24-pin 4mm x 4mm x 1.75mm uSLIC package	Adjustable
MAXM17635AMG+T	-40°C to +125°C	24-pin 4mm x 4mm x 1.75mm uSLIC package	Adjustable

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T= Tape and reel.

MAXM17633/MAXM17634/  
MAXM17635

4.5V to 36V, 2A Himalaya uSLIC  
Step-Down Power Modules

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/19	Initial release	—

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