QPL9503

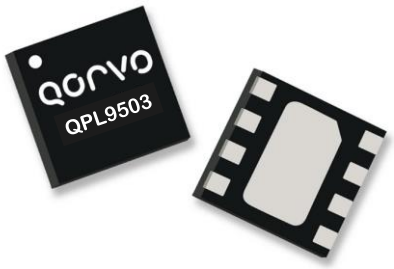
Ultra Low-Noise, Flat Gain LNA

General Description

The QPL9503 is a flat-gain, high-linearity, ultra-low noise amplifier in a small 2 x 2 mm surface-mount package. The LNA provides a gain flatness of 2 dB (peak-to-peak) over a wide bandwidth from 3 to 6 GHz. At 5.5 GHz, the amplifier typically provides 21.6 dB gain, +35.5 dBm OIP3 at a 56mA bias setting, and 0.95 dB noise figure. The LNA can be biased from a single positive supply ranging from 3.3 to 5 volts. The device is housed in a green/RoHS-compliant industry-standard 2x2 mm package.

The QPL9503 is internally matched using a high performance E-pHEMT process and only requires five external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors and a bias resistor going to pin 1. This LNA integrates a shut-down biasing capability to allow for operation in TDD applications.

The QPL9503 is optimized for linear performance across the 3 to 6 GHz frequency band but can operate down to 600 MHz.

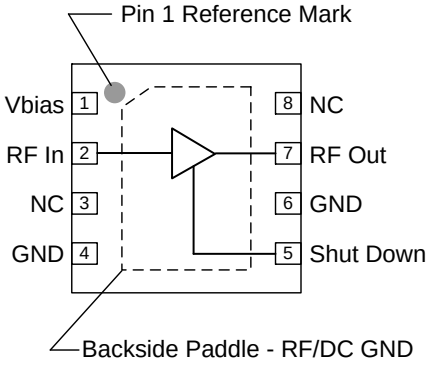


8 Pin 2X2 mm DFN Package

Product Features

- 0.6-6 GHz Operational Bandwidth
- Ultra low noise figure, 0.95 dB NF @ 5.5 GHz
- Bias adjustable for linearity optimization
- 35.5 dBm OIP3 at 65mA I_{DD}
- Shut-down mode pin with 1.8V TTL logic
- Unconditionally stable
- Integrated shutdown control pin
- Maintains OFF state with high Pin drive
- +3V to +5V supply; does not require -Vgg

Functional Block Diagram



Top View

Applications

- 4.5G, 5G Massive MIMO
- Repeaters / DAS
- Mobile Infrastructure
- LTE-U / LAA
- L-band, S-band, C-band radios
- General Purpose Wireless
- TDD or FDD systems

Ordering Information

Part No.	Description
QPL9503SR	100 pcs on 7” reel
QPL9503TR7	2500 pcs on 7” reel
QPL9503EVB-01	5-6GHz Tuned Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150°C
Supply Voltage (V_{DD})	+7 V
RF Input Power, CW, 50Ω, T=25°C	+30 dBm
RF Input Power, WCDMA, 10dB PAR	+27 dBm
RF Input Power, CW, OFF State	+30 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	3.3	5.0	5.25	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

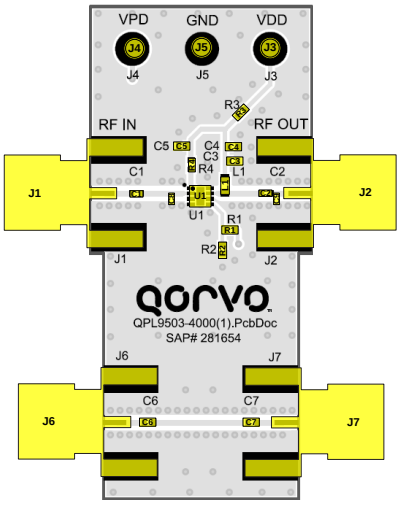
Electrical Specifications

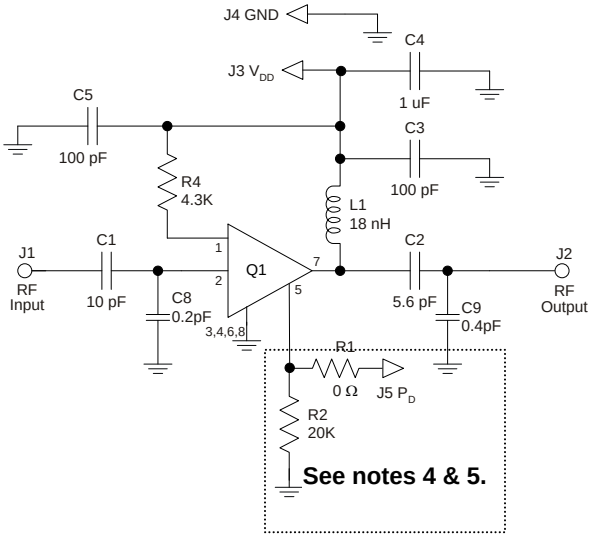
Test conditions unless otherwise noted: V_{DD} =+5V, Temp=+25°C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		600		6000	MHz
Test Frequency			5500		MHz
Gain		18.5	21.6	22.5	dB
Input Return Loss			10		dB
Output Return Loss			9		dB
Noise Figure (1)			0.9	1.3	dB
Output P1dB			+19		dBm
Output IP3	Pout=+5 dBm/tone, Δf=1 MHz	+30	+35.5		dBm
Power Shutdown Control (pin 5)	On state	0		0.63	V
	Off state (Power down)	1.17		V_{DD}	V
Current, I_{DD}	On state	35	56	90	mA
	Off state (Power down)		3		mA
Shutdown pin current, I_{SD}	V_{PD} ≥ 1.17 V		140		µA
Switching Speed	LNA ON to OFF		20		ns
	LNA OFF to ON		400		ns
Thermal Resistance, θ_{jc}	channel to case		48		°C/W

Note:
1) Noise figure data has input trace loss de-embedded.

QPL9503 Evaluation Board





Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. R3 (0 Ω jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. For TDD Applications: R1 = 20K & R2 = 0Ω
5. For FDD Applications: R1 = 20K 'OR' Pin 5 tied to ground. R2 = DNP/Omitted
6. A through line is included on the evaluation board to de-embed the board losses.
7. R4 sets the current draw. Can be changed for the desired bias point.

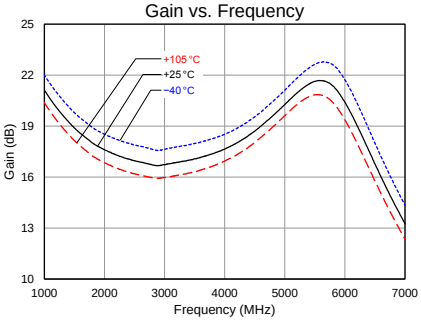
Bill of Material – QPL9503 Evaluation Board

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	Qorvo	
U1	n/a	Ultra Low Noise, Flat Gain LNA	Qorvo	QPL9503
R4	4.3K	Resistor, Chip, 0402, 5%, 1/16W	various	
R2	20K	Resistor, chip, 0402, 5%, 1/16W	various	
R1, 3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
L1	18 nH	Inductor, 0402, 5%, coil	Coilcraft	0402CS-18NXJL
C1	10 pF	CAP, 0402, +/-1%, 50V	Murata	GJM1555C1H100FB01D
C2	5.6 pF	CAP, 0402, +/-0.1pF, 25V	AVX	04023J6R8BBSTR
C8	0.2 pF	CAP, 0402, +/-0.05pF, 50V	Murata	GJM1555C1HR20WB01
C9	0.4 pF	CAP, 0402, +/-0.05pF, 50V	AVX	04023J0R4ABSTR
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	
C3, C5, C6, C7	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	various	

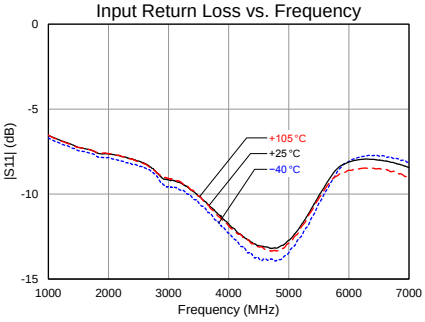
Performance Plots – QPL9503 Evaluation Board

Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD} = 65mA, Temp=+25°C. Noise figure data has input trace loss de-embedded.

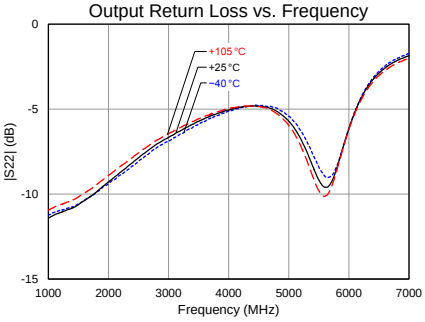
Gain vs. Frequency



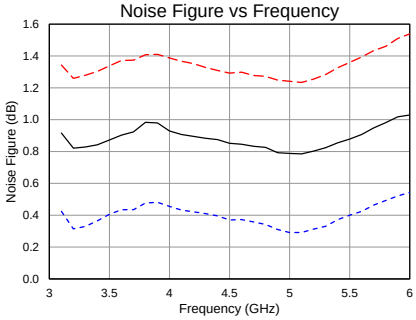
Input Return Loss vs. Frequency



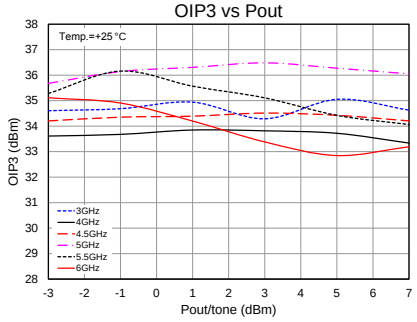
Output Return Loss vs. Frequency



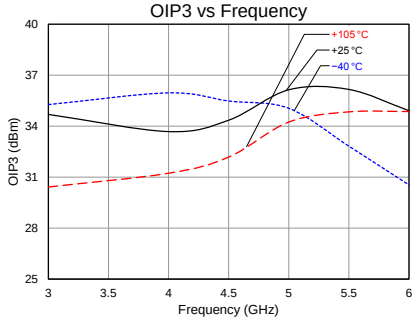
Noise Figure vs Frequency



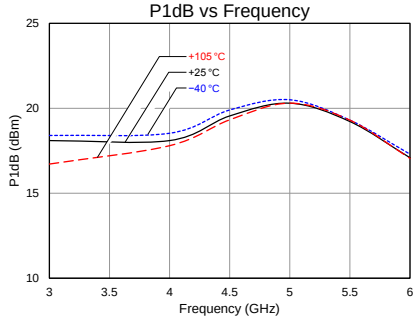
OIP3 vs Pout



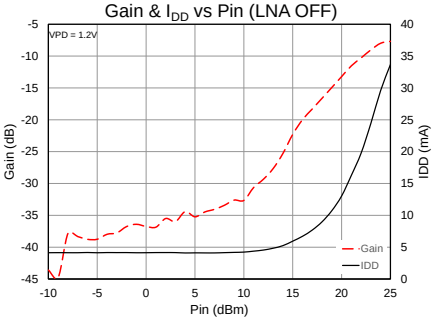
OIP3 vs Frequency



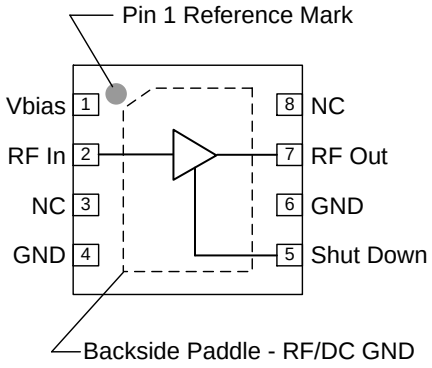
P1dB vs Frequency



Gain & I_{DD} vs Pin (LNA OFF)



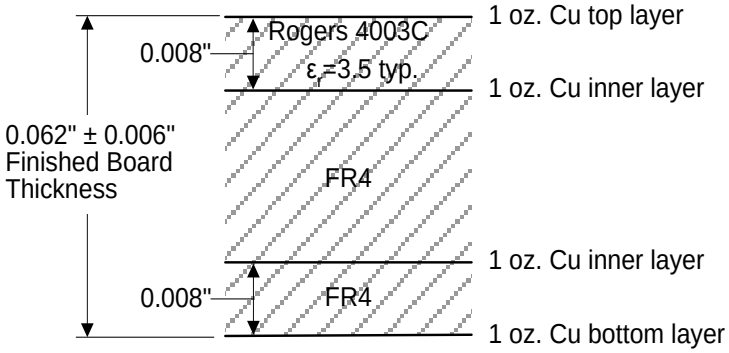
Pin Configuration and Description



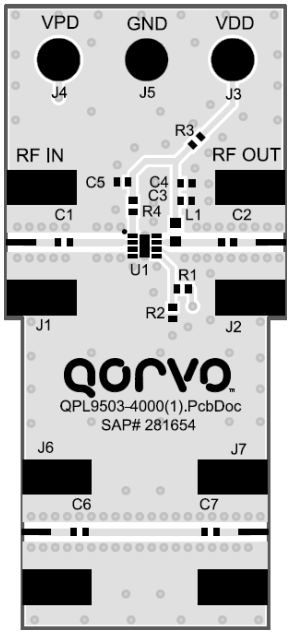
Pin No.	Label	Description
1	Vbias	Sets the Icq bias point for the device.
2	RF In	RF Input pin. A DC Block is required.
5	Shut Down	A high voltage(>1.17V) turns off the device. If the pin is pulled to ground or driven with a voltage less than 0.63V, then the device will operate under LNA ON state.
7	RF Out / DCBias	RF Output pin. DC bias will also need to be injected through a RF bias choke/inductor for operation.
3 ,8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle, 4, 6	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

Qorvo PCB 281645 Material and Stack-up

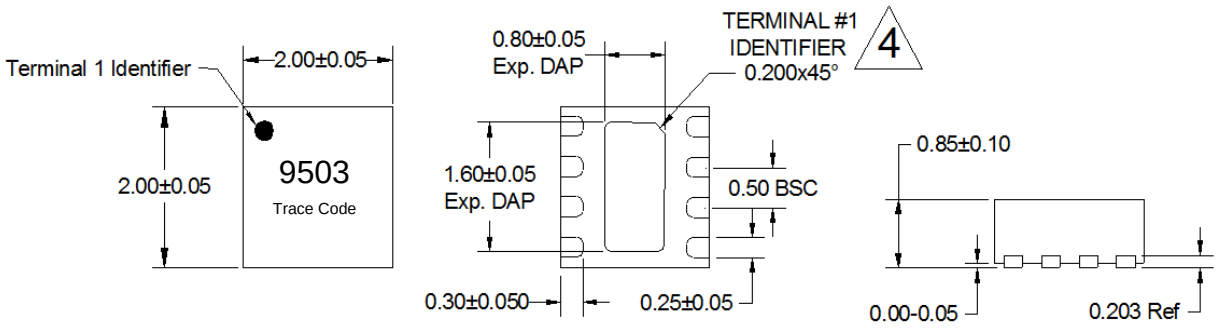


50 ohm line dimensions: width = 0.0182”, spacing = 0.020”



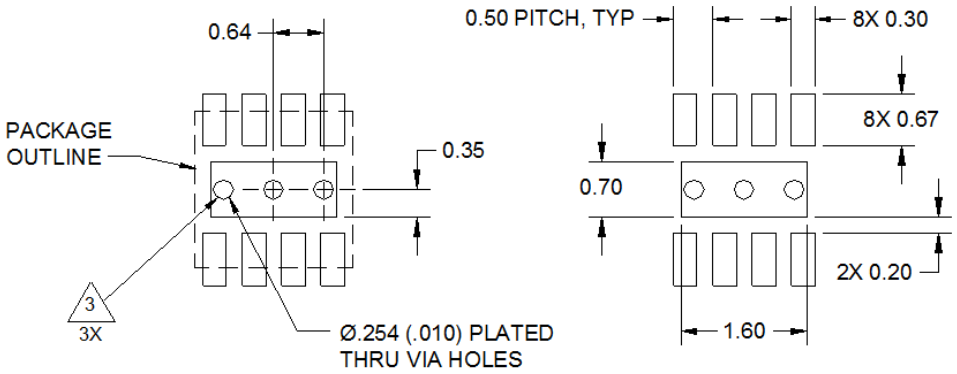
Mechanical Information

Package Marking and Dimensions



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ESDA / JEDEC JS-001-2014
ESD – Charged Device Model (CDM)	C3	ESDA / JEDEC JS-002-2014
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering process.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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