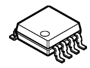
SYSTEM RESET IC WITH WATCHDOG TIMER

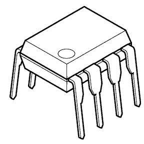
■ GENERAL DESCRIPTION

The NJU7291 is a system reset IC with watchdog timer. It can detect an instantaneous voltage drop and break, and generates a reset signal. The NJU7291 provides a fail-safe function with an internal watchdog timer on various microcomputer systems. It is available in 8-lead DIP and MSOP (TVSP) packages.

■ PACKAGE OUTLINE



NJU7291RB1



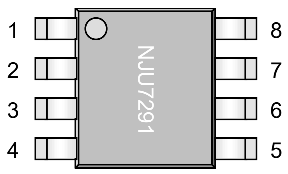
NJU7291D

■ FEATURES

- Supply Voltage Range : V^+ = 2.5 V to 7.0 V
- RESET Detection Voltage : V_{RL} = ± 1.0 % and Adjustable Detection Voltage with External Resistance
- Rising RESET Hold Time and Watchdog Timer RESET Time Setting Ratio = 30 : 1
- Configurable Watchdog Timer Watching Time Independent Setting
- Configurable Stopping Watchdog Timer Function
- Package Outline : MSOP8 (TVSP8)*, DIP8

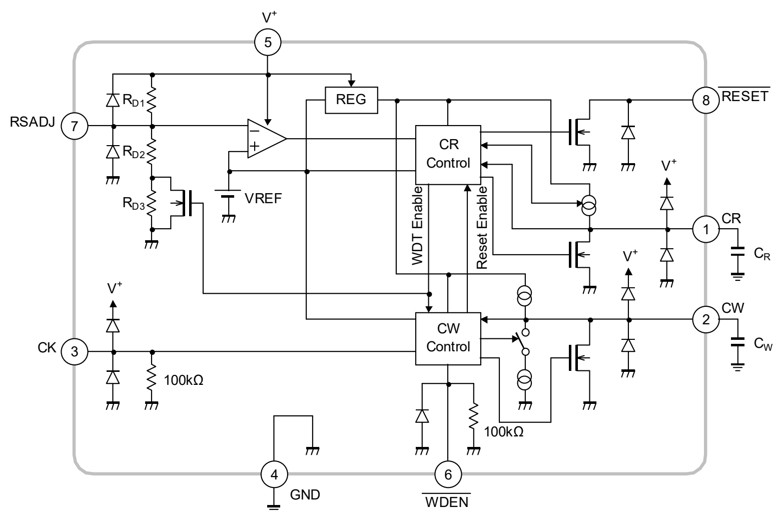
*MEET JEDEC MO-187-DA / THIN TYPE

■ PIN CONFIGRATION / PIN FUNCTION



PIN No.	PIN NAME	FUNCTION
1.	CR	External Capacitor Pin for Setting Reset Pin
2.	CW	External Capacitor Pin for Clock Pin
3.	CK	Clock Input Pin
4.	GND	Ground Pin
5.	V^+	Power Supply Pin
6.	$\overline{\text{WDEN}}$	External Register Pin for Setting Watchdog Timer Pin (Active Low)
7.	RSADJ	External Register Pin for Setting Reset Pin
8.	$\overline{\text{RESET}}$	Reset Signal Output Pin (Active Low)

■ BLOCK DIAGRAM



■ DETECT VOLTAGE LINE UP

DEVICE NAME	V_{RL}	PKG	STATUS
NJU7291RB1-03	3.0V	MSOP8	MP
NJU7291RB1-46	4.6V	MSOP8	PLAN
NJU7291D46	4.6V	DIP8	MP

■ ABSOLUTE MAXIMUM RATING

(T_a = 25 °C)

PARAMETER	SYMBOL	TEST CONDITION	RATINGS	UNIT
Supply Voltage	V^+		8.0	V
Detect Voltage Input voltage	V_{RSADJ}		8.0	V
Clock Input Voltage	V_{CK}	(*1)	8.0	V
$\overline{\text{WDEN}}$ Input Voltage	$V_{\overline{WDEN}}$	(*1)	8.0	V
$\overline{\text{RESET}}$ Output Voltage	$V_{\overline{RESET}}$		8.0	V
$\overline{\text{RESET}}$ Output Sink Current	$I_{\overline{RESET}}$		20	mA
Power Dissipation	P_D	MSOP8(TVSP8) (*2) DIP8(*3)	470 500	mW
Operating Temperature	T_{opr}		- 40 to + 85	°C
Storage Temperature	T_{stg}		- 40 to +125	°C

(*1) : When input voltage is less than +8V, the absolute maximum control voltage is equal to the input voltage.

(*2) : Mounted on glass epoxy board (76.2 × 114.3 × 1.6mm: 2Layers FR-4)

(*3) : Device itself

■ RECOMMENDED OPERATING CONDITION

(T_a = 25 °C)

PARAMETER	SYMBOL	TEST CONDITION	RATINGS	UNIT
Supply Voltage	V^+		2.5 to 7.0	V
Detect Voltage Input voltage	V_{RSADJ}		0 to V^+	V
Clock Input Voltage	V_{CK}		0 to V^+	V
$\overline{\text{WDEN}}$ Input Voltage	$V_{\overline{WDEN}}$		0 to V^+	V

■ ELECTRICAL CHARACTERISTICS

< Voltage Detector Block >

Unless otherwise noted, ($V^+ = V_{RL} + 0.3V$, T_a = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Reset Voltage	V_{RL}		- 1.0 %	-	+1.0 %	V
Hysteresis Voltage	V_{HYS_RS}	$V_{HYS\_RS} = V_{RH}$ (*4) - V_{RL}	63	90	117	mV
Reference Voltage	V_{TRS}		0.95	1.00	1.05	V
Average temperature coefficient of Reference Voltage	$\Delta V_{TRS}/\Delta T_a$	T_a = - 40 °C to + 85°C	-	±200	-	ppm/°C
Output Delay Hold time	T_{PR}	C_R = 0.01µF	1.9	2.5	3.5	ms
CR Pin Charge Current at Detect Voltage	I_{CRD}	V_{CR} = 0.05V	3	4	5	µA
CR Pin Threshold Voltage at Reset Release	V_{TCRD}	V_{CW} = 0.05V	0.95	1.00	1.05	V

(*4) : V_{RH} : Release Voltage

■ ELECTRICAL CHARACTERISTICS

< Watch Dog Timer Block >　　Unless otherwise noted, ($V^+ = V_{RL}+0.3V$, $T_a = 25°C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Input Threshold Voltage	V_{TCK}		0.6	0.9	1.2	V
Clock Input Pulse With	T_{CKW}		0.05	-	-	ms
Clock Input Cycle	T_{CK}		0.1	-	-	ms
WDT Monitor Time	T_{WD}	C_W = 0.01µF	1.5	2.0	2.8	ms
CW Pin Charge Current	I_{CW}	V_{CW} = 0.05V	3	4	5	µA
CW Pin Threshold Voltage at WDT Reset	V_{TCWH}	V_{CR} = 0.05V	0.95	1.00	1.05	V
CW Pin Discharge Current at Clock Detect	I_{CWL}	V_{CW} = 0.5V	30	39	48	µA
CW Pin Threshold Voltage at Changing Charge	V_{TCWL}	V_{CR} = 0.05V	0.18	0.20	0.23	V
WDT Reset Time	T_{WR}	C_R = 0.01µF	0.063	0.083	0.117	ms
CR Pin Charge Current at Timer Reset	I_{CRW}	V_{CR} = 0.05V	45	60	75	µA
CR Pin Threshold Voltage at Release Timer Reset	V_{TCRW}	V_{CW} = 0.05V	0.48	0.50	0.53	V
$\overline{WDEN}$ Pin Threshold Voltage at Stop WDT	V_{TWDIS}		1.6	-	V^+	V
$\overline{WDEN}$ Pin Threshold Voltage at Release Stop WDT	V_{TWEN}		0	-	0.3	V

< Output Block >　　Unless otherwise noted, ($V^+ = V_{RL}+0.3V$, $T_a = 25°C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$\overline{RESET}$ Output Voltage at " L " Output	V_{RSTL}	$I_{\overline{RESET}}$ = 0.5mA, V_{RSADJ} = 0V	-	0.2	0.4	V
$\overline{RESET}$ Output Sink Current at " L " Output	I_{RST}	$V_{\overline{RESET}}$ = 0.5V, V_{RSADJ} = 0V	5	10	-	mA
$\overline{RESET}$ Minimum Operating Voltage	V_{OPL}	$V_{\overline{RESET}}$ = 0.4V, R_{pu} (*5) = 330kΩ	-	0.8	1.2	V

(*5) : R_{pu} : $\overline{RESET}$ Pull up Resistor

< General Characteristics >　　Unless otherwise noted, ($V^+ = V_{RL}+0.3V$, $T_a = 25°C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{SS}	WDT Active	-	170	250	µA

■ TIMING CHART

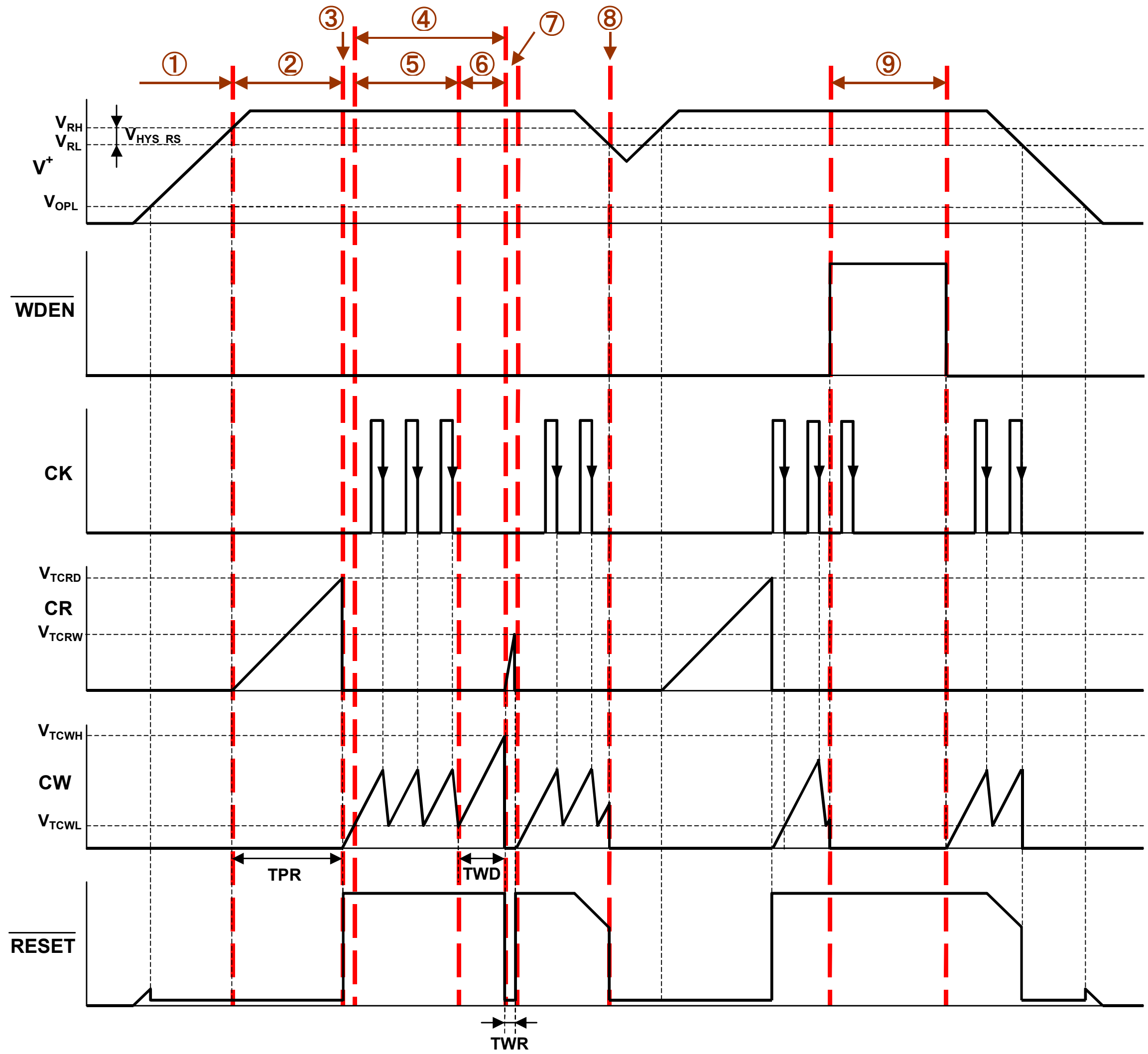


Fig. 1 NJU7291 Timing Chart

■ OPERATING EXPLANATION

● Output Delay Hold Period

① Initial Condition

Under this condition, V^+ is less than release voltage: (V^+<V_{RH} (V_{RH} =V_{RL}+V_{HYS_RS})). The CR Pin and CW Pin are 0(zero) V. (V_{CR}=0V, V_{CW}=0V) and RESET level is "L".

② In the case of V^+ exceeding the Release Voltage: V_{RH}.

The C_R at the CR Pin is charged by "CR Pin Charge Current at Detect Voltage": I_{CRD} (typ. 4μA), then V_{CR} voltage rises. The CW Pin is 0(zero) V. And RESET level keeps "L". The condition returns to the state of ① when V^+ decreases less than release voltage: V_H.

③ In the case of the CR Pin Capacitor Voltage: V_{CR} reaching to the CR Pin Threshold Voltage at Release Timer Reset: V_{TCRD} (typ. 1V), after release.

The RESET level becomes from "L" to "H". At this time, "Output Delay Hold Time": T_{PR} is the following period: Time to becoming of RESET ="H" from V^+=V_{RH}.

And C_R at the CR Pin is discharged then the CR Pin Voltage becomes 0(zero) V. And the C_W at the CW Pin is charged by "CW Pin Charge Current": I_{CW} (typ. 4μA), then the V_{CW} voltage rises. From this condition, "Reset Voltage": V_{RL} will be detectable.

● WDT Monitor Period

④ The standby condition of the clock CK falling edge detection

The C_W is charged by charge current: I_{CW}. It becomes possible to detect the clock CK falling edge with greater than equal to the C_W Pin threshold voltage V_{TCWL} (typ. 0.205V).

⑤ In the case of clock CK falling edge detection

When it detects the clock CK falling edge, CW capacitor is changed to discharging mode by I_{CWL} (typ. 36μA) from charging mode by I_{CW}, and the CW Pin voltage: V_{CW} falls. Then, when the CW Pin voltage: V_{CW} reaches the threshold voltage: V_{TCWL}, it changes to charging mode by I_{CW}, and the CW Pin voltage: V_{CW} rises.

⑥ In the case of clock CK falling edge undetection

When the voltage V_{CW} reaches the CW Pin threshold voltage V_{TCWH} (TYP: 1 V) at the watchdog timer reset without detecting the falling edge of the clock CK while the capacitor CW is being charged with the charging current I_{CW}, the $\overline{RESET}$ changes from "H" to "L", discharges capacitor CW, and CW Pin voltage becomes V_{CW} = 0V.

Then, charging of capacitor CR starts with CR Pin Charge Current at Timer Reset I_{CRW} (TYP: 60 μA) and voltage V_{CR} starts to rise.

The WDT Monitor Time T_{WD} is the time from when the CW Pin voltage V_{CW} reaches the V_{TCWH} from the V_{TCWL}, without detecting the falling edge of the clock.

● WDT Reset Period

⑦ Until the CR Pin Voltage: V_{CR} exceeds "Timer Reset Release Threshold Voltage": V_{TCRW} (typ. 0.5V).

$\overline{RESET}$ = "L" is held until the voltage V_{CR} reaches the V_{TCRW} after charging the capacitor CR with the I_{CRW}.

When the voltage V_{CR} exceeds the V_{TCRW}, $\overline{RESET}$ changes from "L" to "H" to discharge the capacitor CR and the CR Pin voltage becomes V_{CR} = 0 V. Then, the capacitor CW starts to be charged with the I_{CW}, and the watchdog timer monitoring period is restored. The WDT Monitor Time T_{WD} is the time holding $\overline{RESET}$ ="L".

● Detection of Reset Voltage

⑧ In the case of Supply Voltage: V^+ < Reset Voltage: V_{RL}

At the watchdog timer monitoring period and the watchdog timer reset period, the reset signal outputs $\overline{RESET}$ ="L" at this condition. The CR Pin and CW Pin become V_{CR}=0V and V_{CW}=0V to discharge the C_R and C_W.

Then the operating condition returns to the state of ①.

● Stop of WDT Function

⑨ In the case of WDT Timer Setting Pin: $\overline{WDEN}$="H"

Setting to $\overline{WDEN}$="H", WDT Monitor operation is stopped. At this time, the C_W is discharged and V_{CW} becomes 0V.

If Power Supply: V^+ is greater than Reset Voltage: V_{RL}, $\overline{RESET}$ is kept "H" level. Setting to $\overline{WDEN}$="L" or OPEN, the C_W charge operation starts and returns WDT Monitor operation.

Also, when it is set the $\overline{WDEN}$="H" during the WDT Reset period, the WDT Monitor operation stops after the elapse of the WDT Reset Time T_{WR}. When you do not want to use WDT, the Pin handling is the following.

$\overline{WDEN}$="H", CK Pin =GND or OPEN, and CW Pin =OPEN.

■ External Parts Setting

● C_R for Reset Time Setting

The C_R set the following two parameters: "Output Delay Hold Time": T_{PR} and "WDT Reset Time": T_{WR}.
The T_{PR} is calculated the following.

$$T_{PR} = \frac{C_R}{I_{CRD}} \cdot V_{TCRD} \qquad \cdots\cdots\cdots \quad \text{<1>}$$

From formula<1>, C_R is calculated as follows:

$$C_R = \frac{I_{CRD}}{V_{TCRD}} \cdot T_{PR} \qquad \cdots\cdots\cdots \quad \text{<2>}$$

The C_R value can calculate by the following formula.
The CR Pin Charge Current at Detect Voltage: I_{CRD} is 4µA (typ.). The CR Pin Threshold Voltage at Reset Release: V_{TCRD} is 1V (typ.).

$$C_R = 4 \times T_{PR} \times 10^{-6} \quad \text{[F]} \qquad \cdots\cdots\cdots \quad \text{<3>}$$ The unit of T_{PR} is [s] (second).

The WDT Reset Time: T_{WR} is decided depending on the value of capacitor: C_R. The T_{WR} is calculated the following.

$$T_{WR} = \frac{C_R}{I_{CRW}} \cdot V_{TCRW} \qquad \cdots\cdots\cdots \quad \text{<4>}$$

The WDT Reset Time: T_{WR} can calculate by the following formula.
The CR Pin Charge Current at Timer Reset: I_{CRW} is 60µA (typ.). The CR Pin Threshold Voltage at Release Timer Reset: V_{TCRW} is 0.5V (typ.).

$$T_{WR} = \frac{C_R}{120} \times 10^{6} \quad \text{[s]} \qquad \cdots\cdots\cdots \quad \text{<5>}$$

From formula<3> and <5>, the relation between T_{PR} and T_{WR} becomes the following.

$$T_{WR} = \frac{T_{PR}}{30} \quad \text{[s]} \qquad \cdots\cdots\cdots \quad \text{<6>}$$

From above mention, the relation between C_R, T_{PR} and T_{WR} becomes fig 2.

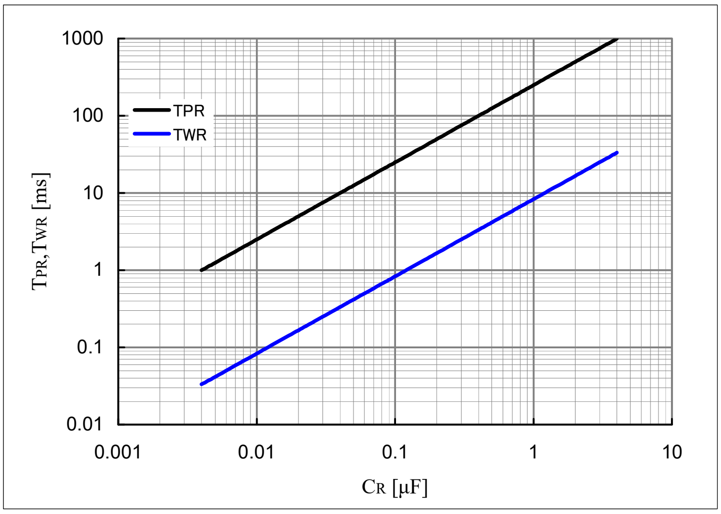


Fig 2. Output Delay Hold Time(T_{PR}) and WDT Reset Time(T_{WR}) vs.C_R for Reset Time Setting

● C_W for Clock Monitor Time Setting

The C_W set the following: "WDT Monitor Time": T_{WD}.
The T_{WD} is calculated the following.

$$T_{WD} = \frac{C_W}{I_{CW}} \cdot (V_{TCWH} - V_{TCWL}) \cdot\cdot \quad \text{<7>}$$

From formula<7>, C_W is calculated as follows:

$$C_W = \frac{I_{CW}}{V_{TCWH} - V_{TCWL}} \cdot T_{WD} \cdot\cdot\cdot\cdot \quad \text{<8>}$$

The C_W value can calculate by the following formula.The CW Pin Charge Current: I_{CW} is 4μA (typ.). The CW Pin Threshold Voltage at WDT Reset: V_{TCWH} is 1V (typ.). The CW Pin Threshold Voltage at Changing Charge: V_{TCWH} is 0.2V (typ.).

$$C_W = 5 \times T_{WD} \times 10^{-6} \text{ [F]} \cdot\cdot\cdot\cdot\cdot\cdot \quad \text{<9>}$$

The unit of T_{WD} is [s] (second).

The relation between C_W and T_{WD} becomes Fig 3.

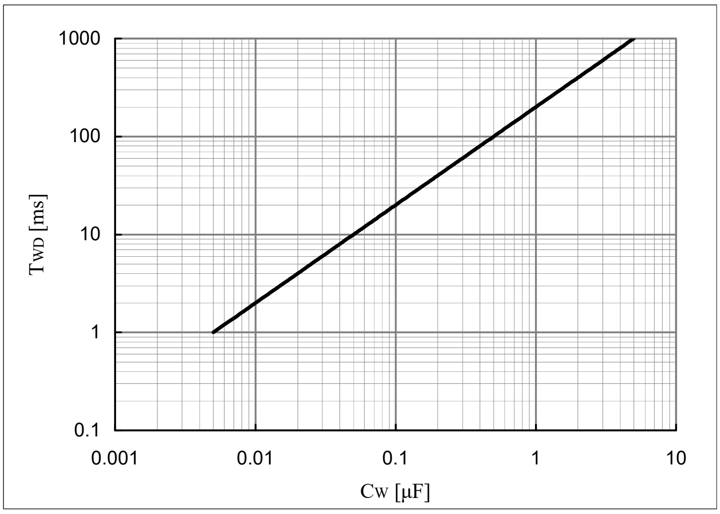
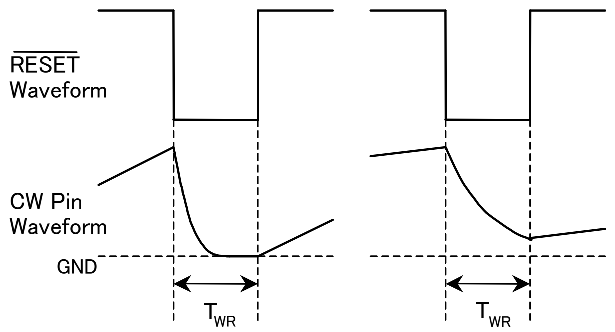


Fig 3. WDT Monitor Time(T_{WD}) vs.C_W for Clock Monitor Time Setting

— PRECAUTION —

The C_W discharge time becomes long as with the increasing of C_W as shown in Fig 4. For this reason, if the C_W discharge is not completed within the TWR, a malfunction occurs in next watchdog timer operation.

To prevent this malfunction, you should set the C_R value greater than one-fifth of C_W value.



(a) at C_W fully discharge (b) at C_W faulty discharge

Fig 4. WDT Reset Time (T_{WR}) and CW Pin Voltage Waveform

- External R_1/R_2 for Reset Voltage Setting

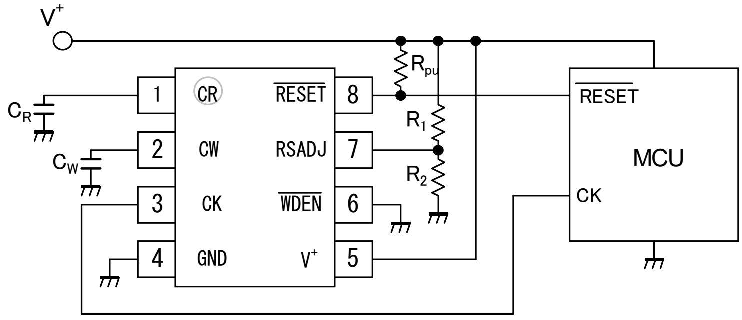


Fig 5. Application example using external resistance for Reset Voltage Setting

You should consider IC internal resistance for reset voltage setting when setting reset voltage using external resistance R_1/R_2 like Fig 5. The Fig 6 shows the block including IC internal resistance for reset voltage setting.

The Reset Voltage: V_{RL} and Release Voltage: V_{RH} are calculated the following using external resistance R_1/R_2.

[Reset Voltage: V_{RL} (Transistor M1 is OFF)]

$$V_{RL} = \left\{ \frac{R_{D1}}{R_{D2}+R_{D3}} \cdot \frac{1+\left(R_{D2}+R_{D3}\right)/R_2}{1+R_{D1}/R_1} + 1 \right\} \cdot V_{REF} \quad \cdot \quad \text{<10>}$$

[Release Voltage: V_{RH} (Transistor M1 is ON)]

$$V_{RH} = \left(\frac{R_{D1}}{R_{D2}} \cdot \frac{1+R_{D2}/R_2}{1+R_{D1}/R_1} + 1 \right) \cdot V_{REF} \quad \cdot\cdot\cdot \quad \text{<11>}$$

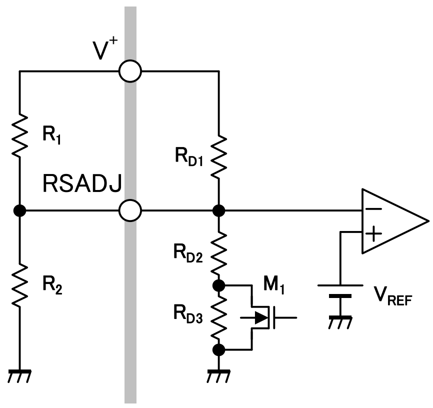


Fig 6. Reset Voltage Detection Block

From Reset Voltage V_{RL} and Release Voltage V_{RH} , Hysteresis Voltage V_{HYS_RS} is calculated as follows:

[Hysteresis Voltage: V_{HYS_RS}]

$$V_{HYS\_RS} = \frac{R_{D1} \cdot R_{D3}}{R_{D2} \cdot \left(R_{D2}+R_{D3}\right) \cdot \left(1+R_{D1}/R_1\right)} \cdot V_{REF} \quad \cdot\cdot\cdot \text{<12>}$$

How to decide the R_1/R_2 value you want to set arbitrary reset voltage V_{RL} is as follows.

First, you should decide R_1 value. At this time, the Hysteresis Voltage is calculated by formula<12>. Next, R2 decides The R_2 value is decided by applying V_{RL} obtained from formula <10> to formula following <13>. Because the $R_{D1}/R_{D2}/R_{D3}$ are different depending on the reset detection voltage rank, you should confirm separately to our sales department. The V_{REF} is equal to voltage detection reference voltage, therefore V_{REF}=1V.

$$R_2 = \frac{R_{D2}+R_{D3}}{\frac{R_{D2}+R_{D3}}{R_{D1}} \cdot \left(V_{RL}-1\right) \cdot \left(1+\frac{R_{D1}}{R_1}\right) - 1} \quad \cdot\cdot\cdot\cdot \quad \text{<13>}$$

Ex. Using NJU7291x-03

NJU7291x-03 Reset Voltage: V_{RL} is set at 3.0V (initial value). The IC internal resistance: R_{D1} to R_{D3} for reset voltage setting is shown Table 1. (4.6V rank is referred to Table 2)

Applying these values to the formula <10> to <13>, the formula <14> to <17> is obtained. V_{REF} = 1[V] and a resistance unit is [kΩ].

[Reset Voltage: V_{RL}]

$$V_{RL} = 2 \cdot \frac{1 + 209/R_2}{1 + 418/R_1} + 1 \quad [V] \qquad \cdots\cdots\cdot \quad <14>$$

[Release Voltage: V_{RH}]

$$V_{RH} = 2.09 \cdot \frac{1 + 200/R_2}{1 + 418/R_1} + 1 \quad [V] \qquad \cdots\cdots\cdot \quad <15>$$

[Hysteresis Voltage: V_{HYS_RS}]

$$V_{HYS\_RS} = \frac{0.09}{1 + 418/R_1} \quad [V] \qquad \cdots\cdots\cdot \quad <16>$$

[Calculation of R2]

$$R_2 = \frac{209}{0.5 \cdot (V_{RL} - 1) \cdot \left(1 + \frac{418}{R_1}\right) - 1} \quad [k\Omega] \qquad \cdot\cdot \quad <17>$$

Table1. IC internal resistance value of the reset voltage detection block [NJU7291x-03]

R_{D1}	418 kΩ
R_{D2}	200 kΩ
R_{D3}	9 kΩ

Table2. IC internal resistance value of the reset voltage detection block [NJU7291x-46]

R_{D1}	480 kΩ
R_{D2}	130 kΩ
R_{D3}	3.342 kΩ

■ Attention in the use

If some noise occurs on the power line, the power supply voltage: V^+ drop below reset voltage: V_{RL} momentary. Therefore, it has possibility to output the reset signal (RESET="L").
In that case, it should be inserted a capacitor: C_S between RSADJ Pin and GND for filtering.
However, the voltage rising time at RSADJ Pin is slowed shown as Fig 8.

In case of inserting the C_S, the Output Delay Hold Time is calculated as follows.

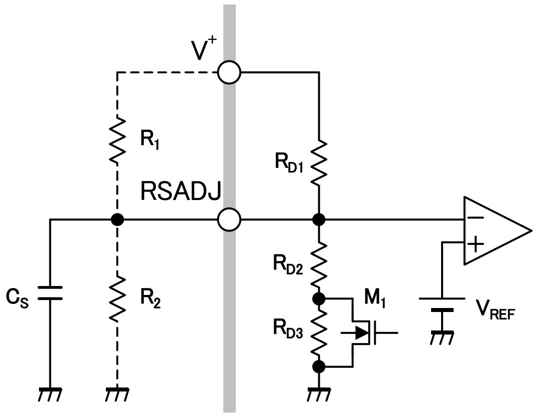


Fig.7 Measures against power line noise

$$T_{DPR} = \tau \cdot \ln\left\{ 1 \Big/ \left(1 - \frac{V_{TRS}}{V^+} \cdot \frac{R_{D1} + R_{D2}}{R_{D2}} \right) \right\} \quad \cdots \quad <18>$$

$$\tau = \frac{R_{D1} \cdot R_{D2}}{R_{D1} + R_{D2}} \cdot C_S \quad \cdots\cdots\cdots \quad <19>$$

The Output Delay Hold time without C_S is assumed to be T_{PR0}.

$$T_{PR} = T_{DPR} + T_{PR0} \quad \cdots\cdots \quad <20>$$

From formula<1>, the T_{PR0} can be calculated as follows:

$$T_{PR0} = \frac{C_R}{I_{CRD}} \cdot V_{TCRD}$$

In the case of using the external resistance: R_1/R_2, you should calculate R_{D1}/R_{D2} replaced the following.

$$R_{D1} \Rightarrow \frac{R_{D1} \cdot R_1}{R_{D1} + R_1} \quad , \quad R_{D2} \Rightarrow \frac{R_{D2} \cdot R_2}{R_{D2} + R_2}$$

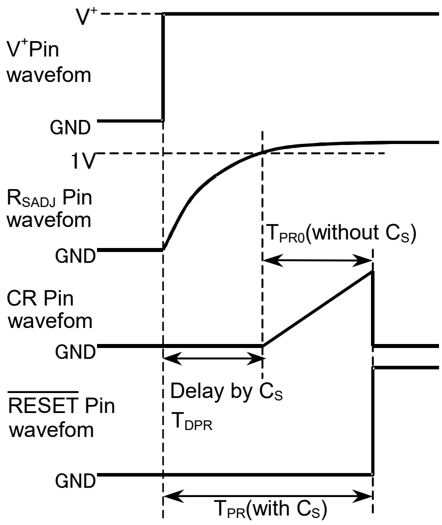


Fig 8. Each Pin Voltage Waveform at inserting C_S