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FAIRCHILD SEMICONDUCTOR®

November 2013

# FDMS039N08B

## N-Channel PowerTrench® MOSFET

**80 V, 100 A, 3.9 mΩ**

## Features

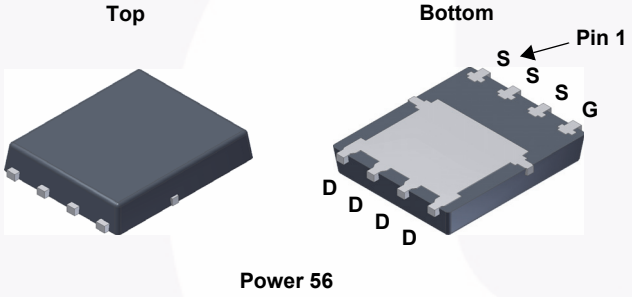
- $R_{DS(on)}$ = 3.2 mΩ (Typ.) @ $V_{GS}$ = 10 V, $I_D$ = 50 A
- Low FOM $R_{DS(on)}$ *$Q_G$
- Low Reverse Recovery Charge, $Q_{rr}$ = 80 nC
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

## Description

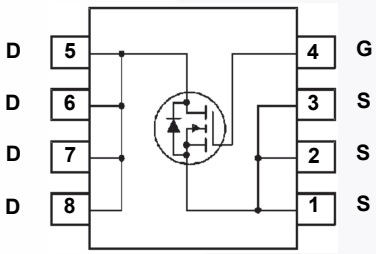
This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

## Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies




Power 56




## MOSFET Maximum Ratings $T_C$ = 25°C unless otherwise noted.

| Symbol | Parameter | | | FDMS039N08B | Unit |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | | | 80 | V |
| $V_{GSS}$ | Gate to Source Voltage | | | ±20 | V |
| $I_D$ | Drain Current | - Continuous ($T_C$ = 25°C) | | 100 | A |
| | | - Continuous ($T_A$ = 25°C) | (Note 1a) | 19.4 | |
| $I_{DM}$ | Drain Current | - Pulsed | (Note 2) | 400 | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy | | (Note 3) | 240 | mJ |
| $P_D$ | Power Dissipation | ($T_C$ = 25°C) | | 104 | W |
| | | ($T_A$ = 25°C) | (Note 1a) | 2.5 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | | -55 to +150 | °C |

## Thermal Characteristics

| Symbol | Parameter | | FDMS039N08B | Unit |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case, Max. | | 1.2 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient, Max. | (Note 1a) | 50 | |

## Package Marking and Ordering Information

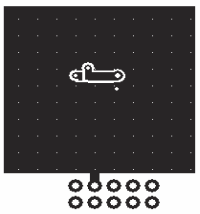
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMS039N08B | FDMS039N08B | Power 56 | 13 ” | 12 mm | 3000 units |

## Electrical Characteristics $T_C$ = 25°C unless otherwise noted.

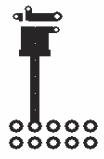
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 80 | - | - | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | - | 0.04 | - | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 64 V, $V_{GS}$ = 0 V | - | - | 1 | μA |
| $I_{GSS}$ | Gate to Body Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | - | - | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2.5 | - | 4.5 | V |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 50 A | - | 3.2 | 3.9 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 50 A | - | 100 | - | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 5715 | 7600 | pF |
| $C_{oss}$ | Output Capacitance | | - | 881 | 1170 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 15 | - | pF |
| $C_{oss}$(er) | Engry Releted Output Capacitance | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V | - | 1646 | - | pF |
| $Q_{g(tot)}$ | Total Gate Charge at 10V | $V_{DS}$ = 40 V, $I_D$ = 50 A, $V_{GS}$ = 0 V to 10 V | - | 77 | 100 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | - | 34 | - | nC |
| $Q_{gs2}$ | Gate Charge Threshold to Plateau | | - | 13 | - | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | (Note 4) | - | 16 | - | nC |
| ESR | Equivalent Series Resistance | f = 1 MHz | - | 1.2 | - | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 40 V, $I_D$ = 50 A, $V_{GS}$ = 10 V, $R_G$ = 4.7 Ω | - | 42 | 94 | ns |
| $t_r$ | Turn-On Rise Time | | - | 25 | 60 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 48 | 106 | ns |
| $t_f$ | Turn-Off Fall Time | (Note 4) | - | 17 | 44 | ns |
| **Drain-Source Diode Characteristics** | | | | | | |
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | - | - | 100 | A |
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | 400 | A |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 50 A | - | - | 1.3 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_{SD}$ = 50 A, $V_{DD}$ = 40 V, $dI_F/dt$ = 100 A/μs | - | 68 | - | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 80 | - | nC |

**Notes:**

1.$R_{\theta JA}$ is determined with the device mounted on a 1in$^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in$^2$ pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Repetitive rating: pulse-width limited by maximum junction temperature.

3. L = 0.3 mH, $I_{AS}$ = 40 A, starting $T_J$ = 25°C.

4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

**Figure 1. On-Region Characteristics**

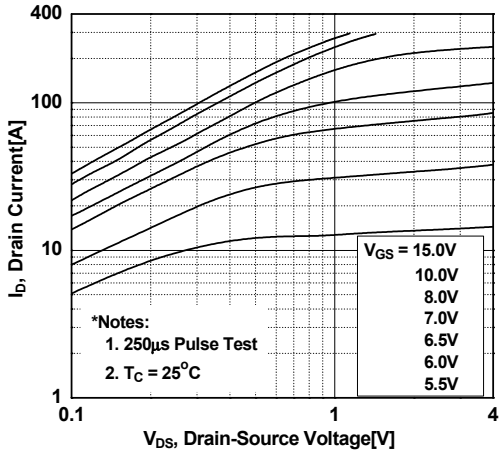



**Figure 2. Transfer Characteristics**

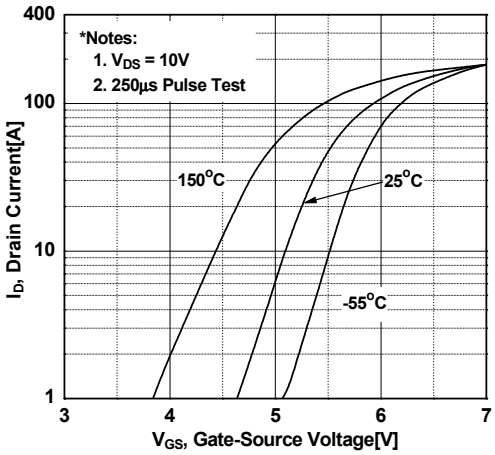



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

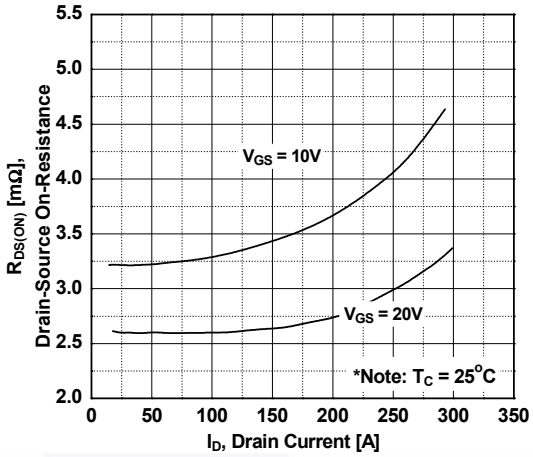



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

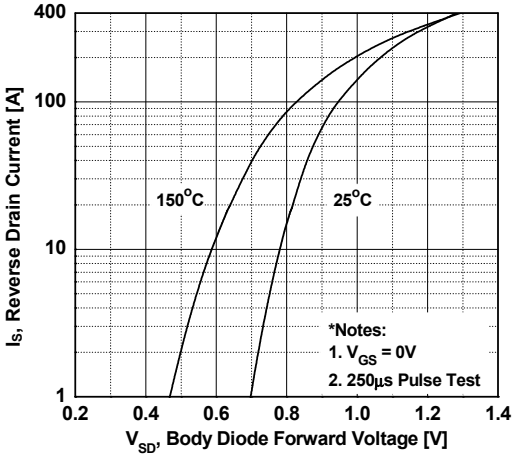



**Figure 5. Capacitance Characteristics**

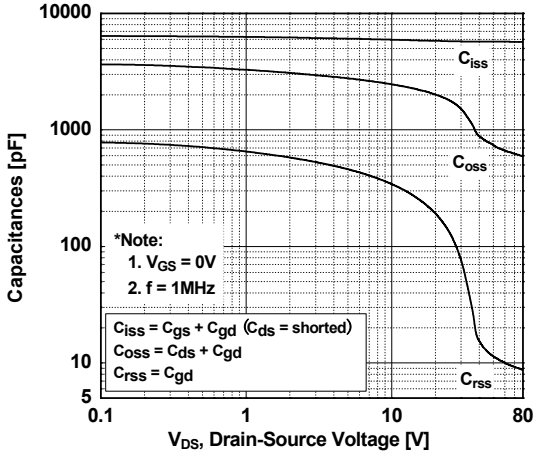
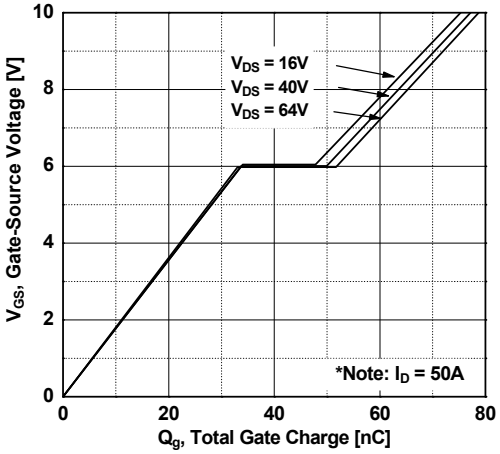



**Figure 6. Gate Charge Characteristics**



## Typical Performance Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation vs. Temperature**

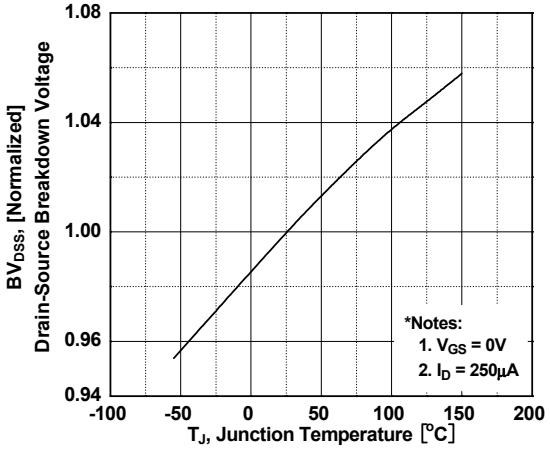



**Figure 8. On-Resistance Variation vs. Temperature**

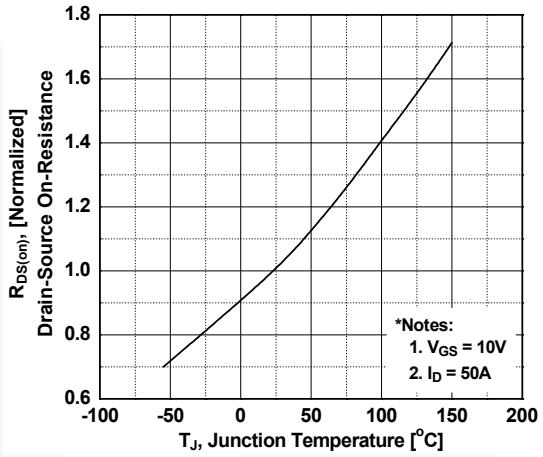



**Figure 9. Maximum Safe Operating Area**

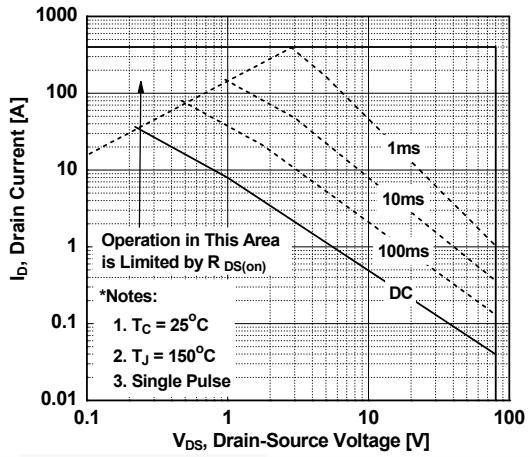



**Figure 10. Maximum Drain Current vs. Case Temperature**

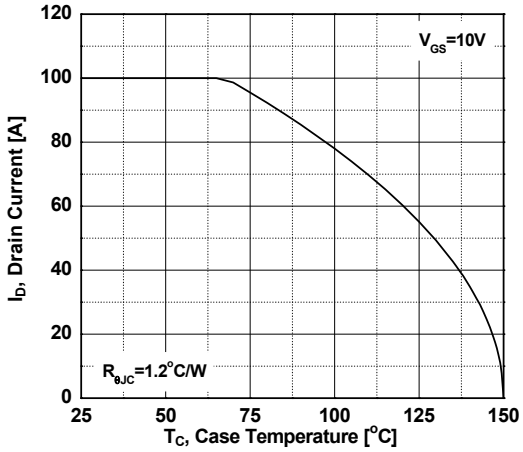



**Figure 11. Unclamped Inductive Switching Capability**

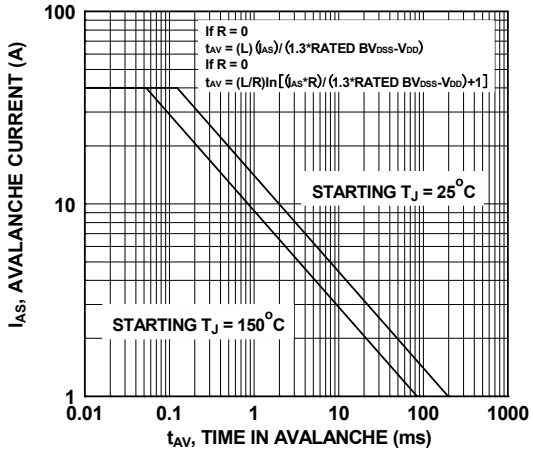
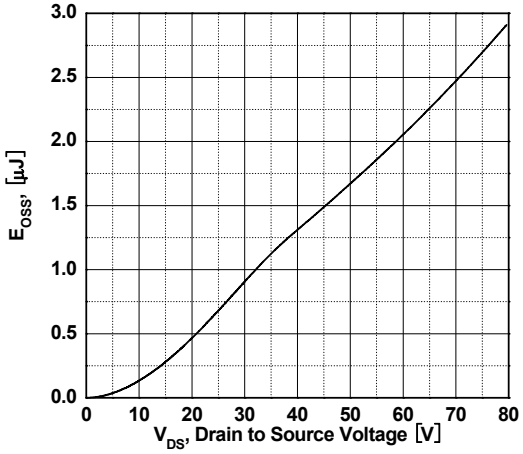



**Figure 12. Eoss vs. Drain to Source Voltage**



## Typical Performance Characteristics (Continued)

**Figure 13. Transient Thermal Response Curve**

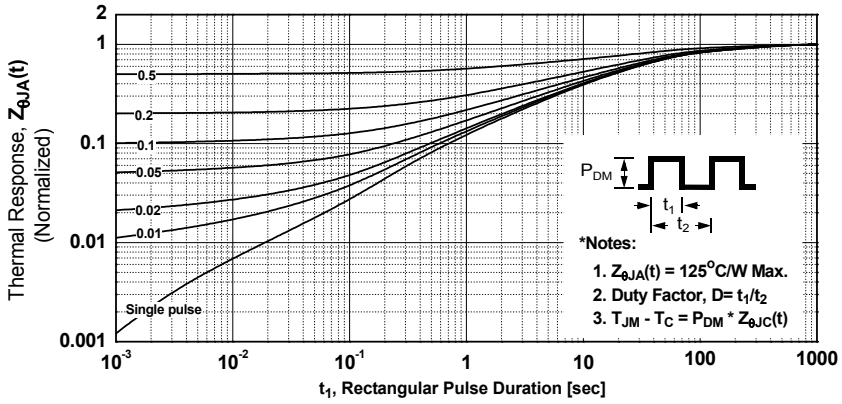


**Figure 14. Gate Charge Test Circuit & Waveform**

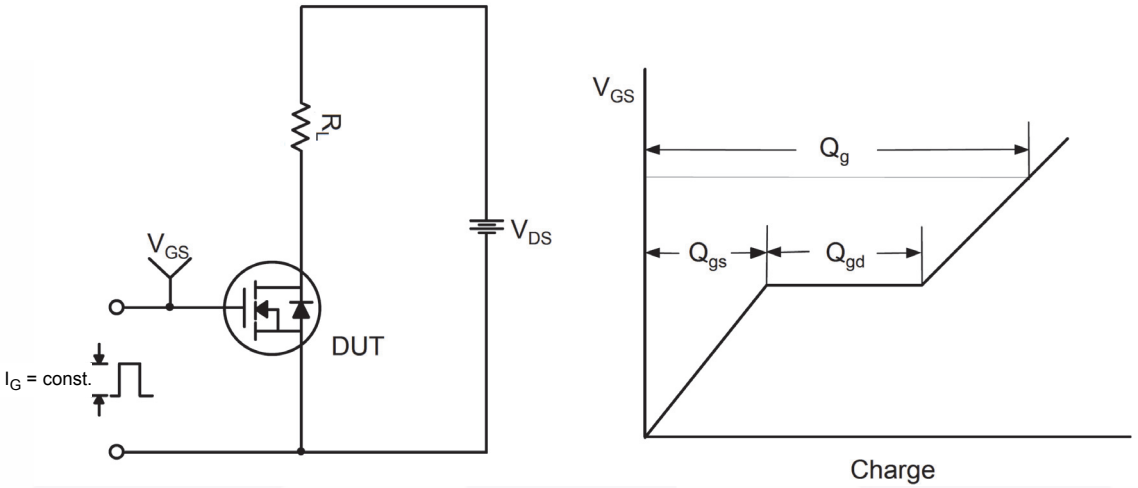



**Figure 15. Resistive Switching Test Circuit & Waveforms**

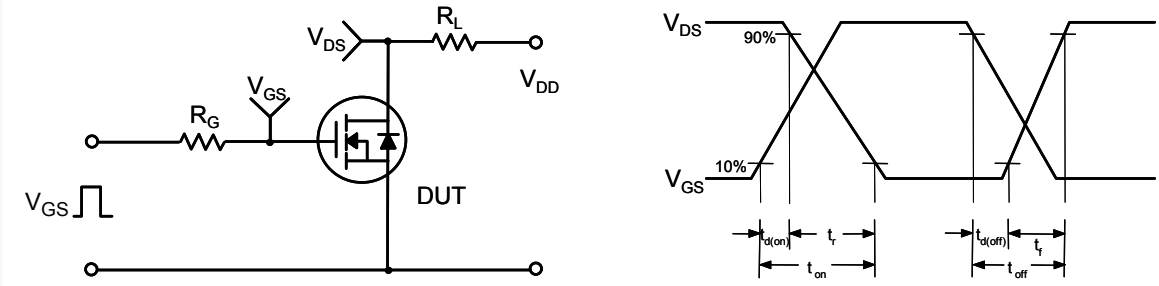



**Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms**

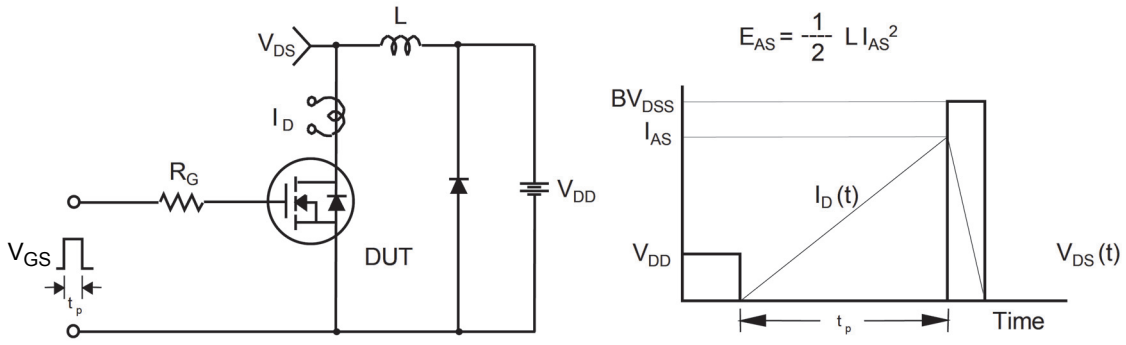
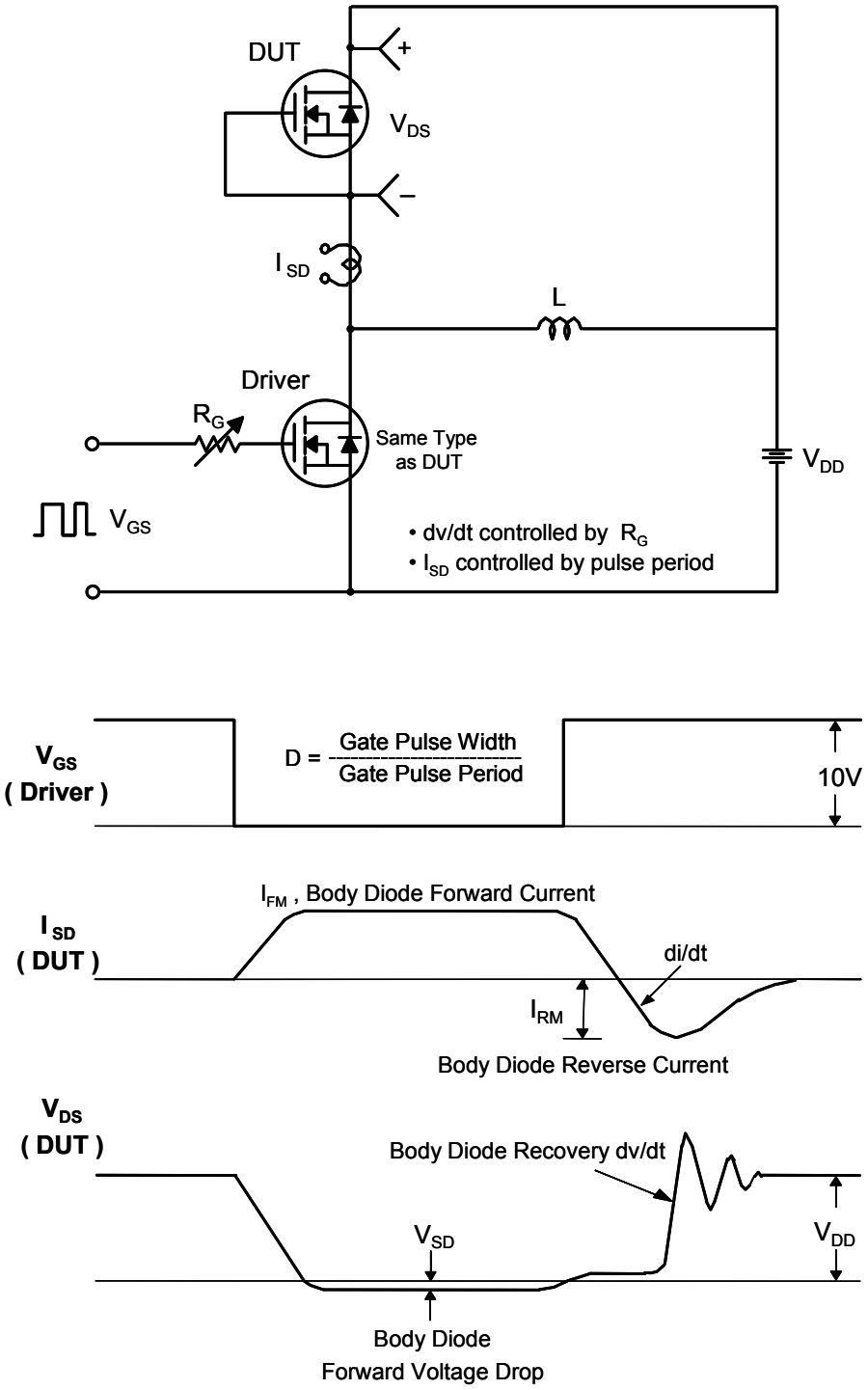
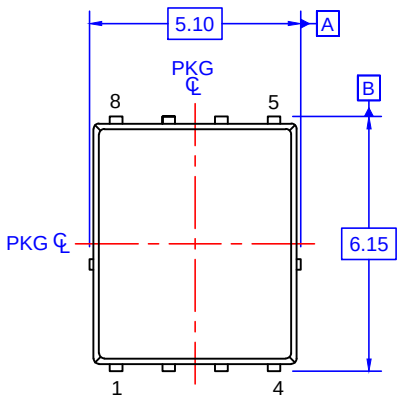


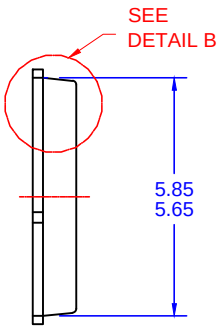
**Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms**

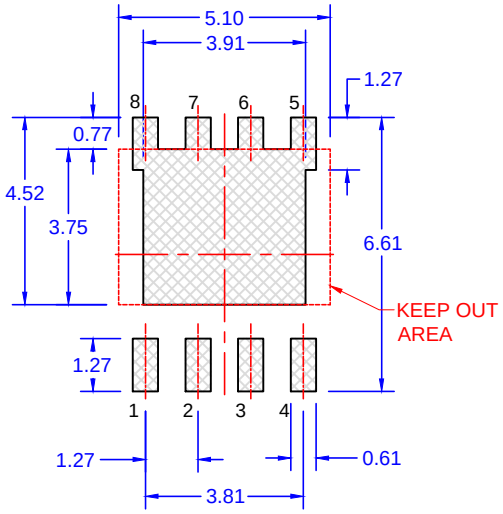


PQFN8 5X6, 1.27P
CASE 483AE
ISSUE A

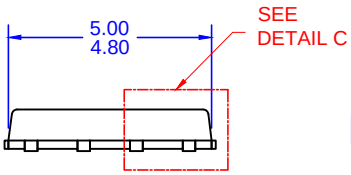



TOP VIEW

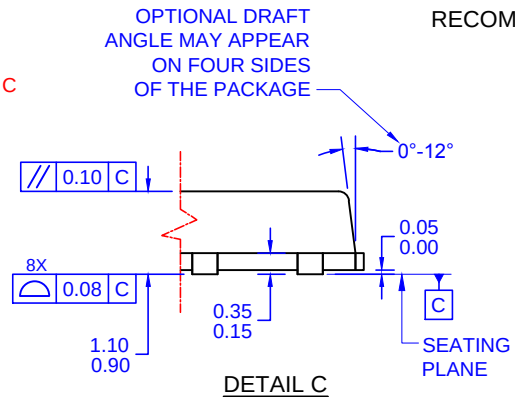


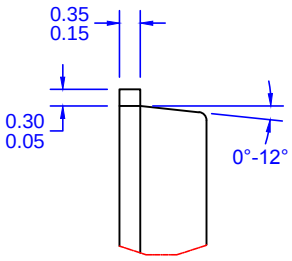

LAND PATTERN
RECOMMENDATION



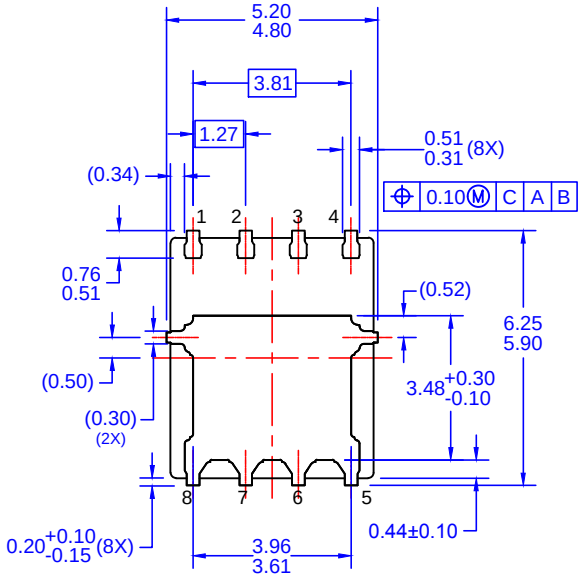

SIDE VIEW




DETAIL C
SCALE: 2:1




DETAIL B
SCALE: 2:1




BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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