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### FDN335N

### N-Channel 2.5V Specified PowerTrench™ MOSFET

### **General Description**

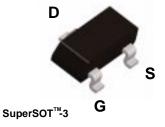
This N-Channel 2.5V specified MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

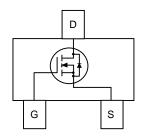
### **Applications**

- DC/DC converter
- Load switch

### **Features**

- 1.7 A, 20 V.  $R_{DS(ON)}=0.07~\Omega~@V_{GS}=4.5~V$   $R_{DS(ON)}=0.100~\Omega~@V_{GS}=2.5~V.$
- Low gate charge (3.5nC typical).
- High performance trench technology for extremely low  $R_{\scriptscriptstyle DS(ON)}.$
- High power and current handling capability.





Absolute Maximum Ratings TA = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		20	V
V <sub>GSS</sub>	Gate-Source Voltage		<u>±</u> 8	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	1.7	А
	- Pulsed		8	
$P_D$	Power Dissipation for Single Operation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
$T_J$ , $T_{stg}$	Operating and Storage Junction Temperature Range		-55 to +150	°C

### **Thermal Characteristics**

$R_{\theta^{JA}}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
R <sub>OJC</sub>	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Package Outlines and Ordering Information

T dollago o dillinoo dila ordoring illiorination					
Device Marking	Device	Reel Size	Tape Width	Quantity	
335	FDN335N	7"	8mm	3000 units	

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	20			V
<u>Δ</u> BVbss ΔTJ	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ ,Referenced to 25°C		14		mV/∘C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V			1	μА
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 8 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	$V_{GS} = -8 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Chara	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250  \mu A$	0.4	0.9	1.5	V
ΔVGS(th) ΔT <sub>J</sub>	Gate Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ ,Referenced to 25°C		-3		mV/∘C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 1.7 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 1.7 \text{ A}, T_J = 125 ^{\circ}\text{C}$ $V_{GS} = 2.5 \text{ V}, I_D = 1.5 \text{ A}$		0.055 0.079 0.078	0.070 0.120 0.100	Ω
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 5 V	8			Α
<b>g</b> FS	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 1.5 \text{ A}$		7		S
Dynamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V},$		310		pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		80		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 1		40		pF
	g Characteristics (Note 2)	·	ļ.		ļ.	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 1 A,	Ĭ	5	15	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$		8.5	17	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			11	20	ns
t <sub>f</sub>	Turn-Off Fall Time			3	10	ns
$Q_q$	Total Gate Charge	$V_{DS} = 10 \text{ V}, I_{D} = 1.7 \text{ A},$		3.5	5	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 4.5 \text{ V},$		0.55		nC
Q <sub>gd</sub>	Gate-Drain Charge	1		0.95		nC
Drain-Sa	urce Diode Characteristics	and Maximum Patings		!	!	
<u> סומווו-30</u>  s	Maximum Continuous Drain-Source				0.42	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 0.42 \text{ A}$ (Note 2)		0.7	1.2	V

#### Notes:

1:  $R_{\text{QJA}}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\text{QJC}}$  is guaranteed by design while  $R_{\text{QCA}}$  is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in² Pad of 2 oz. Cu.



b) 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width  $\leq 300~\mu\text{s},~\text{Duty Cycle} \leq 2.0\%$ 

### **Typical Characteristics**

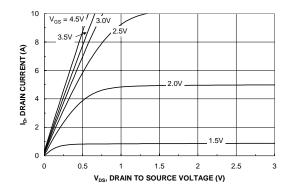


Figure 1. On-Region Characteristics.

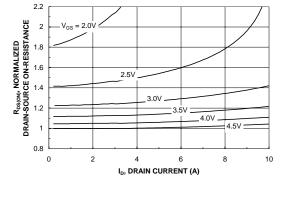


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

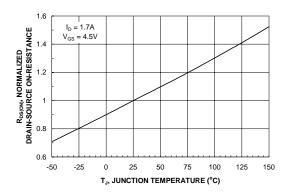


Figure 3. On-Resistance Variation with Temperature.

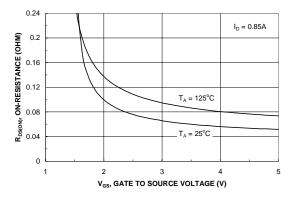


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

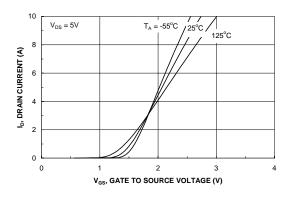


Figure 5. Transfer Characteristics.

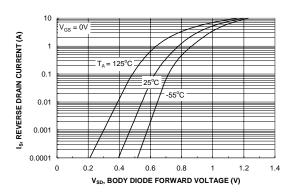
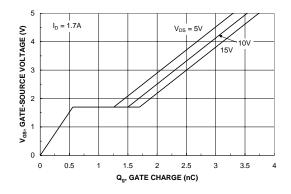


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics (continued)



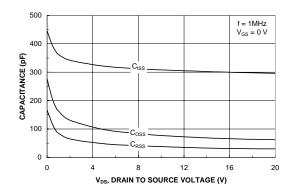
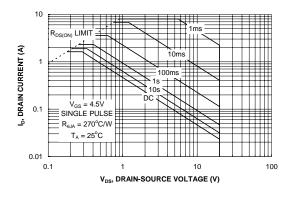


Figure 7. Gate Charge Characteristics.





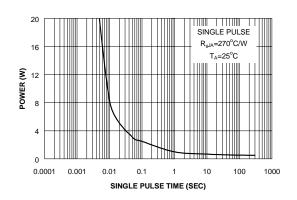


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

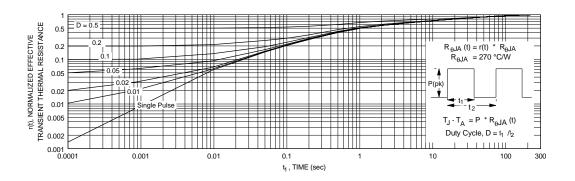


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient themal response will change depending on the circuit board design.

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