



PSMN7R5-30MLD

N-channel 30 V, 7.5 mΩ logic level MOSFET in LFPAK33 using NextPowerS3 Technology

11 August 2015

Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK33 package. NextPowerS3 portfolio utilising Nexperia's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

2. Features and benefits

- Ultra low Q_G , Q_{GD} and Q_{OSS} for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor > 1
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with $< 1 \mu\text{A}$ leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Mini Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Exposed leads for optimal visual solder inspection

3. Applications

- On-board DC-to-DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control

4. Quick reference data

Table 1. Quick reference data

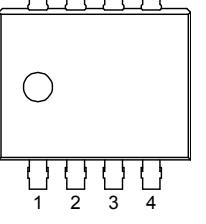
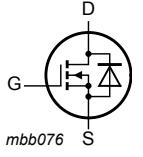
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$; Fig. 2	-	-	57	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 1	-	-	45	W

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 10$ A; $T_j = 25$ °C; Fig. 10		-	8.2	10.3	mΩ
		$V_{GS} = 10$ V; $I_D = 15$ A; $T_j = 25$ °C; Fig. 10		-	6.3	7.6	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 4.5$ V; $I_D = 15$ A; $V_{DS} = 15$ V; Fig. 12 ; Fig. 13		-	1.7	2.5	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5$ V; $I_D = 15$ A; $V_{DS} = 15$ V; Fig. 12 ; Fig. 13		-	5.8	8.8	nC
Source-drain diode							
S	softness factor	$I_S = 15$ A; $V_{GS} = 0$ V; $dI_S/dt = -100$ A/μs; $V_{DS} = 15$ V; Fig. 16		-	1.2	-	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	 LFPAK33 (SOT1210)	

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN7R5-30MLD	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 8 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN7R5-30MLD	7D530L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25^{\circ}\text{C} \leq T_j \leq 175^{\circ}\text{C}$		-	30	V
V_{DGR}	drain-gate voltage	$25^{\circ}\text{C} \leq T_j \leq 175^{\circ}\text{C}; R_{GS} = 20\text{ k}\Omega$		-	30	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25^{\circ}\text{C}$; Fig. 1		-	45	W
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25^{\circ}\text{C}$; Fig. 2		-	57	A
		$V_{GS} = 10\text{ V}; T_{mb} = 100^{\circ}\text{C}$; Fig. 2		-	40	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^{\circ}\text{C}$; Fig. 3		-	230	A
T_{stg}	storage temperature			-55	175	$^{\circ}\text{C}$
T_j	junction temperature			-55	175	$^{\circ}\text{C}$
$T_{\text{sld(M)}}$	peak soldering temperature			-	260	$^{\circ}\text{C}$
Source-drain diode						
I_S	source current	$T_{mb} = 25^{\circ}\text{C}$		-	38	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^{\circ}\text{C}$		-	230	A
Avalanche ruggedness						
$E_{DS(\text{AL})S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25^{\circ}\text{C}; I_D = 15\text{ A}; V_{\text{sup}} \leq 30\text{ V}; R_{GS} = 50\text{ }\Omega$; unclamped; $t_p = 97\text{ }\mu\text{s}$	[1]	-	28.3	mJ

[1] Protected by 100% test

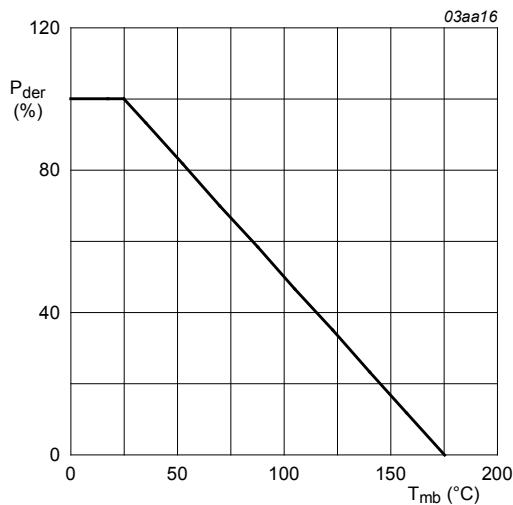


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}C)} \times 100 \%$$

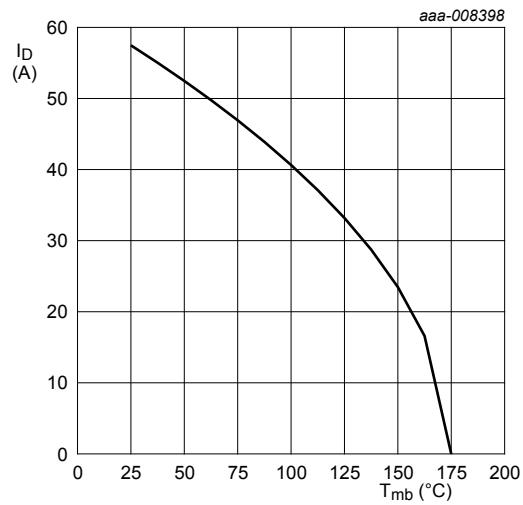


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

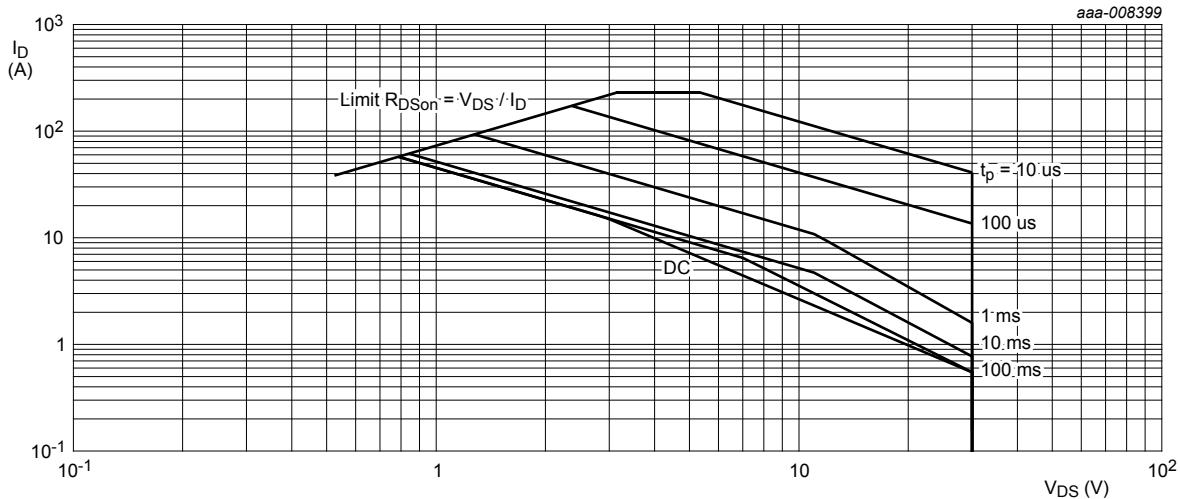


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25^{\circ}C; I_{DM} \text{ is a single pulse}$$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	3.1	3.32	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5		-	57	-	K/W
		Fig. 6		-	178	-	K/W

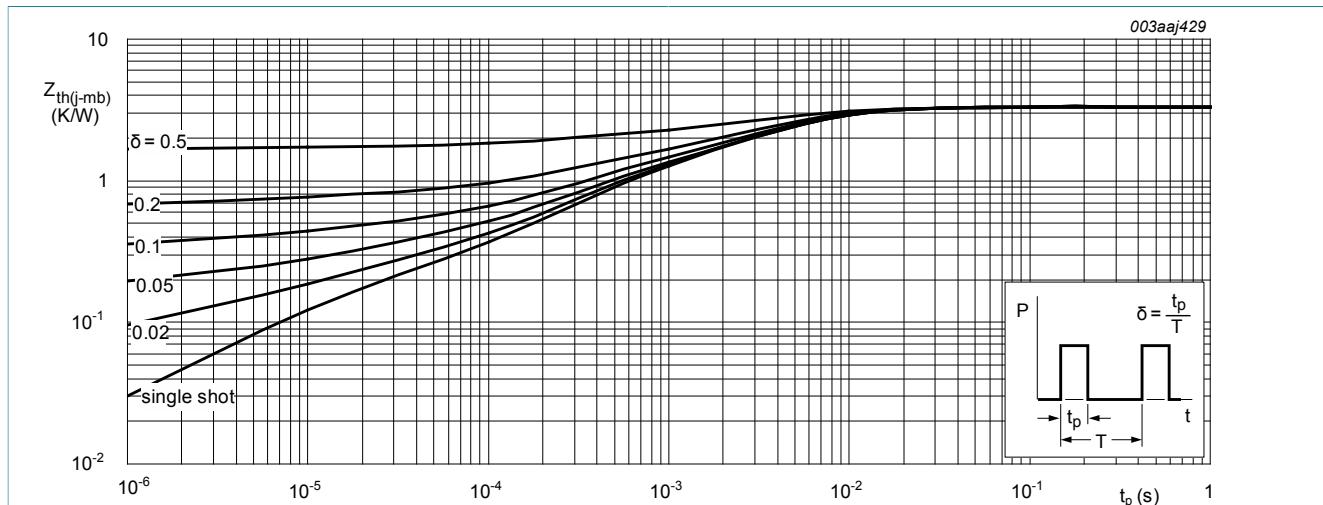


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

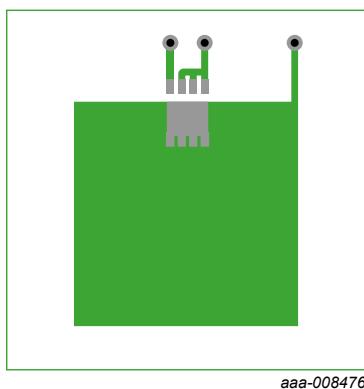


Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

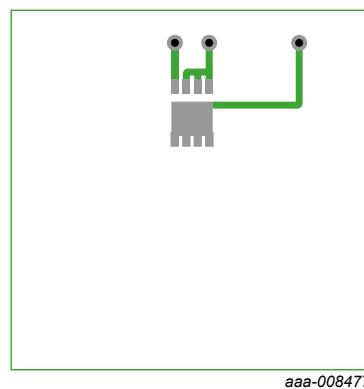


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$		27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C$		1.2	1.7	2.2	V

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25^\circ C \leq T_j \leq 150^\circ C$		-	-3.8	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	-	1	μA
		$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 125^\circ C$		-	0.26	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 10 A; T_j = 25^\circ C$ Fig. 10		-	8.2	10.3	mΩ
		$V_{GS} = 4.5 V; I_D = 10 A; T_j = 150^\circ C$ Fig. 11 ; Fig. 10		-	-	17	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 25^\circ C$ Fig. 10		-	6.3	7.6	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 150^\circ C$ Fig. 11 ; Fig. 10		-	-	12.5	mΩ
R_G	gate resistance	$f = 1 MHz$		-	0.25	0.49	Ω

Dynamic characteristics

$Q_{G(tot)}$	total gate charge	$I_D = 15 A; V_{DS} = 15 V; V_{GS} = 10 V$ Fig. 12 ; Fig. 13		-	11.3	17	nC
		$I_D = 15 A; V_{DS} = 15 V; V_{GS} = 4.5 V$ Fig. 12 ; Fig. 13		-	5.8	8.8	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$		-	10.2	-	nC
Q_{GS}	gate-source charge	$I_D = 15 A; V_{DS} = 15 V; V_{GS} = 4.5 V$ Fig. 12 ; Fig. 13		-	1.97	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	1.14	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	0.83	-	nC
Q_{GD}	gate-drain charge			-	1.7	2.5	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 15 A; V_{DS} = 15 V$; Fig. 12 ; Fig. 13		-	2.9	-	V
C_{iss}	input capacitance	$V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz$ $T_j = 25^\circ C$; Fig. 14		-	655	982	pF
C_{oss}	output capacitance			-	578	867	pF
C_{rss}	reverse transfer capacitance			-	50	75	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V; R_L = 1 \Omega; V_{GS} = 4.5 V$ $R_{G(ext)} = 5 \Omega$		-	7.1	-	ns
t_r	rise time			-	10.4	-	ns
$t_{d(off)}$	turn-off delay time			-	8.5	-	ns
t_f	fall time			-	5.5	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{oss}	output charge	$V_{GS} = 0 \text{ V}$; $V_{DS} = 15 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25^\circ \text{C}$		-	11	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 10 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25^\circ \text{C}$; Fig. 15		-	0.82	1.2	V
t_{rr}	reverse recovery time	$I_S = 15 \text{ A}$; $dI_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 15 \text{ V}$; Fig. 16		-	23	46	ns
Q_r	recovered charge	[1]	-	11	22	nC	
t_a	reverse recovery rise time		-	10.2	-	ns	
t_b	reverse recovery fall time		-	12.6	-	ns	
S	softness factor		-	1.2	-		

[1] includes capacitive recovery

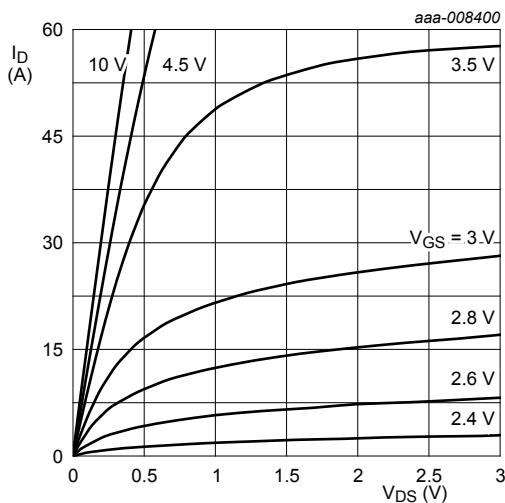


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

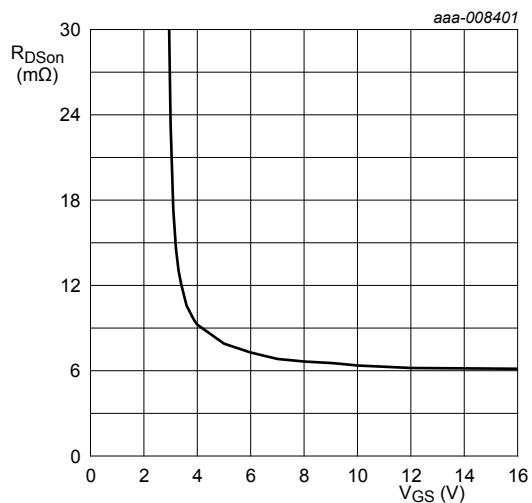
 $T_j = 25^\circ \text{C}$ 

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

 $T_j = 25^\circ \text{C}; I_D = 15 \text{ A}$

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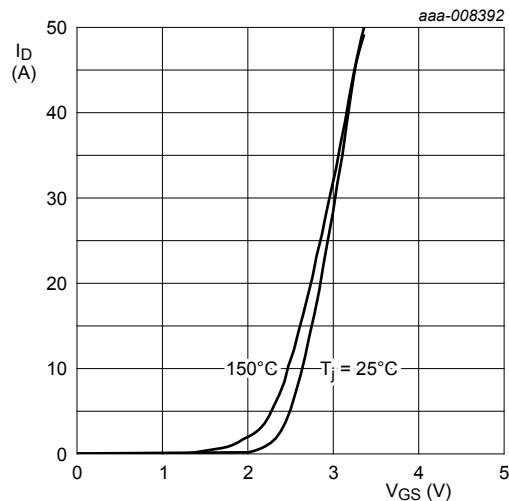


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

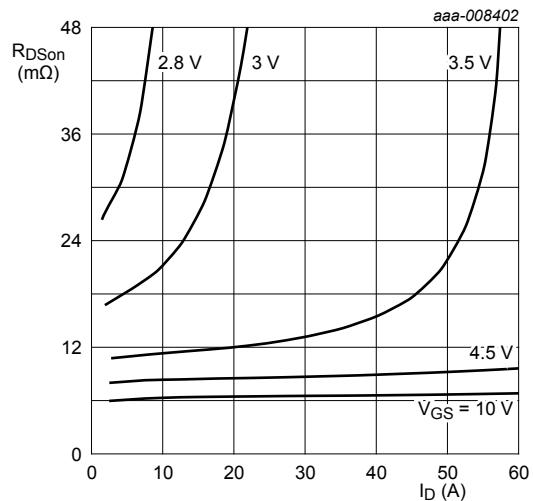


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ C$

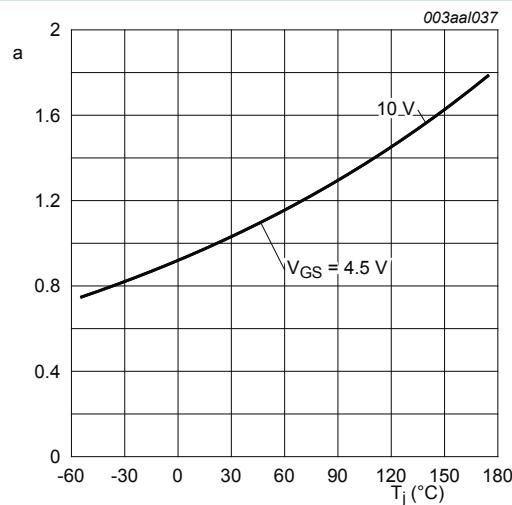


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

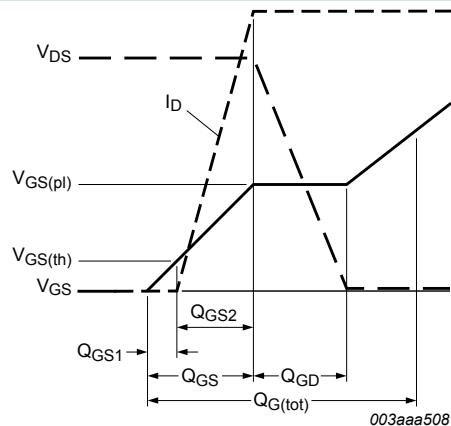


Fig. 12. Gate charge waveform definitions

N-channel 30 V, 7.5 mΩ logic level MOSFET in LFPAK33 using NextPowerS3 Technology

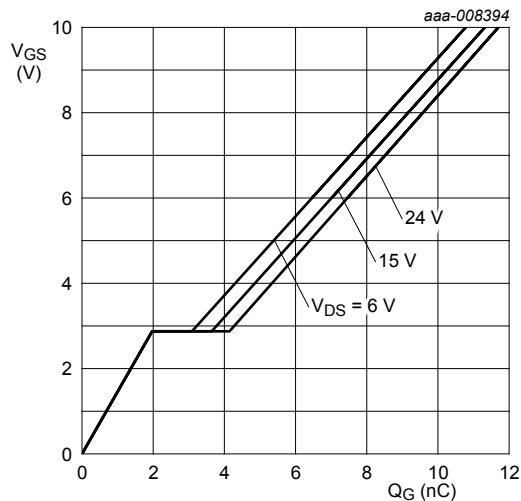


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}$; $I_D = 15\text{A}$

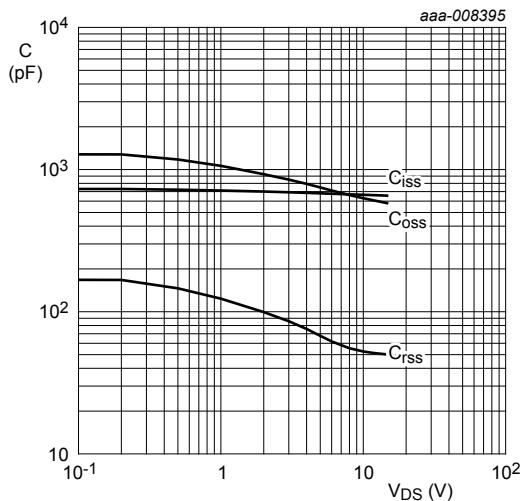


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{V}$; $f = 1\text{MHz}$

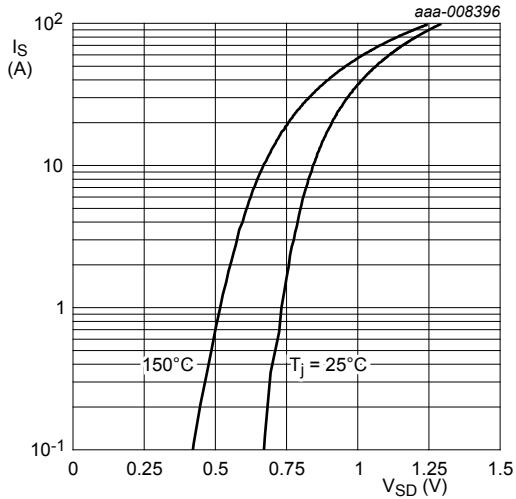


Fig. 15. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{V}$

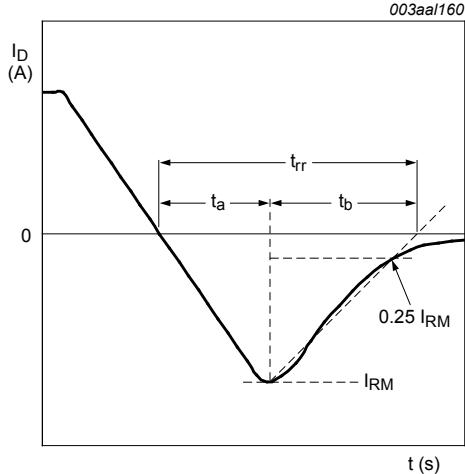


Fig. 16. Reverse recovery timing definition

11. Package outline

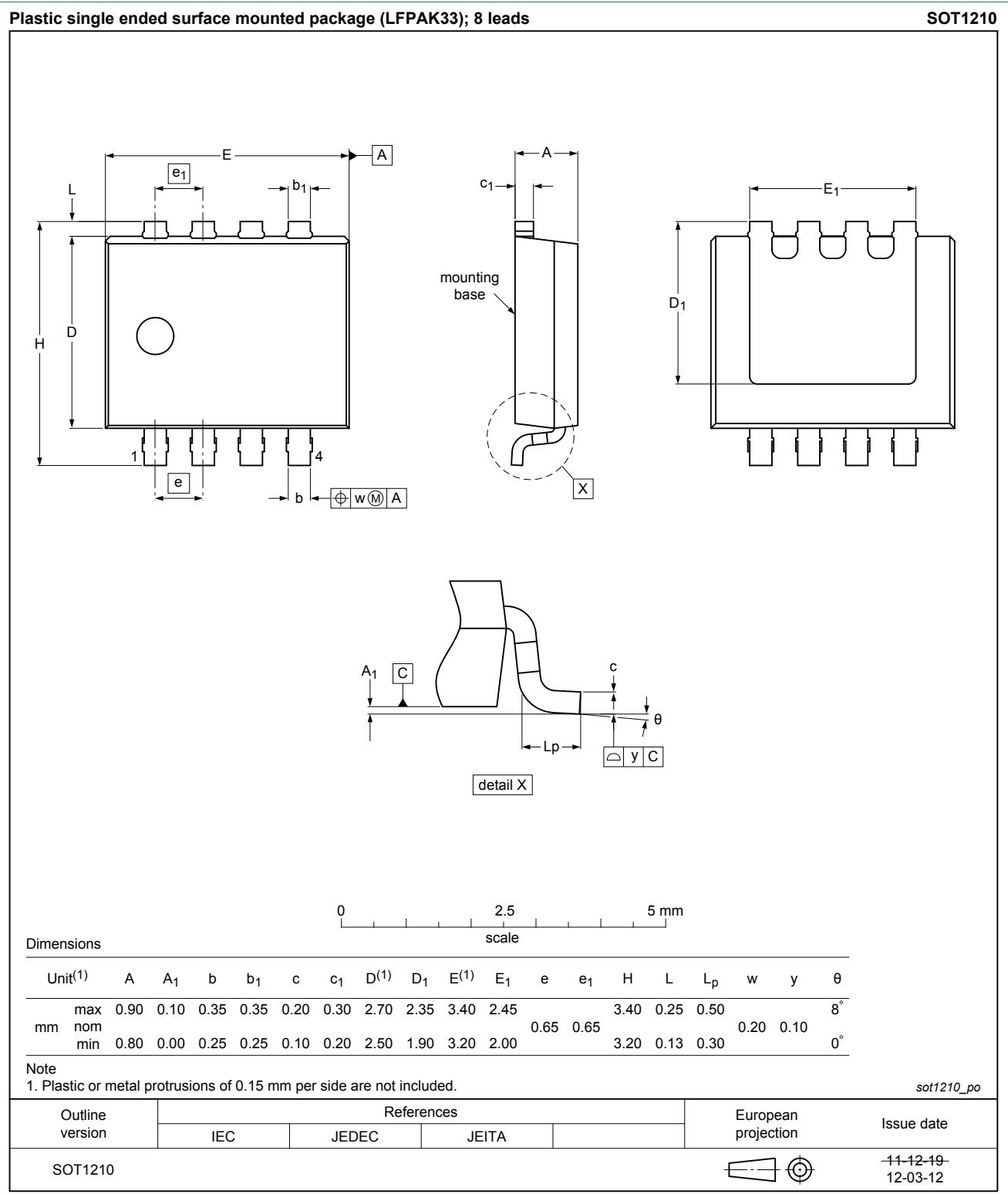


Fig. 17. Package outline LFPAK33 (SOT1210)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
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