TXS0108E-Q1 8-Bit Bi-directional, Level-Shifting, Voltage Translator for Open-Drain and Push-Pull Applications

1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Device Temperature Grade 1: –40°C to 125°C
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- No Direction-Control Signal Needed
- Maximum Data Rates
  - 110 Mbps (Push Pull)
  - 1.2 Mbps (Open Drain)
- 1.4 V to 3.6 V on A Port and 1.65 V to 5.5 V on B Port ($V_{CCA} \leq V_{CCB}$)
- No Power-Supply Sequencing Required – Either V_{CCA} or V_{CCB} Can Be Ramped First
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22 (A Port)
  - 2000 V Human Body Model (A114-B)
  - 1000 V Charged-Device Model (C101)
- IEC 61000-4-2 ESD (B Port)
  - ±8 kV Contact Discharge
  - ±6 kV Air-Gap Discharge

2 Applications

- Automotive

3 Description

This 8-bit non-inverting translator uses two separate configurable power-supply rails. The A port tracks the V_{CCA} pin supply voltage. The V_{CCA} pin accepts any supply voltage between 1.4 V and 3.6 V. The B port tracks the V_{CCB} pin supply voltage. The V_{CCB} pin accepts any supply voltage between 1.65 V and 5.5 V. Two input supply pins allows for low Voltage bidirectional translation between any of the 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V voltage nodes.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance (Hi-Z) state.

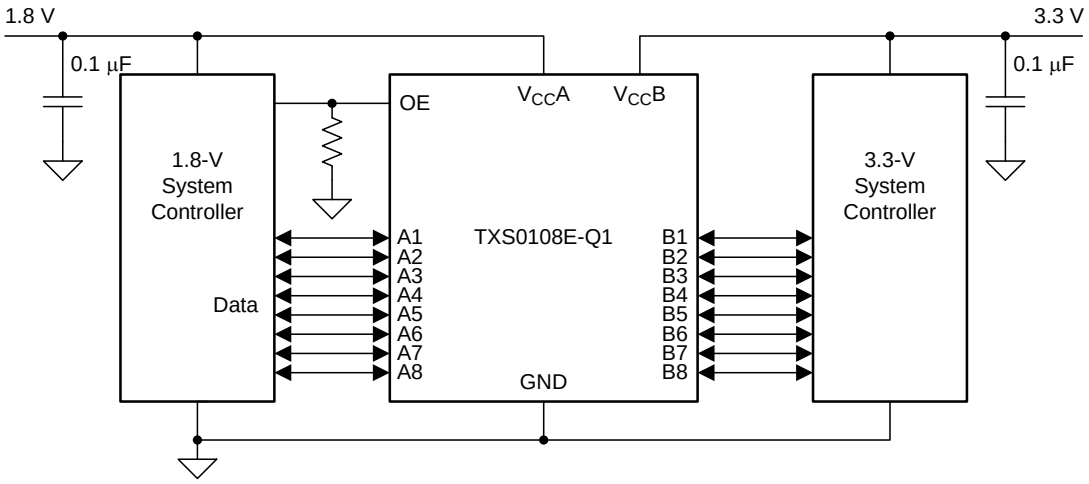
To ensure the Hi-Z state during power-up or power-down periods, tie OE to GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXS0108E-Q1	TSSOP (20)	6.50 mm × 6.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application



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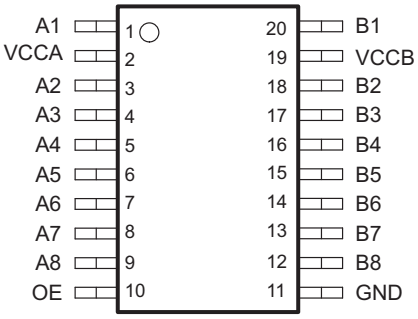
5 Pin Configuration and Functions

PW PACKAGE
20-PIN TSSOP
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1	1	I/O	Input/output 1. Referenced to V_{CCA}
A2	3	I/O	Input/output 2. Referenced to V_{CCA}
A3	4	I/O	Input/output 3. Referenced to V_{CCA}
A4	5	I/O	Input/output 4. Referenced to V_{CCA}
A5	6	I/O	Input/output 5. Referenced to V_{CCA}
A6	7	I/O	Input/output 6. Referenced to V_{CCA}
A7	8	I/O	Input/output 7. Referenced to V_{CCA}
A8	9	I/O	Input/output 8. Referenced to V_{CCA}
B1	20	I/O	Input/output 1. Referenced to V_{CCB}
B2	18	I/O	Input/output 2. Referenced to V_{CCB}
B3	17	I/O	Input/output 3. Referenced to V_{CCB}
B4	16	I/O	Input/output 4. Referenced to V_{CCB}
B5	15	I/O	Input/output 5. Referenced to V_{CCB}
B6	14	I/O	Input/output 6. Referenced to V_{CCB}
B7	13	I/O	Input/output 7. Referenced to V_{CCB}
B8	12	I/O	Input/output 8. Referenced to V_{CCB}
GND	11	–	Ground
OE	10	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
VCCA	2	I	A-port supply voltage. 1.5 V ≤ V_{CCA} ≤ 3.6 V, V_{CCA} ≤ V_{CCB}.
VCCB	19	I	B-port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{CCA}		–0.5	4.6	V
Supply voltage, V_{CCB}		–0.5	5.5	V
Input voltage, V_I(2)	A port	–0.5	4.6	V
	B port	–0.5	6.5	
Voltage applied to any output in the high-impedance or power-off state, V_O(2)	A port	–0.5	4.6	V
	B port	–0.5	6.5	
Voltage applied to any output in the high or low state, V_O(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
	B port	–0.5	V_{CCB} + 0.5	V
Input clamp current, I_{IK}	V_I < 0		–50	mA
Output clamp current, I_{OK}	V_O < 0		–50	mA
Continuous output current, I_O		–50	50	mA
Continuous current through V_{CCA}, V_{CCB}, or GND		–100	100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative Voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

					MIN	MAX	UNIT
V_{CCA}	Supply voltage(3)				1.4	3.6	V
V_{CCB}	Supply voltage(3)				1.65	5.5	V
V_{IH}	High-level input voltage	A-Port I/Os	V_{CCA} (V) = 1.4 to 1.95	V_{CCB} (V) = 1.65 to 5.5	V_{CCI} – 0.2	V_{CCI}	V
			V_{CCA} (V) = 1.95 to 3.6	V_{CCB} (V) = 1.65 to 5.5	V_{CCI} – 0.4	V_{CCI}	
		B-Port I/Os	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5	V_{CCI} – 0.4	V_{CCI}	V
		OE	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5	V_{CCA} × 0.65	5.5	V
V_{IL}	Low-level input voltage	A-Port I/Os	V_{CCA} (V) = 1.4 to 1.95	V_{CCB} (V) = 1.65 to 5.5	0	0.15	V
			V_{CCA} (V) = 1.95 to 3.6	V_{CCB} (V) = 1.65 to 5.5	0	0.15	
		B-Port I/Os	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5	0	0.15	V
		OE	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5	0	V_{CCA} × 0.35	V
$\Delta t/\Delta v$	Input transition rise or fall rate	A-Port I/Os Push-pull	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5		10	ns/V
		B-Port I/Os Push-pull	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5		10	ns/V
		Control input	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5		10	ns/V
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

6.4 Thermal Information

THERMAL METRIC(1)		TXS0108E-Q1 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	52.4	
ψ_{JT}	Junction-to-top characterization parameter	2.3	
ψ_{JB}	Junction-to-board characterization parameter	51.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: T_A = –40°C to 125°C[1][2][3]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA} (V)	V_{CCB} (V)	T_A = 25°C			T_A = –40°C to 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OHA}	Port A output high voltage	I_{OH} = –20 μA, $V_{IB} \geq V_{CCB}$ – 0.4 V	1.4 to 3.6	1.65 to 5.5				V_{CCA} × 0.67		V
V_{OLA}	Port A output low voltage	I_{OL} = 180 μA, $V_{IB} \leq$ 0.15 V	1.4	1.65 to 5.5					0.4	V
		I_{OL} = 220 μA, $V_{IB} \leq$ 0.15 V	1.65	1.65 to 5.5					0.4	
		I_{OL} = 300 μA, $V_{IB} \leq$ 0.15 V	2.3	1.65 to 5.5					0.4	
		I_{OL} = 400 μA, $V_{IB} \leq$ 0.15 V	3	1.65 to 5.5					0.55	
V_{OHB}	Port B output high voltage	I_{OH} = –20 μA, $V_{IA} \geq V_{CCA}$ – 0.2 V	1.4 to 3.6	1.65 to 5.5				V_{CCB} × 0.67		V
V_{OLB}	Port B output low voltage	I_{OL} = 220 μA, $V_{IA} \leq$ 0.15 V	1.4 to 3.6	1.65					0.4	V
		I_{OL} = 300 μA, $V_{IA} \leq$ 0.15 V	1.4 to 3.6	2.3					0.4	
		I_{OL} = 400 μA, $V_{IA} \leq$ 0.15 V	1.4 to 3.6	3					0.55	
		I_{OL} = 620 μA, $V_{IA} \leq$ 0.15 V	1.4 to 3.6	4.5					0.55	
I_I	Input leakage current	OE: $V_I = V_{CCI}$ or GND	1.4	1.65 to 5.5	–1		1		2	μA
I_{OZ}	High-impedance state output current	A or B port	1.4	1.65 to 5.5	–1		1	–2	2	μA
I_{CCA}	V_{CCA} supply current	$V_I = V_O$ = Open, I_O = 0	1.4 to 3.6	2.3 to 5.5					2	μA
			3.6	0					2	
			0	5.5					–1	
I_{CCB}	V_{CCB} supply current	$V_I = V_O$ = Open, I_O = 0	1.4 to 3.6	2.3 to 5.5					6	μA
			3.6	0					–1	
			0	5.5					1.5	
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND, I_O = 0	1.4 to 3.6	2.3 to 5.5					8	μA
I_{CCZA}	High-impedance state V_{CCA} supply current	$V_I = V_O$ = Open, I_O = 0, OE = GND	1.4 to 3.6	1.65 to 5.5					2	μA
I_{CCZB}	High-impedance state V_{CCB} supply current	$V_I = V_O$ = Open, I_O = 0, OE = GND	1.4 to 3.6	1.65 to 5.5					6	μA
C_i	Input capacitance	OE	3.3	3.3		4.5			6.75	pF
C_{io}	Input-to-output internal capacitance	A port	3.3	3.3		6			7.6	pF
		B port	3.3	3.3		5.5			6.9	

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

6.6 Timing Requirements: V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

			$V_{CC\ B}$ = 1.8 V ± 0.15 V		$V_{CC\ B}$ = 2.5 V ± 0.2 V		$V_{CC\ B}$= 3.3 V ± 0.3 V		$V_{CC\ B}$= 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull			40		60		60		60	Mbps
	Open-drain			0.8		0.8		1		1	
t_w Pulse duration	Data inputs	Push-pull	25		16.7		16.7		16.7		ns
		Open-drain	1250		1250		1000		1000		

6.7 Timing Requirements: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

			$V_{CC\ B}$ = 1.8 V ± 0.15 V		$V_{CC\ B}$ = 2.5 V ± 0.2 V		$V_{CC\ B}$= 3.3 V ± 0.3 V		$V_{CC\ B}$= 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull			45		65		70		70	Mbps
	Open-drain			0.8		0.8		0.8		1	
t_w Pulse duration	Data inputs	Push-pull	22.2		15.3		15.3		15.3		ns
		Open-drain	1250		1250		1250		1000		

6.8 Timing Requirements: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

				V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
Data rate		Push-pull			80		95		100	Mbps
		Open-drain			0.8		0.8		1	
t_w	Pulse duration	Data inputs	Push-pull	12.5		10.5		10		ns
			Open-drain	1250		1250		1000		

6.9 Timing Requirements: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

				V_{CCB} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
Data rate		Push-pull			100		110	Mbps
		Open-drain			0.8		1.2	
t_w	Pulse duration	Data inputs	Push-pull	10		9.1		ns
			Open-drain	1250		833		

6.10 Switching Characteristics: V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving		11		9.2		8.6		8.6	ns
			Open-drain driving	2.5	14.4	2	12.8	2	12.2	1.9	12	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving		12		10		9.8		9.7	
			Open-drain driving	0.9	720	0.9	554	1	473	1.5	384	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving		12.7		11.1		11		12	ns
			Open-drain driving	3.4	13.2	2.6	9.6	2.3	8.5	2	7.5	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving		9.5		6.2		5.1		4.2	
			Open-drain driving		745		603		519		407	
t_{en}	Enable time	OE-to-A or B	Push-pull driving		480		480		480		480	ns
t_{dis}	Disable time	OE-to-A or B			400		400		400		400	ns
t_{rA}	Input rise time	A-port rise time	Push-pull driving	3	13.1	2.4	9.8	2	9	2	8.9	ns
			Open-drain driving	220	982	180	716	140	592	100	481	
t_{rB}	Input rise time	B-port rise time	Push-pull driving	2.6	11.4	1.6	7.4	1	6	0.7	5	ns
			Open-drain driving	220	1020	150	756	100	653	40	370	
t_{fA}	Input fall time	A-port fall time	Push-pull driving	2.3	9.9	1.7	7.7	1.6	6.8	1.7	6	ns
			Open-drain driving	2.4	10	1.8	8.2	1.7	9	1.5	9.15	
t_{fB}	Input fall time	B-port fall time	Push-pull driving	2	8.7	1.3	5.5	1	3.8	1	3.1	
			Open-drain driving	2	11.5	1.3	8.6	1	9.6	1	7.7	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1		1		1	ns

6.11 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

PARA-METER		TEST CONDITIONS		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving		8.2		6.4		5.7		5.6	ns
			Open-drain driving	2.1	11.4	1.7	9.9	1.6	9.3	1.5	8.9	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving		9		5.6		6.5		6.3	
			Open-drain driving	0.15	729	0.2	584	0.3	466	0.3	346	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving		9.8		8		7.4		7	ns
			Open-drain driving	3.19	12.1	2	8.5	1.9	7.3	1.8	6.2	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving		10.2		7		5.8		5	
			Open-drain driving		733		578		459		323	
t_{en}	Enable time	OE-to-A or B	Push-pull driving		100		100		100		100	ns
t_{dis}	Disable time	OE-to-A or B	Push-pull driving		410		410		410		410	ns
t_{rA}	Input rise time	A-port rise time	Push-pull driving	2.7	11.9	2	8.6	1.9	7.8	1.8	7.4	ns
			Open-drain driving	250	996	200	691	150	508	110	365	
t_{rB}	Input rise time	B-port rise time	Push-pull driving	2.5	10.5	1.7	7.4	1.1	5.3	60	4.7	ns
			Open-drain driving	250	1001	170	677	120	546	32	323	
t_{fA}	Input fall time	A-port fall time	Push-pull driving	2.1	8.8	1.6	7.1	1.4	6.8	1.4	6.06	ns
			Open-drain driving	2.2	9	1.7	7.2	1.4	6.8	1.2	6.1	
t_{fB}	Input fall time	B-port fall time	Push-pull driving	2	8.3	1.3	5.4	0.9	3.9	0.7	3	
			Open-drain driving	2	10.5	1	10.7	1	9.6	0.6	7.8	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1		1		1	ns

6.12 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARA-METER		TEST CONDITIONS		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving		5		4		3.7	ns
			Open-drain driving		6.2		6.3		5.8	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving		5.2		4.3		3.9	
			Open-drain driving		5		17.5		15.5	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving		5.4		4.7		4.2	ns
			Open-drain driving		7.3		6		4.9	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving		5.9		4.4		3.5	
			Open-drain driving		5		5		5	
t_{en}	Enable time	OE-to-A or B	Push-pull driving		100		100		100	ns
t_{dis}	Disable time	OE-to-A or B			400		400		400	ns
t_{rA}	Input rise time	A-port rise time	Push-pull driving	1.89	7.3	1.6	6.4	1.5	5.8	ns
			Open-drain driving	110.00	692	157	529	116	377	
t_{rB}	Input rise time	B-port rise time	Push-pull driving	1.70	6.5	1.3	5.1	0.9	4.32	ns
			Open-drain driving	107.00	693	140	483	77	304	
t_{fA}	Input fall time	A-port fall time	Push-pull driving	1.50	5.7	1.2	4.7	1.3	3.8	ns
			Open-drain driving	1.50	5.6	1.2	4.7	1.1	4.2	
t_{fB}	Input fall time	B-port fall time	Push-pull driving	1.40	5.4	0.9	4.1	0.7	3	
			Open-drain driving	0.40	14.2	0.5	19.4	0.4	3	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1		1	ns

6.13 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITION (DRIVING)		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving		3.8		3.28	ns
			Open-drain driving		5.3		4.8	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving		3.9		3.5	
			Open-drain driving		5		12.5	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving		4.2		3.8	ns
			Open-drain driving		5.5		4.5	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving		4.32		4.3	
			Open-drain driving		5		5	
t_{en}	Enable time	OE-to-A or B	Push-pull driving		100		100	ns
t_{dis}	Disable time	OE-to-A or B	Push-pull driving		400		400	ns
t_{rA}	Input rise time	A-port rise time	Push-pull driving	1.5	5.7	1.4	5	ns
			Open-drain driving	129	446	99.6	337	
t_{rB}	Input rise time	B-port rise time	Push-pull driving	1.35	5	1	4.24	ns
			Open-drain driving	129	427	77	290	
t_{fA}	Input fall time	A-port fall time	Push-pull driving	1.4	4.5	1.3	3.5	ns
			Open-drain driving	1.4	4.4	1.2	3.7	
t_{fB}	Input fall time	B-port fall time	Push-pull driving	1.3	4.2	1.1	3.1	
			Open-drain driving	1.3	4.2	1.1	3.1	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1	ns

7 Typical Characteristics

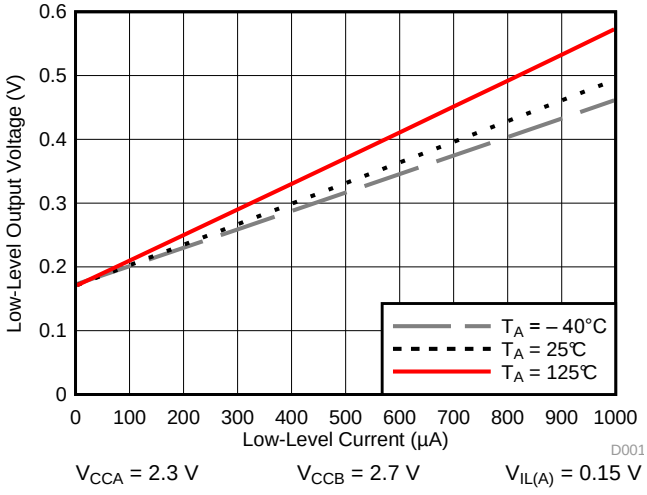


Figure 1. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

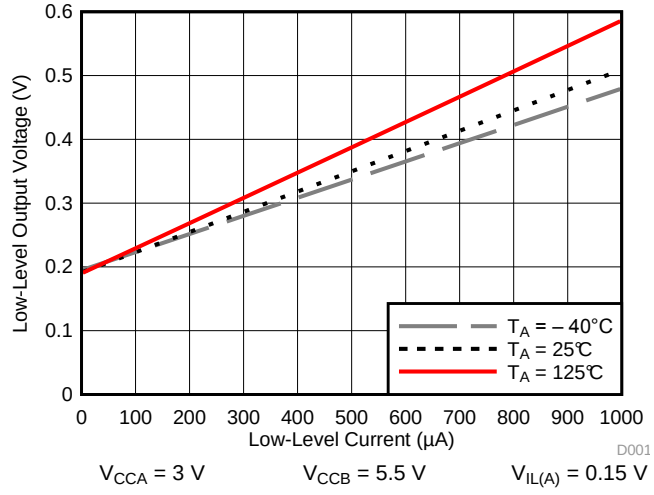


Figure 2. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

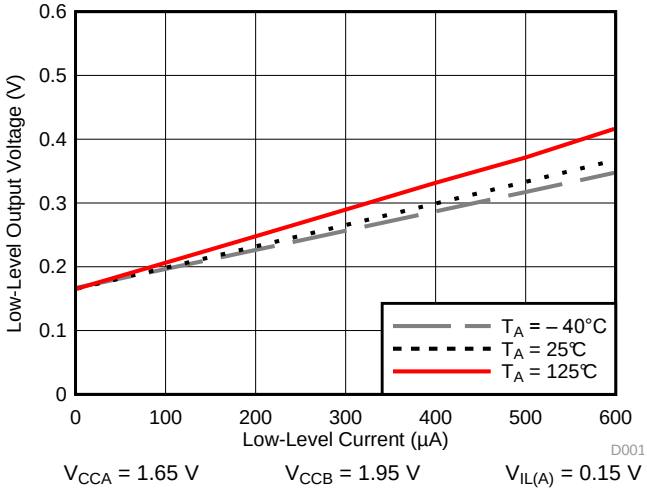


Figure 3. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

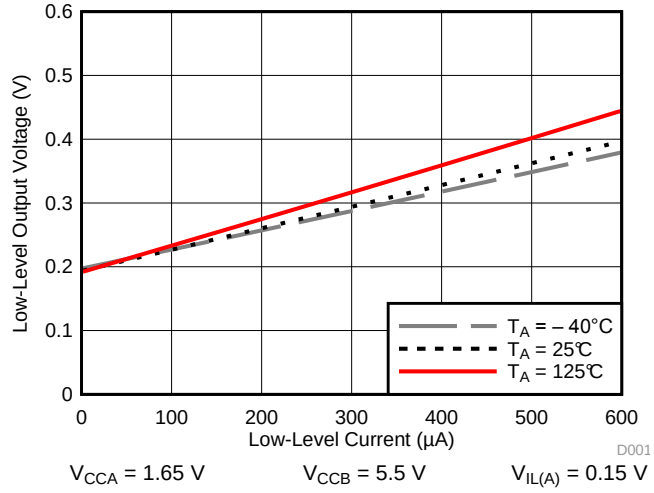
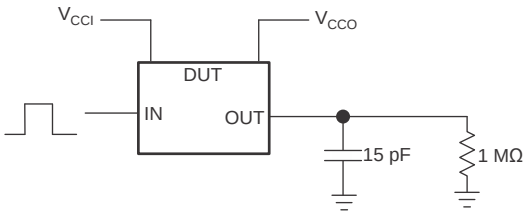


Figure 4. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

8 Parameter Measurement Information

8.1 Load Circuits

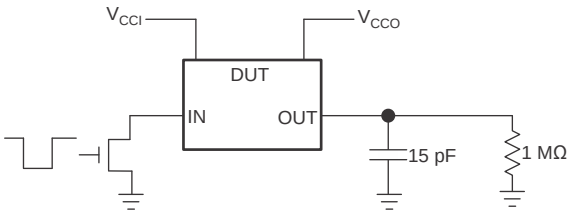
Figure 5 shows the push-pull driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time. Figure 6 shows the open-drain driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time.



(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

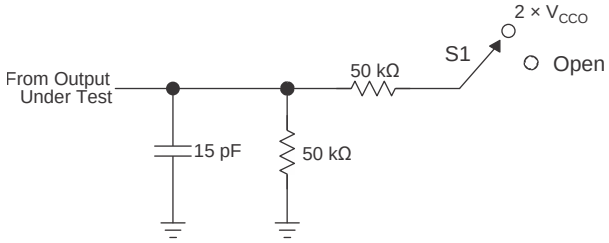
Figure 5. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time And Fall-Time Measurement Using a Push-Pull Driver



(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

Figure 6. Data Rate (10 pF), Pulse Duration (10 pF), Propagation Delay, Output Rise-Time And Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
t_{PZL}, t_{PLZ} (t_{dis})	2 × V_{CCO}
t_{PHZ}, t_{PZH} (t_{en})	Open

(1) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

(2) t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 7. Load Circuit for Enable-Time and Disable-Time Measurement

8.2 Voltage Waveforms

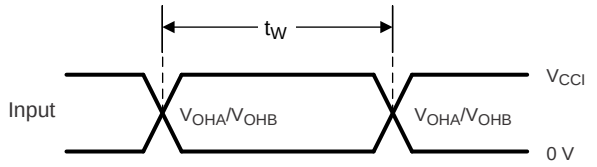


Figure 8. Pulse Duration (Push-Pull)

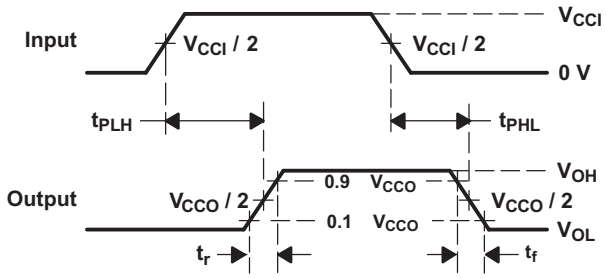
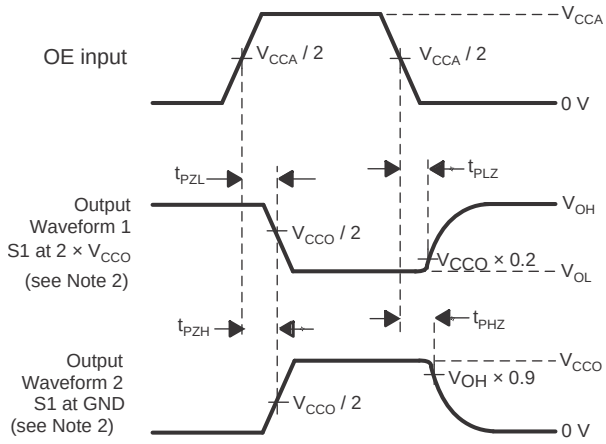


Figure 9. Propagation Delay Times



- C_L includes probe and jig capacitance.
- Waveform 1 in Figure 10 is for an output with internal such that the output is high, except when OE is high (see Figure 7). Waveform 2 in Figure 10 is for an output with conditions such that the output is low, except when OE is high.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- t_{PZL} and t_{PZH} are the same as t_{en}.
- t_{PLH} and t_{PHL} are the same as t_{pd}.
- V_{CCI} is the V_{CC} associated with the input port.
- V_{CCO} is the V_{CC} associated with the output port.

Figure 10. Enable and Disable Times

9 Detailed Description

9.1 Overview

The TXS0108E-Q1 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A-port accepts I/O voltages ranging from 1.4 V to 3.6 V. The B-port accepts I/O voltages from 1.65 V to 5.5 V. The device uses pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. The pull-up resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

9.2 Functional Block Diagram

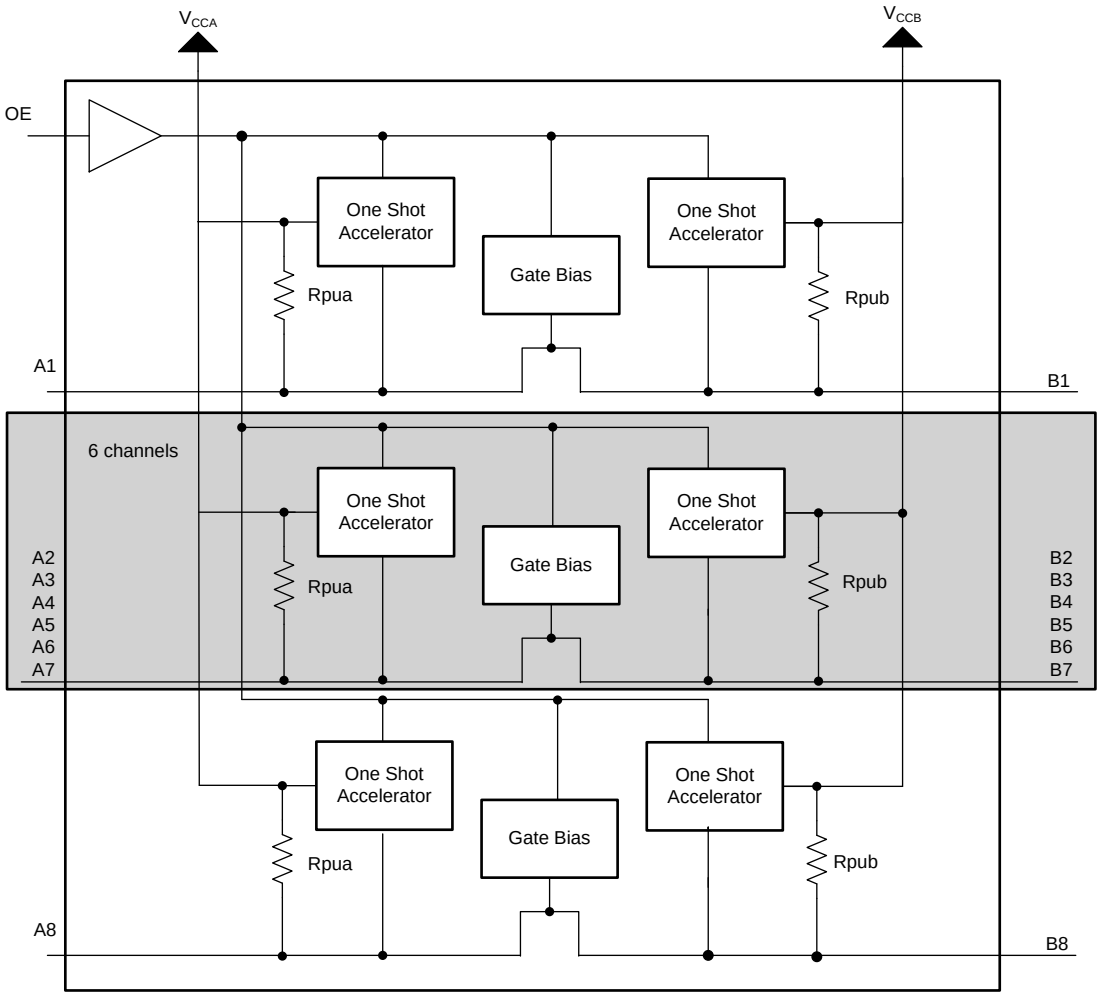


Figure 11. Functional Block Diagram

Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40 kΩ when the output is driving low. R_{PUA} and R_{PUB} have a value of 4 kΩ when the output is driving high. R_{PUA} and R_{PUB} are disabled when OE = Low.

9.3 Feature Description

9.3.1 Architecture

Figure 12 describes semi-buffered architecture design this application requires for both push-pull and open-drain mode. This application uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high edges), a high-on-resistance N-channel pass-gate transistor (on the order of 300 Ω to 500 Ω) and pull-up resistors (to provide DC-bias and drive capabilities) to meet these requirements. This design needs no direction-control signal (to control the direction of data flow from A to B or from B to A). The resulting implementation supports both low-speed open-drain operation as well as high-speed push-pull operation.

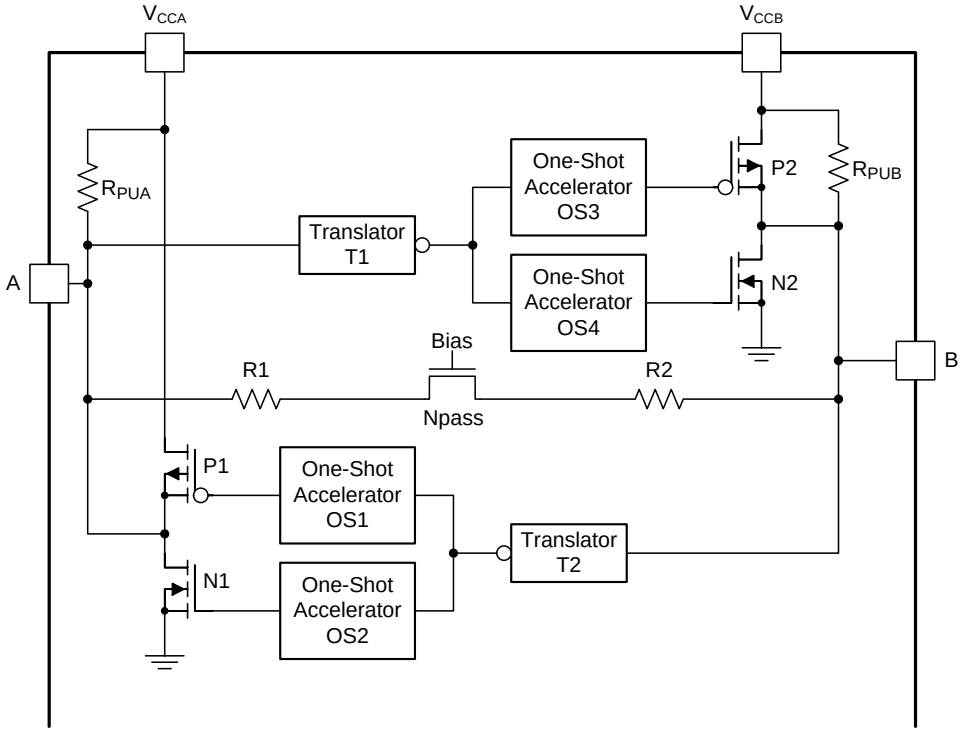


Figure 12. Architecture of a TXS0108E-Q1 Cell

When transmitting data from A-ports to B-ports, during a rising edge the one-shot circuit (OS3) turns on the PMOS transistor (P2) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from A to B, the one-shot circuit (OS4) turns on the N-channel MOSFET transistor (N2) for a short-duration which speeds up the high-to-low transition. The B-port edge-rate accelerator consists of one-shot circuits OS3 and OS4. Transistors P2 and N2 and serves to rapidly force the B port high or low when a corresponding transition is detected on the A port.

When transmitting data from B- to A-ports, during a rising edge the one-shot circuit (OS1) turns on the PMOS transistor (P1) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from B to A, the one-shot circuit (OS2) turns on NMOS transistor (N1) for a short-duration and this speeds up the high-to-low transition. The A-port edge-rate accelerator consists of one-shots OS1 and OS2, transistors P1 and N1 components and form the edge-rate accelerator and serves to rapidly force the A port high or low when a corresponding transition is detected on the B port.

Feature Description (continued)

9.3.2 Input Driver Requirements

The continuous DC-current *sinking* capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TXS0108E-Q1 I/O pins. Because the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest DC-current *sourcing* capability of hundreds of micro-amperes, as determined by the internal pull-up resistors.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge-rate and output impedance of the external device driving TXS0108E-Q1 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

9.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one-shot triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The one-shot circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The one-shot duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance of the TXS0108E-Q1 output. Therefore, TI recommends that this lumped-load capacitance is considered in order to avoid one-shot retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

9.3.4 Enable and Disable

The TXS0108E-Q1 has an OE pin input that is used to disable the device by setting the OE pin low, which places all I/Os in the Hi-Z state. The disable time (t_{dis}) indicates the delay between the time when the OE pin goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the design must allow for the one-shot circuitry to become operational after the OE pin goes high.

9.3.5 Pull-up or Pull-down Resistors on I/O Lines

The TXS0108E-Q1 has the smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40 kΩ when the output is driving low. R_{PUA} and R_{PUB} have a value of 4 kΩ when the output is driving high. R_{PUA} and R_{PUB} are disabled when OE = Low. This feature provides lower static power consumption (when the I/Os are passing a low), and supports lower V_{OL} values for the same size pass-gate transistor, and helps improve simultaneous switching performance.

9.4 Device Functional Modes

The TXS0108E-Q1 device has two functional modes, enabled and disabled. To disable the device set the OE pin input low, which places all I/Os in a high impedance state. Setting the OE pin input high enables the device.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TXS0108E-Q1 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The device is ideal for use in applications where an open-drain driver is connected to the data I/Os. The device is appropriate for applications where a push-pull driver is connected to the data I/Os, but the TXB0104 device, (SCES650) *4-Bit Bidirectional Voltage-Level Translator* might be a better option for such push-pull applications. The device is a semi-buffered auto-direction-sensing voltage translator design is optimized for translation applications (for example, MMC Card Interfaces) that require the system to start out in a low-speed open-drain mode and then switch to a higher speed push-pull mode.

10.2 Typical Application

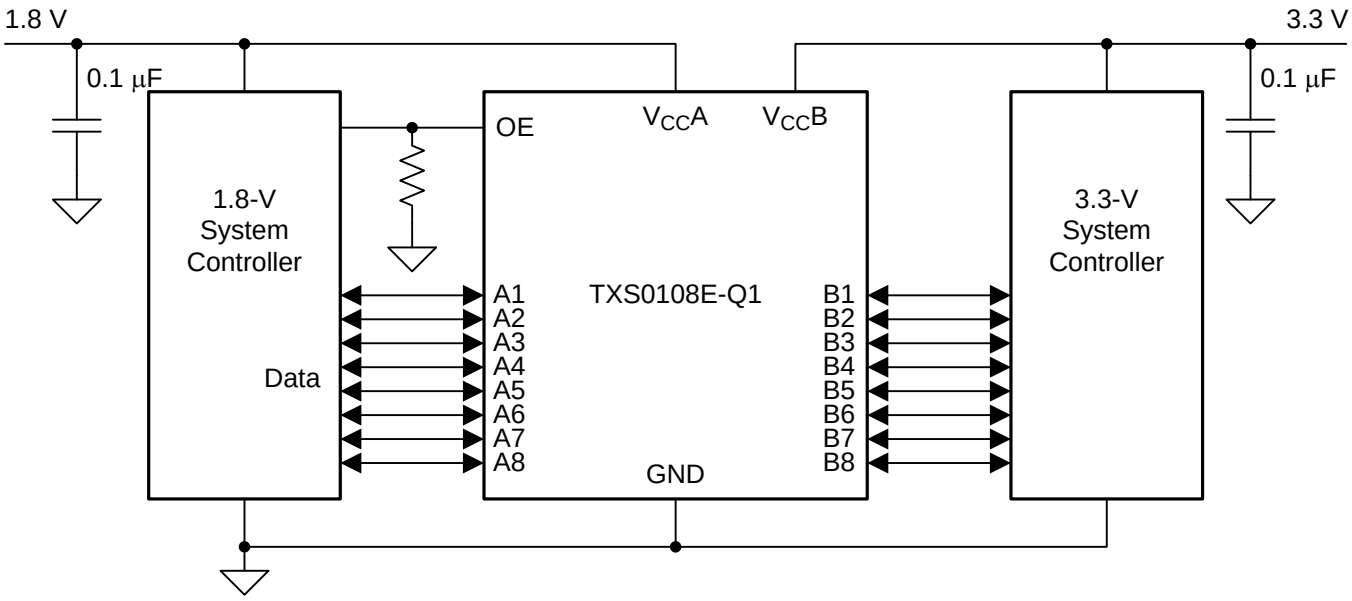


Figure 13. Typical Application Circuit

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 1. Ensure that $V_{CCA} \leq V_{CCB}$.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.4 V to 3.6 V
Output voltage range	1.65 V to 5.5 V

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

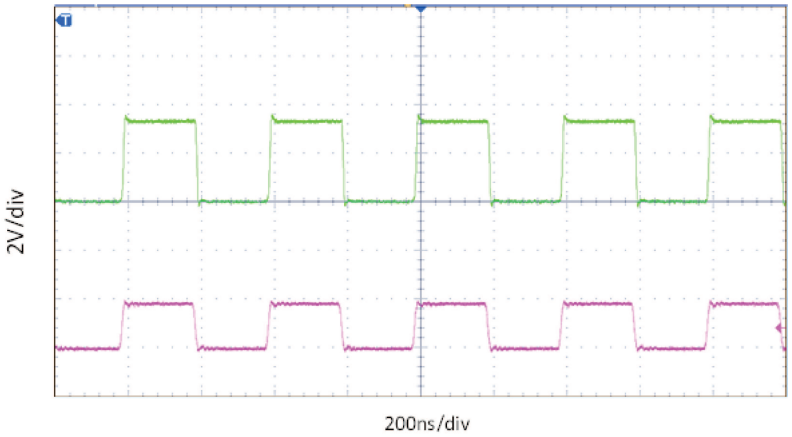
- Input voltage range
  - Use the supply voltage of the device that is driving the TXS0108E-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low

the value must be less than the V_{IL} of the input port.

- Output voltage range
  - Use the supply voltage of the device that the TXS0108E-Q1 device is driving to determine the output voltage range.
  - The TXS0108E-Q1 device has smart internal pull-up resistors. External pull-up resistors can be added to reduce the total RC of a signal trace if necessary.
- An external pull-down resistor decreases the output VOH and VOL. Use Equation 1 to calculate the VOH as a result of an external pull-down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4\ k\Omega) \quad (1)$$

10.2.3 Application Curves



V_{CCA} = 1.8 V V_{CCB} = 3.3 V

Figure 14. Level-Translation of a 2.5-MHz Signal

11 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pull-down resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pull-down resistor to ground is determined by the current-sourcing capability of the driver.

12 Layout

12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB pin and GND pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver.

12.2 Layout Example

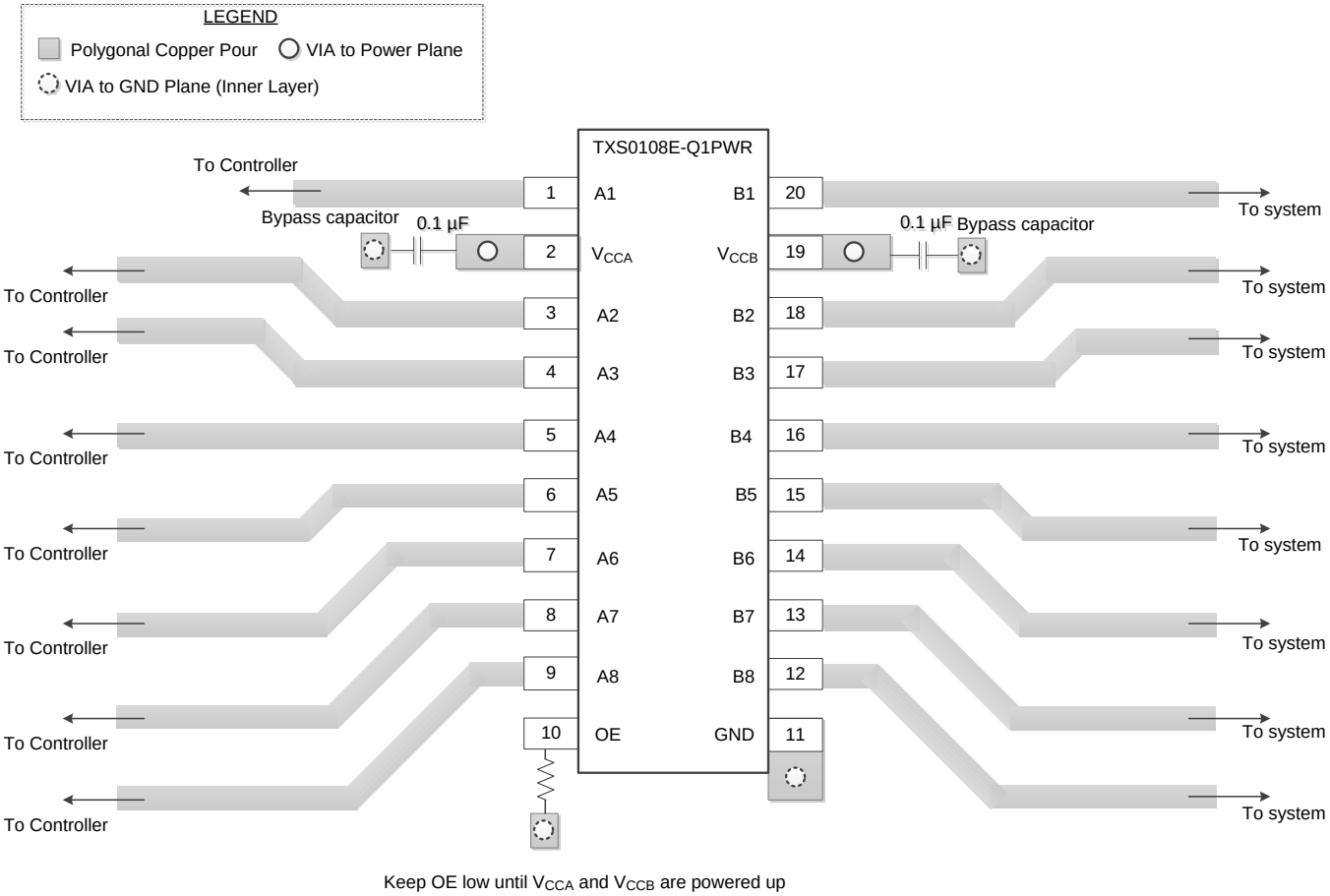


Figure 15. Layout Example

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

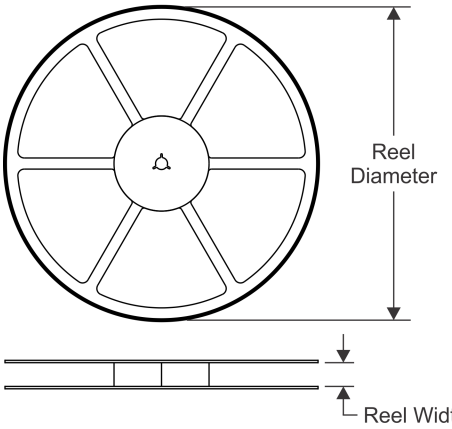
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

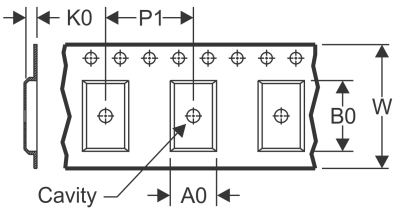
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

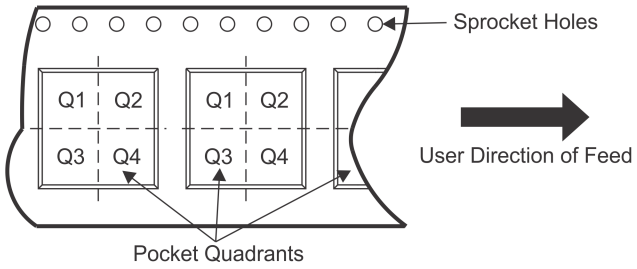


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

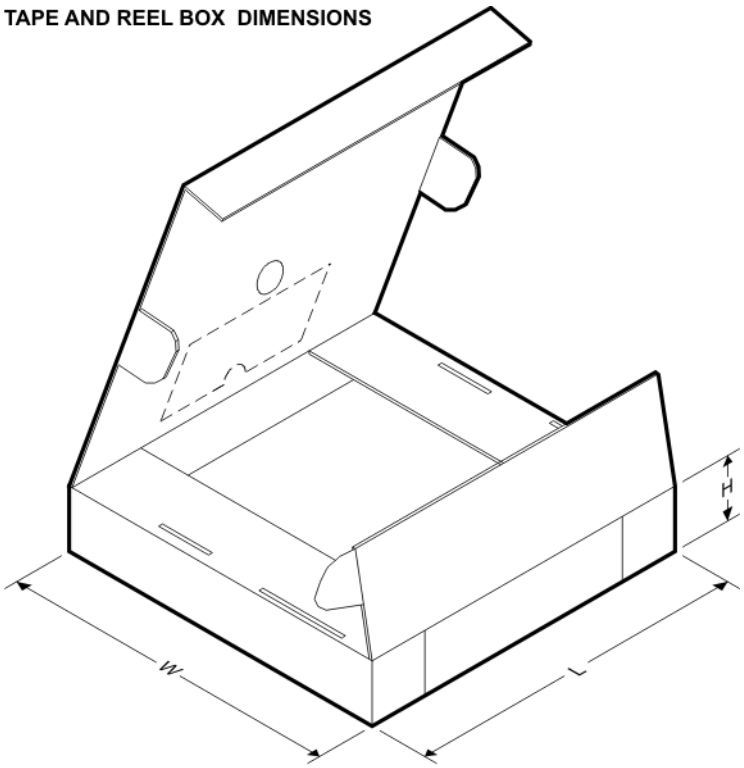
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0108EQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0108EQPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS0108EQPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YF08EQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TXS0108E-Q1 :

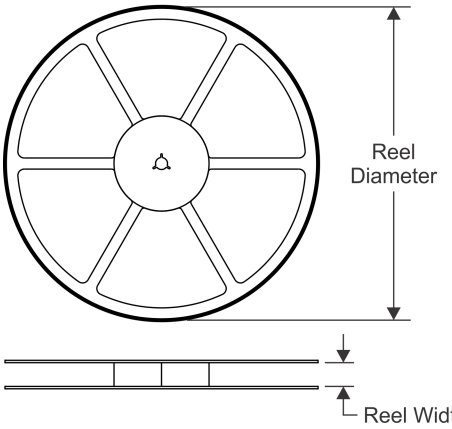
- Catalog: TXS0108E

NOTE: Qualified Version Definitions:

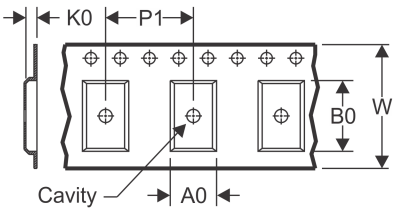
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

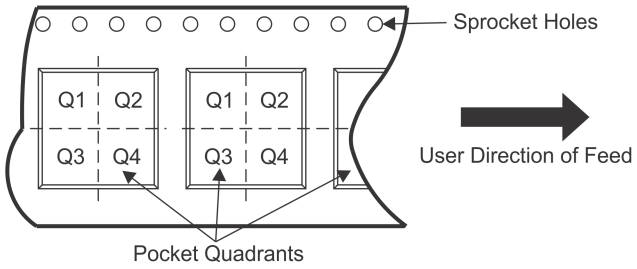


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

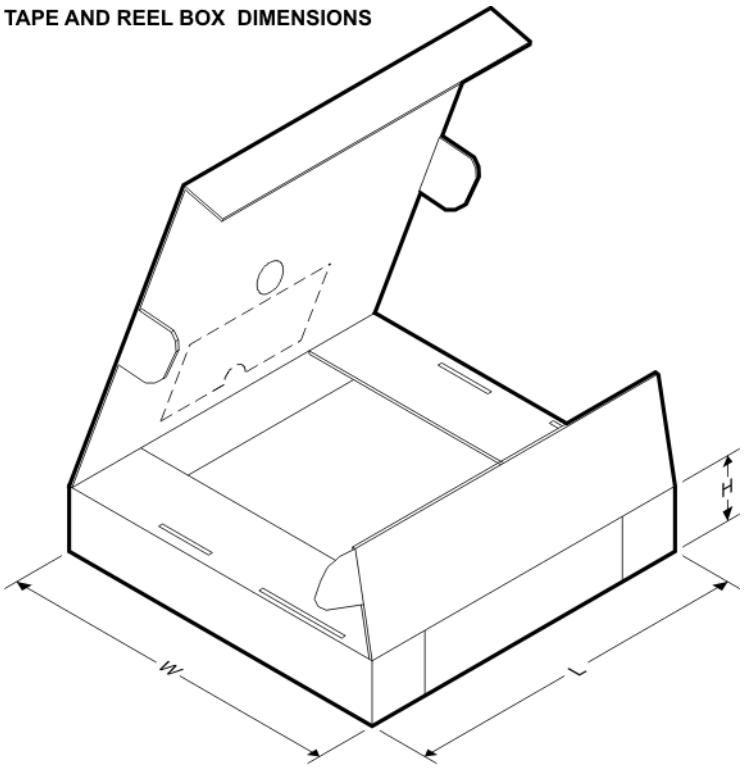
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0108EQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

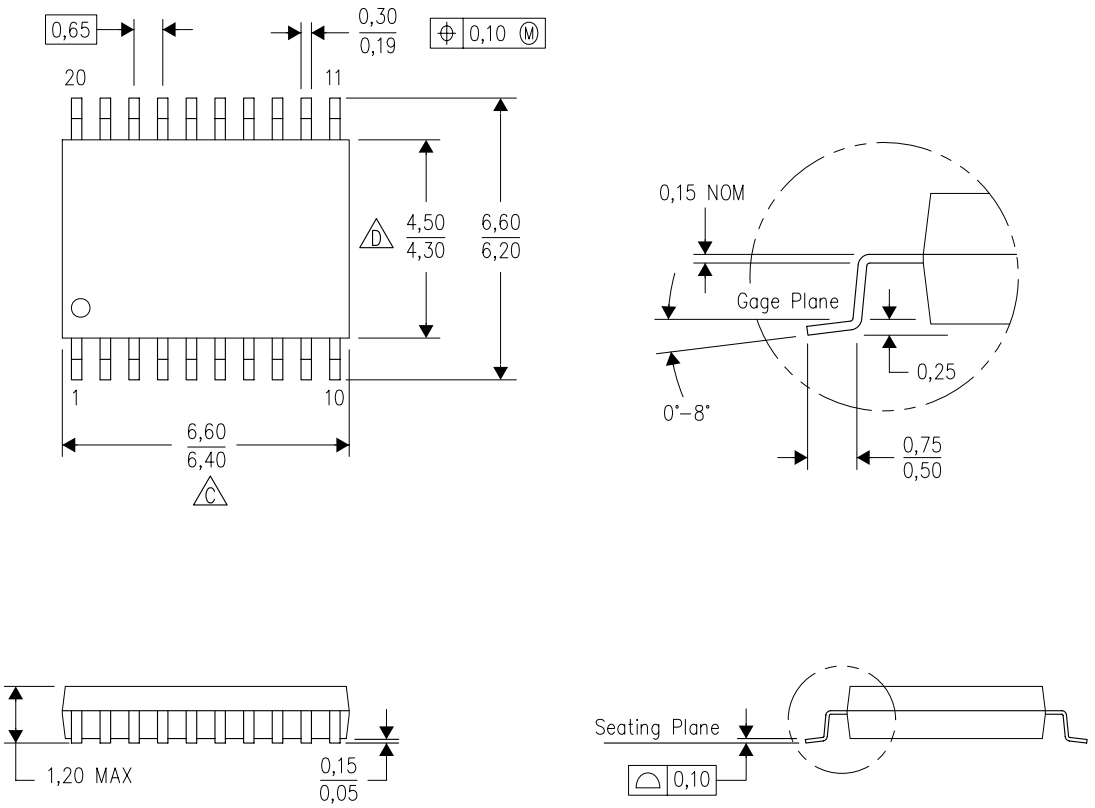
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0108EQPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



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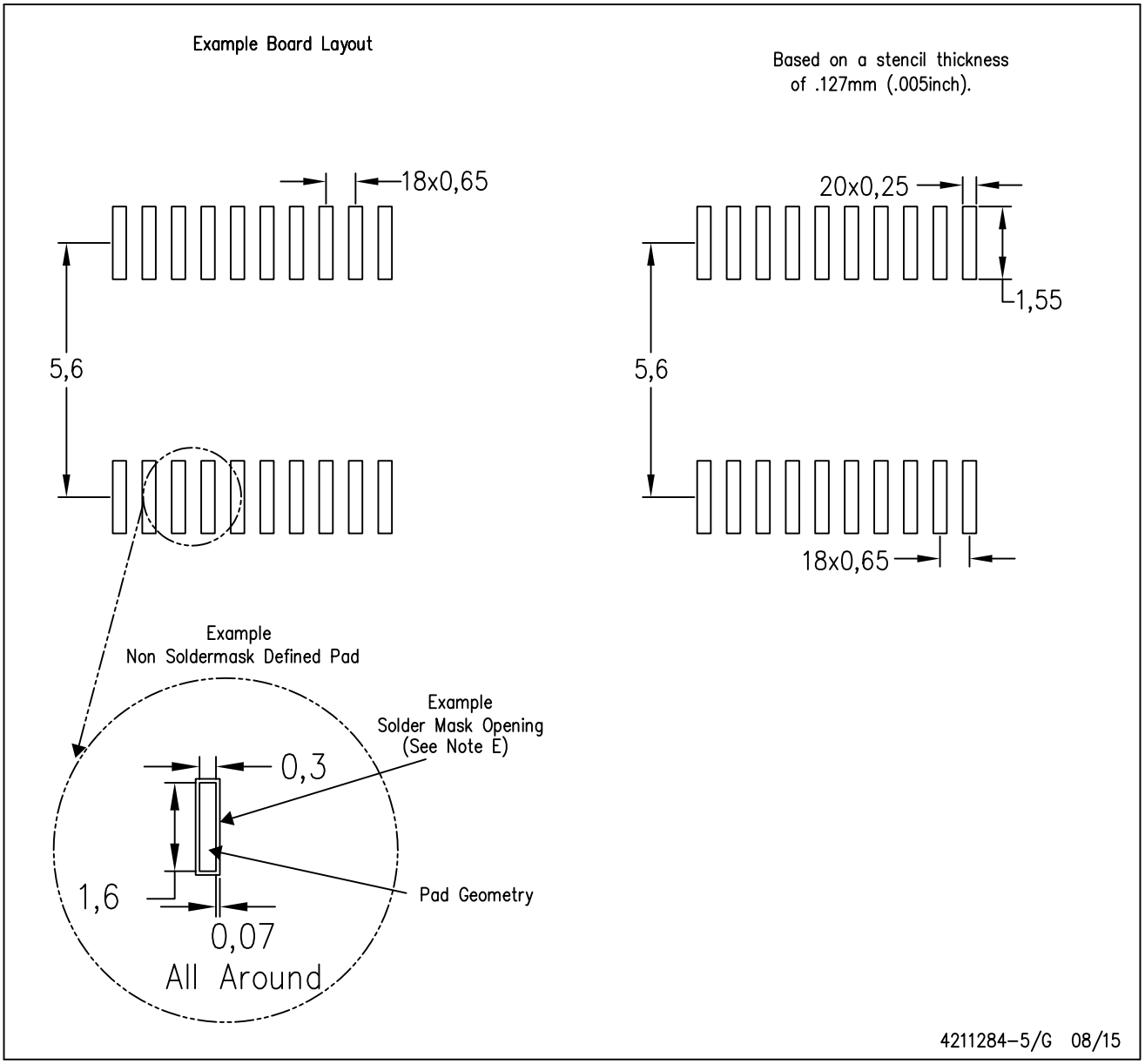
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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