74HC153; 74HCT153

Dual 4-input multiplexer

Rev. 9 — 14 January 2021

Product data sheet

1. General description

The 74HC153; 74HCT153 is a dual 4-input multiplexer. The device features independent enable inputs ($n\overline{E}$) and common data select inputs (S0 and S1). For each multiplexer, the select inputs select one of the four binary inputs and routes it to the multiplexer output (nY). A HIGH on \overline{E} forces the corresponding multiplexer outputs LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- · Input levels:
 - For 74HC153: CMOS level
 - For 74HCT153: TTL level
- Non-inverting outputs
- · Separate enable input for each output
- Common select inputs
- · Complies with JEDEC standard no. 7A
- · Permits multiplexing from n lines to 1 line
- Enable line provided for cascading (n lines to 1 line)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C.

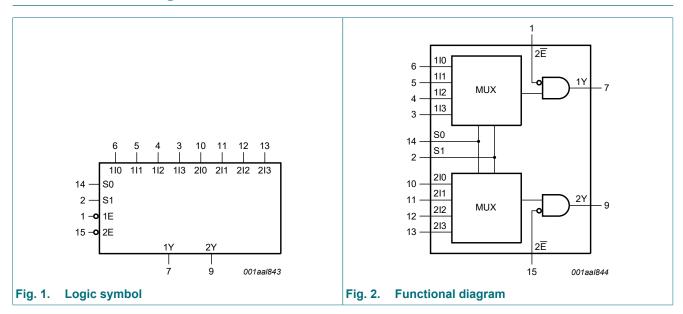
3. Ordering information

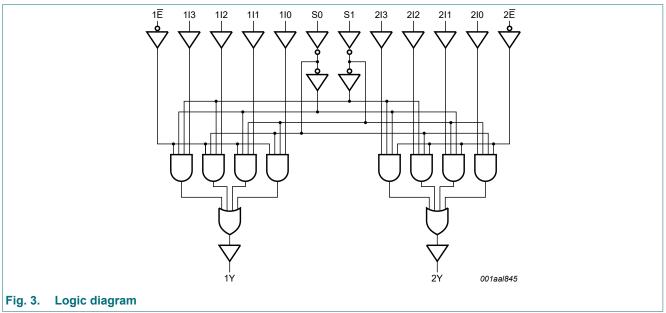
Table 1. Ordering information

Type number	Package				
	Temperature range	Name	Description	Version	
74HC153D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads;	SOT109-1	
74HCT153D			body width 3.9 mm		
74HC153DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1	
74HC153PW	4HC153PW -40 °C to +125 °C TSSOP16		plastic thin shrink small outline package;	SOT403-1	
74HCT153PW			16 leads; body width 4.4 mm		



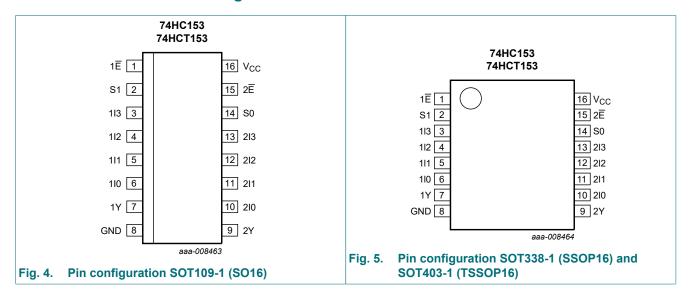
4. Functional diagram





5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Ē, 2Ē	1, 15	output enable inputs (active LOW)
S0, S1	14, 2	data select inputs
110, 111, 112, 113	6, 5, 4, 3	data inputs source 1
1Y	7	multiplexer output source 1
GND	8	ground (0 V)
2Y	9	multiplexer output source 2
210, 211, 212, 213	10, 11, 12, 13	data inputs source 2
Vcc	16	supply voltage

3 / 15

6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care.$

select In	puts	data inpi	uts			output enable	output
S0	S1	nI0	nl1	nl2	nI3	nΕ	nY
X	X	X	X	Х	Х	Н	L
L	L	L	Х	X	X	L	L
L	L	Н	X	Х	Х	L	Н
Н	L	X	L	Х	X	L	L
Н	L	X	Н	Х	Х	L	Н
L	Н	X	Х	L	X	L	L
L	Н	X	Х	Н	X	L	Н
Н	Н	X	Х	X	L	L	L
Н	Н	X	X	Х	Н	L	Н

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Io	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For SOT338-1 (SSOP16) package: P $_{\rm tot}$ derates linearly with 8.5 mW/K above 91 $^{\circ}\text{C}.$

For SOT403-1 (TSSOP16) package: Ptot derates linearly with 8.5 mW/K above 91 °C.

^[2] For SOT109-1 (SO16) package: Ptot derates linearly with 12.4 mW/K above 110 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		74HC153	3	7	4HCT15	3	Unit
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC153	3					1				
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_{O} = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_{O} = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_{O} = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	+125 °C	Unit
			Min Typ Max		Max	Min Max		Min	Max	
74HCT1	53								<u>'</u>	
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	Ι _O = -20 μΑ	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
I _I i	output voltage	I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1	-	±1	μA
Icc	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8	-	80	-	160	μΑ
ΔI _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V								
		1ln, 2ln	-	45	162	-	203	-	221	μA
		nĒ	-	60	216	-	270	-	294	μA
		Sn	-	135	486	-	608	-	662	μΑ
C _I	input capacitance			3.5	-	-	-	-	-	pF

6 / 15

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; for test circuit, see Fig. 8; unless otherwise specified

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC15	3		'				1		•	
t _{pd}	propagation delay	1In to nY, 2In to nY; [1] see Fig. 6								
		V _{CC} = 2.0 V	-	47	145	-	180	-	220	ns
		V _{CC} = 4.5 V	-	17	29	-	36	-	44	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	14	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	14	25	-	31	-	38	ns
		Sn to nY; see Fig. 7								
		V _{CC} = 2.0 V	-	50	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	18	30	-	38	-	45	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	14	26	-	33	-	38	ns
		nE to nY; see Fig. 7								
		V _{CC} = 2.0 V	-	33	100	-	125	-	150	ns
		V _{CC} = 4.5 V	-	12	20	-	25	-	30	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	10	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	10	17	-	21	-	26	ns
t_{t}	transition time	see <u>Fig. 6</u> [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	per package; [3] $V_1 = GND$ to V_{CC}	-	30	-	-	-	-	-	pF

7 / 15

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HCT1	53						1		·	
t _{PHL}	HIGH to LOW propagation	1In to nY, 2In to nY; [1] see Fig. 6								
	delay	V _{CC} = 4.5 V	-	19	34	-	43	-	51	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	16	-	-	-	-	-	ns
t _{PLH}	LOW to HIGH propagation	1In to nY, 2In to nY; [1] see Fig. 6								
	delay	V _{CC} = 4.5 V	-	13	24	-	30	-	36	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	16	-	-	-	-	-	ns
t _{pd}	propagation	Sn to nY; see Fig. 7 [1]								
	delay	V _{CC} = 4.5 V	-	20	34	-	43	-	51	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
		nE to nY; see Fig. 7 [1]								
		V _{CC} = 4.5 V	-	14	27	-	34	-	41	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
t _t	transition time	see <u>Fig. 6</u> [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	per package; [3] V _I = GND to V _{CC} - 1.5 V	-	30	-	-	-	-	-	pF

- t_{pd} is the same as t_{PHL} and t_{PLH}.
- t_t is the same as t_{THL} and t_{TLH} . C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f_i = input frequency in MHz;

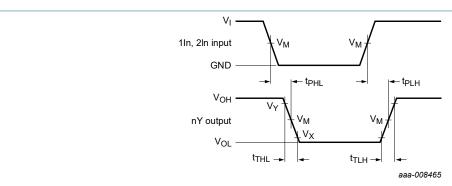
f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

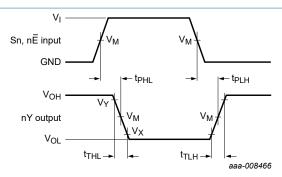
 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$



Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Waveforms showing the input (1In, 2In) to output (1Y, 2Y) propagation delays and output transition times Fig. 6.



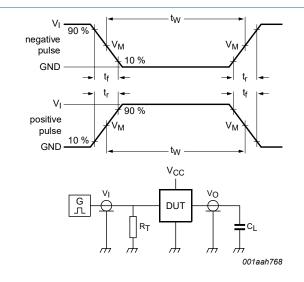
Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Waveforms showing the input (Sn, nE) to output (nY) propagation delays

Table 8. Measurement points

Туре	Input	Output	Output									
	V _M	V _M	V _Y									
74HC153	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}								
74HCT153	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}								



Test data is given in Table 9.

Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

Fig. 8. Test circuit for measuring switching times

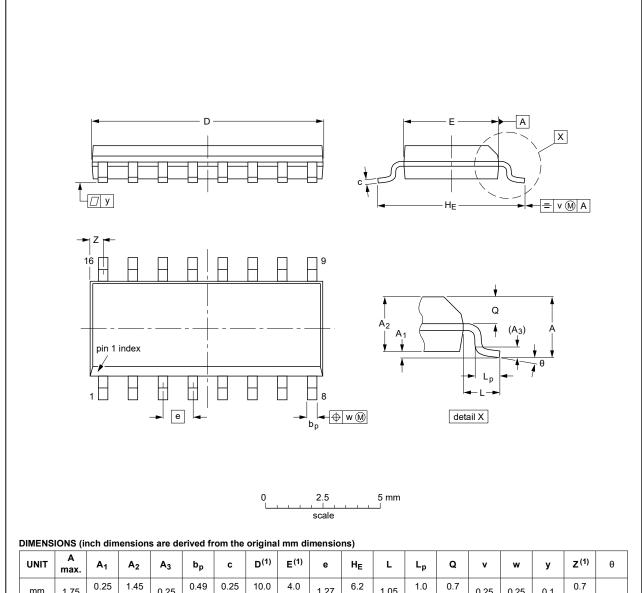
Table 9. Test data

Туре	Input		Load	Test
	VI	t _r , t _f	CL	
74HC153	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74HCT153	3.0 V	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075		0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN	ISSUE DATE
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig. 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

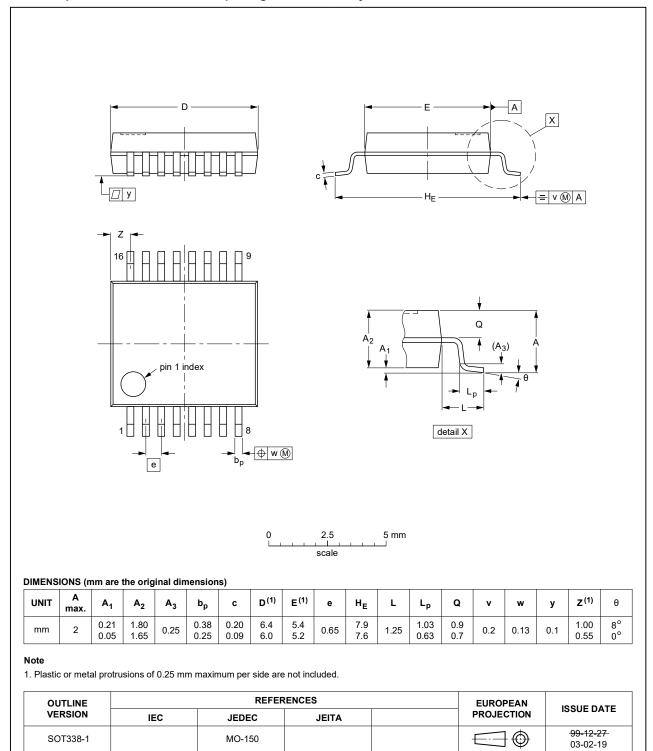
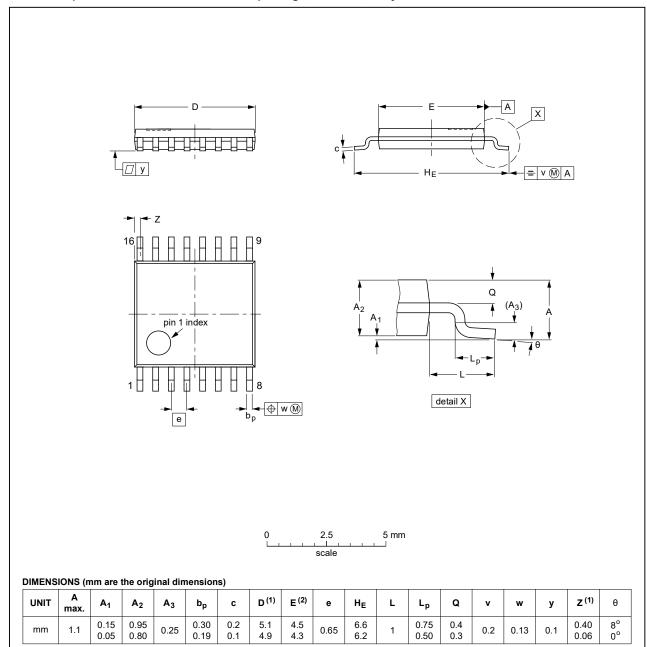


Fig. 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE	REFERENCES			EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT403-1		MO-153				99-12-27 03-02-18

Fig. 11. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT153 v.9	20210114	Product data sheet	-	74HC_HCT153 v.8
Modifications:	Type number	er 74HCT153DB (SOT338-	-1/SSOP16) remo	ved.
74HC_HCT153 v.8	20190813	Product data sheet	-	74HC_HCT153 v.7
Modifications:		ers 74HC153DB and 74HC rating values for P _{tot} total p	•	,
74HC_HCT153 v.7	20181010	Product data sheet	-	74HC_HCT153 v.6
Modifications:	guidelines o Legal texts	of this data sheet has beer of Nexperia. have been adapted to the l ers 74HC153DB and 74HC	new company nar	ne where appropriate.
74HC_HCT153 v.6	20160511	Product data sheet	-	74HC_HCT153 v.5
Modifications:	Type number	ers 74HC153N and 74HCT	153N (SOT38-4)	removed.
74HC_HCT153 v.5	20140123	Product data sheet	-	74HC_HCT153 v.4
Modifications:	• <u>Table 1</u> and	Section 11: all references	to 14 pin package	es removed.
74HC_HCT153 v.4	20131128	Product data sheet	-	74HC_HCT153 v.3
74HC_HCT153 v.3	20130722	Product data sheet	-	74HC_HCT153_CNV v.2
74HC_HCT153_CNV v.2	19970827	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1.	General description	1
2.	Features and benefits	1
3.	Ordering information	1
4.	Functional diagram	2
5.	Pinning information	3
5.1	l. Pinning	3
5.2	2. Pin description	3
6.	Functional description	4
7.	Limiting values	4
8.	Recommended operating conditions	5
9.	Static characteristics	5
10.	. Dynamic characteristics	7
11.	Package outline	10
12.	. Abbreviations	13
13.	. Revision history	13
14.	. Legal information	14

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74HCT153PW,112 74HCT153PW,118