TPD1E10B09 Single-Channel ESD Protection Device in 0402 Package

1 Features

- Provides System-Level ESD Protection for I/O Interfaces up to ±9 V
- IEC 61000-4-2 Level 4
  - ±20 kV (Air-Gap Discharge),
  - ±20 kV (Contact Discharge)
- IEC 61000-4-5 Surge Protection
  - 4.5 A (8/20 µs)
- I/O Capacitance 10 pF (Typical)
- R_{DYN} 0.5 Ω (Typical)
- DC Breakdown Voltage ±9.5 V (Minimum)
- Ultra Low Leakage Current 100 nA (Maximum)
- 13-V Clamping Voltage (Max at I_{PP} = 1 A)
- Industrial Temperature Range: –40°C to 125°C
- Space-Saving 0402 Footprint (1 mm × 0.6 mm × 0.5 mm)

2 Applications

- End Equipment:
  - Tablets
  - Remote Controllers
  - Wearables
  - Set-Top Boxes
  - Electronic Point of Sale (EPOS)
  - eBooks
- Interfaces:
  - Audio Lines
  - Push-buttons
  - General-Purpose Input and Output (GPIO)

3 Description

The TPD1E10B09 device is a single-channel electrostatic discharge (ESD) transient voltage suppression (TVS) diode in a small 0402 package. This ESD protection diode offers ±20 kV IEC 61000-4-2 (level 4) contact and air-gap ESD protection. The back-to-back TVS diode configuration allows for bipolar or bidirectional signal support. The 10-pF line capacitance is suitable for a wide range of applications supporting data rates up to 500 Mbps. The 0402 package is an industry standard and is convenient for component placement in space-constrained applications.

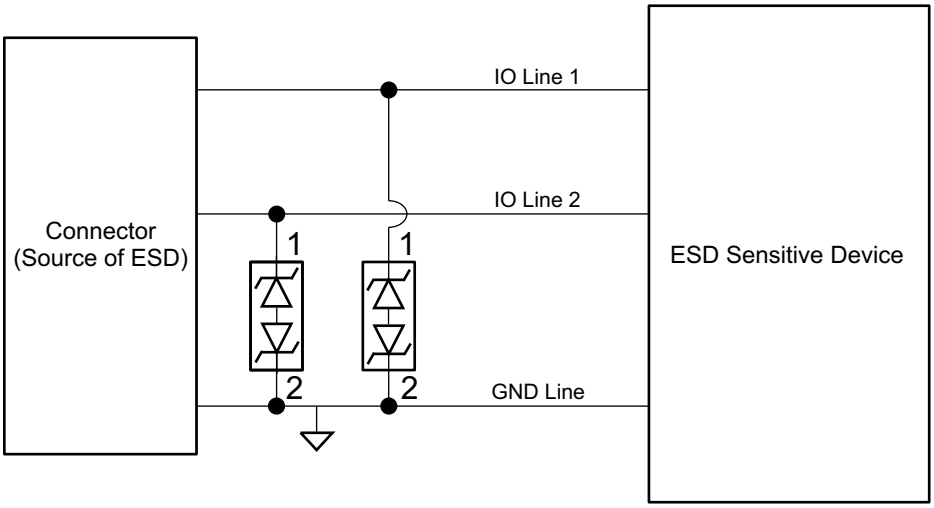
Typical applications of this ESD protection TVS diode are circuit protection for audio lines (microphone, earphone, and speaker phone), SD interfacing, keypad or other buttons, V_{BUS} pin and ID pin of USB ports, and general-purpose I/O ports. This ESD clamp is good for the protection of end equipment like eBooks, tablets, remote controllers, wearables, set-top boxes, and electronic point of sale equipment.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD1E10B09	X1SON (2)	0.60 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



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- Added capacitive measurement frequency ... 4

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- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (March 2012) to Revision B — **Page**

- Added THERMAL INFORMATION table. ... 4

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- Updated FEATURES. ... 1
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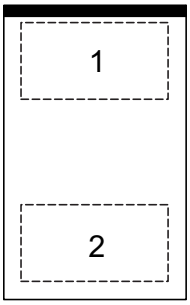
- Added APPLICATION INFORMATION section. ... 8

5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



Pin Functions

PIN	I/O	DESCRIPTION
1	I/O	ESD protected I/O
2		

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
	Operating temperature	–40	125	°C
I_{PP}	Peak pulse current (tp = 8/20 µs)		4.5	A
P_{PP}	Peak pulse power (tp = 8/20 µs)		90	W
T_{stg}	Storage temperature	–65	155	°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		IEC 61000-4-2 Contact Discharge	20000	
		IEC 61000-4-2 Air-Gap Discharge	20000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A		–40		125	°C
Operating voltage	Pin 1 to 2 or pin 2 to 1	–9		9	V

6.4 Thermal Information

THERMAL METRIC[1]		TPD1E10B09 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	615.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	404.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	493.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	127.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	493.3	°C/W
P	Power Dissipation[2]	162	mW

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Max junction temperature: 125°C; power dissipation calculated at 25°C ambient temperature using JEDEC High K board Standard. Not to be used for steady state power dissipation in the breakdown region.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	Pin 1 to 2 or pin 2 to 1			9	V
I_{LEAK}	Leakage current	Pin 1 = 5 V, pin 2 = 0 V			100	nA
VClamp1,2	Clamp voltage with ESD strike on pin 1, pin 2 grounded.	I_{PP} = 1 A, tp = 8/20 µSec[1]			13	V
		I_{PP} = 5 A, tp = 8/20 µSec[1]			17	
VClamp2,1	Clamp voltage with ESD strike on pin 2, pin 1 grounded.	I_{PP} = 1 A, tp = 8/20 µSec[1]			13	V
		I_{PP} = 4.5 A, tp = 8/20 µSec[1]			20	
R_{DYN}	Dynamic resistance	Pin 1 to pin 2[2]		0.5		Ω
		Pin 2 to pin 1[2]		0.5		
C_{IO}	I/O capacitance	V_{IO} = 2.5 V; *f* = 1 MHz		10		pF
$V_{BR1,2}$	Break-down voltage, pin 1 to pin 2	I_{IO} = 1 mA	9.5			V
$V_{BR2,1}$	Break-down voltage, pin 2 to pin 1	I_{IO} = 1 mA	9.5			V

(1) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics from I_{PP} = 10 A to I_{PP} = 20 A.

6.6 Typical Characteristics

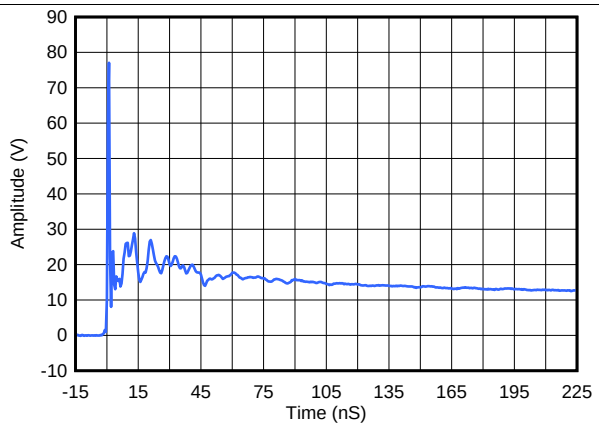


Figure 1. ESD Clamp Voltage +8 kV Contact ESD

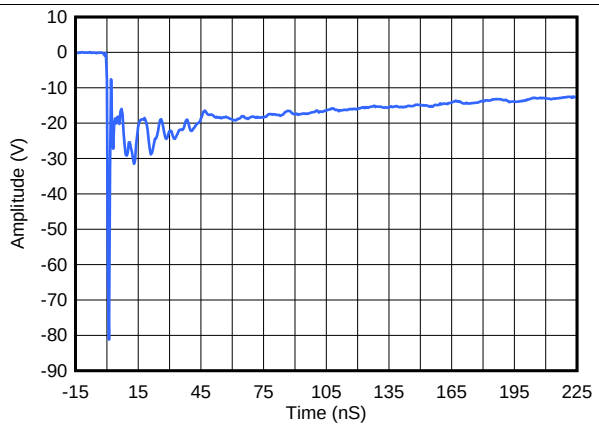


Figure 2. ESD Clamp Voltage –8 kV Contact ESD

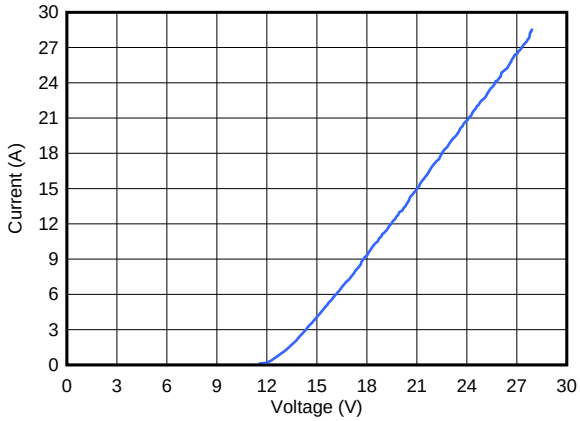


Figure 3. Transmission Line Pulse (TLP) Waveform Pin 1 to Pin 2

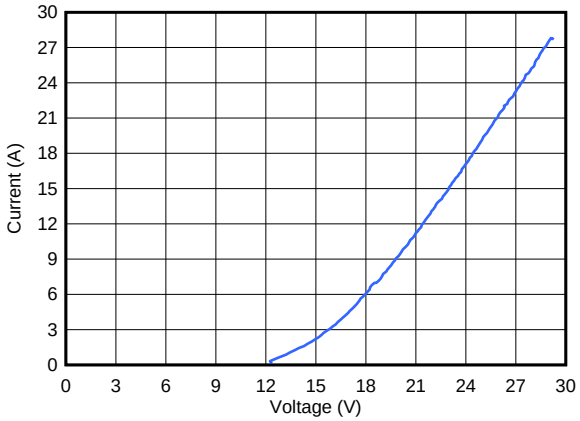


Figure 4. Transmission Line Pulse (TLP) Waveform Pin 2 to Pin 1

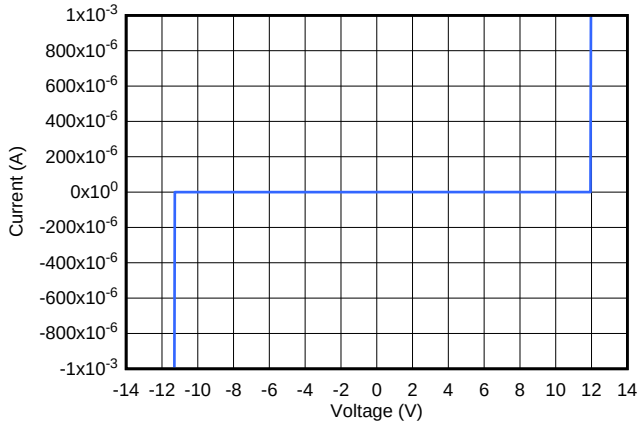


Figure 5. IV Curve

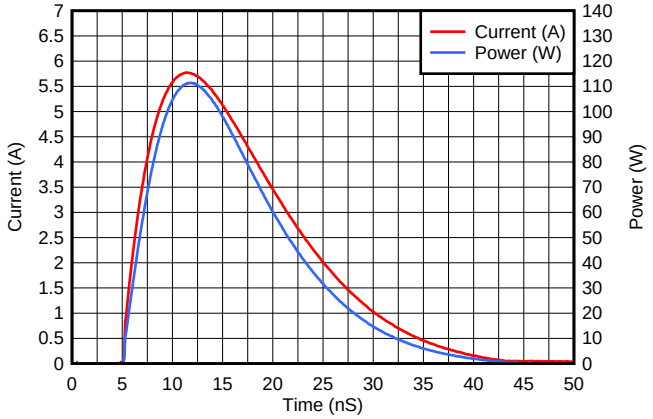


Figure 6. Positive Surge Waveform 8/20 µs

Typical Characteristics (continued)

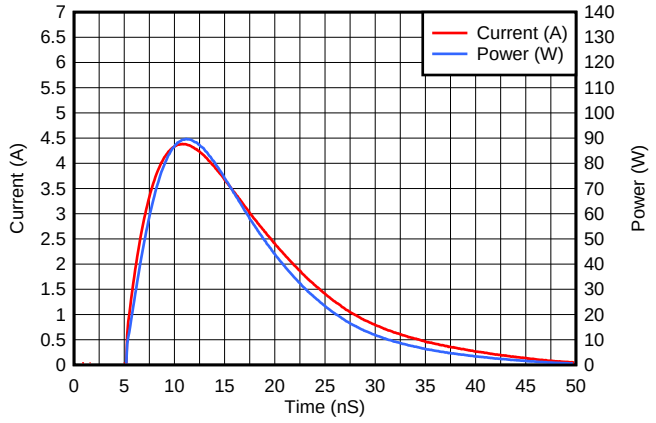


Figure 7. Negative Surge Waveform 8/20 µs

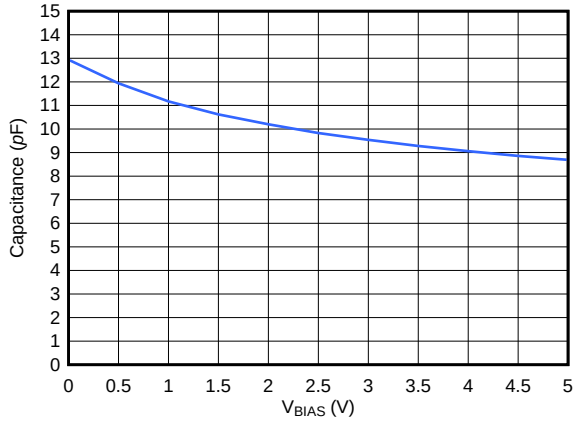


Figure 8. Pin Capacitance Across V_{BIAS}

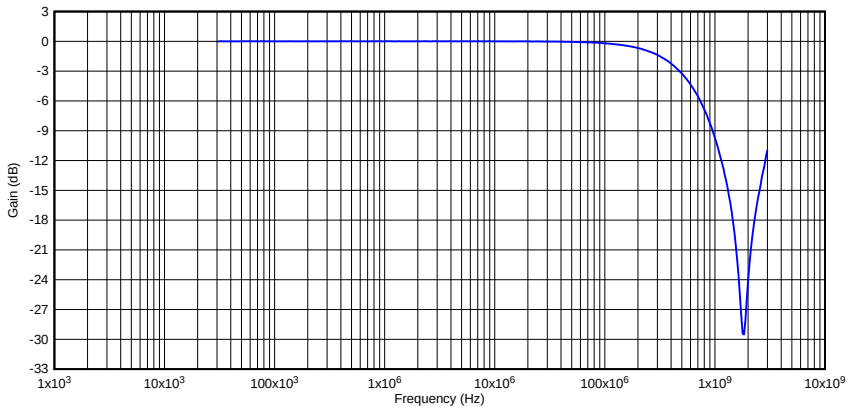


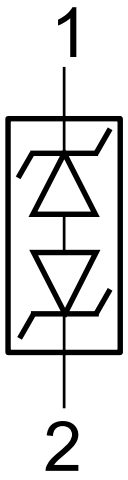
Figure 9. Insertion Loss

7 Detailed Description

7.1 Overview

TPD1E10B09 is a single-channel ESD TVS that provides ±20-kV IEC 61000-4-2 (Level 4) contact and air-gap ESD protection. The 10-pF back-to-back diode architecture is suitable for signals that range from –9 V to 9 V and supports data rates up to 500 Mbps. The industry-standard 0402 package is convenient for placement in applications with limited space.

7.2 Functional Block Diagram



7.3 Feature Description

TPD1E10B09 is a bidirectional TVS with high ESD protection level. This device protects circuit from ESD strikes up to ±20-kV contact and ±20-kV air-gap specified in the IEC 61000-4-2 level 4 international standard. The device can also handle up to 4.5-A surge current (IEC 61000-4-5 8/20 µs). The I/O capacitance of 10 pF supports a data rate up to 500 Mbps. This clamping device has a small dynamic resistance of 0.5 Ω typically. This makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 13 V when the device is taking 1-A transient current. The breakdown is bidirectional so that this protection device is a good fit for GPIO, especially audio lines which carry bidirectional signals. Low leakage allows the diode to conserve power when working below the V_{RWM}. The industrial temperature range of –40°C to 125°C makes this ESD device work at extensive temperatures in most environments. The space-saving 0402 package can fit into small electronic devices like mobile equipment and wearables.

7.4 Device Functional Modes

TPD1E10B09 is a passive clamp that has low leakage during normal operation when the voltage between pin 1 and pin 2 is below V_{RWM} and activates when the voltage between pin 1 and pin 2 goes above V_{BR}. During IEC ESD events, transient voltages as high as ±20 kV can be clamped between the two pins. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD1E10B09 is a single-channel back-to-back diode that protects one bidirectional signal line from electrostatic discharge and surge pulses. Because the diode is bidirectional, TPD1E10B09 protects signals that have positive or negative polarity. During normal operation, the diode behaves as a 10-pF capacitance to ground. Board layout is critical for optimal performance of any diode.

Placement: The diode should be placed very close to the external connector for optimal performance. Ideally, the diode should be placed on the line that it is protecting.

Layout: Pin 1 of the diode should be right over the protected signal line. There should a thick and short trace from pin 2 to ground. An example is shown in *Layout*.

8.2 Typical Application

A system with a human interface is vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these connectors. TPD1E10B09 is a single-channel ESD protection device containing back-to-back TVS diodes, which is typically used to provide a path to ground for dissipating ESD events on bidirectional signal lines between a human interface connector and a system. As the current from ESD passes through the device, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

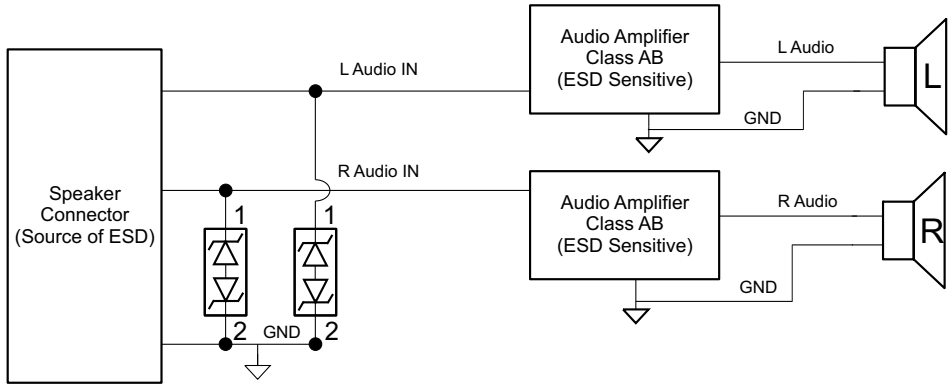


Figure 10. Typical Application Schematic

8.2.1 Design Requirements

For this design example, two TPD1E10B09s will be used to protect left and right audio channels. Table 1 lists the known system parameters for this audio application.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Audio Amplifier Class	AB
Audio signal voltage range	–8 V to 8 V
Audio frequency content	20 Hz to 20 kHz
Required IEC 61000-4-2 ESD Protection	±15-kV Contact/ ±15-kV Air-Gap

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer should make sure:

- The voltage range on the protected line does not exceed the reverse standoff voltage of the TVS diode(s) (V_{RWM}).
- The operating frequency is supported by the I/O capacitance, C_{IO}, of the TVS diode.
- The IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode.

For this application, the audio signal voltage range is –8 V to 8 V. The V_{RWM} for the TVS is –9.5 V to 9.5 V; therefore, the bidirectional TVS will not break down during normal operation, and normal operation of the audio signal will not be affected due to the signal voltage range. In this application, a bidirectional TVS like TPD1E10B09 is required.

Next, consider the frequency content of this audio signal. In this application with the class AB amplifier, the frequency content is from 20 Hz to 20 kHz; ensure that the TVS I/O capacitance will not distort this signal by filtering it. With TPD1E10B09 typical capacitance of 10 pF, which leads to a typical cutoff frequency of just under 500 MHz, this diode has sufficient bandwidth to pass the audio signal without distorting it.

Finally, the human interface in this application requires protection for ±15-kV Contact and ±15-kV Air-Gap ESD, which is above the standard Level 4 IEC 61000-4-2 system-level ESD protection. A standard TVS cannot survive this level of IEC ESD stress. However, TPD1E10B09 can survive at least ±20-kV Contact and ±20-kV Air-Gap ESD. Therefore, the device can provide sufficient ESD protection for the interface, even though the requirements are stringent. For any TVS diode to provide its full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will see during ESD events, it is crucial that a system designer uses proper board layout of their TVS ESD protection diodes. See *Layout* for instructions on properly laying out TPD1E10B09.

8.2.3 Application Curves

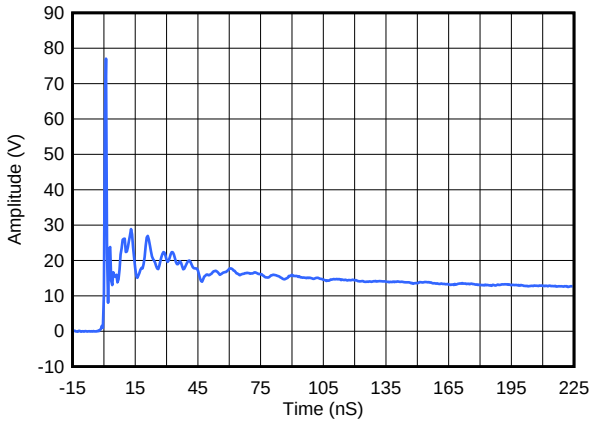


Figure 11. ESD Clamp Voltage +8-kV Contact ESD

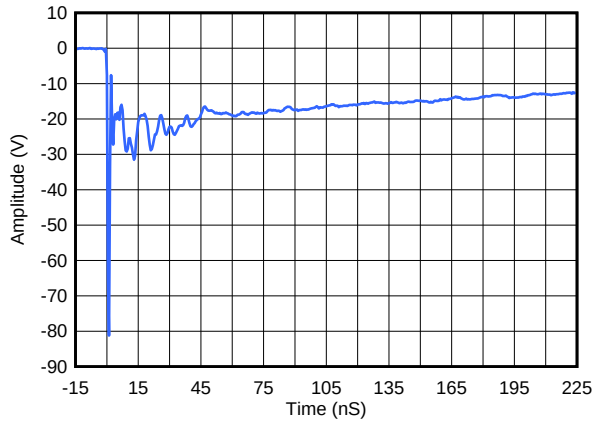


Figure 12. ESD Clamp Voltage –8-kV Contact ESD

9 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, so there is no need to power it. Do not violate the maximum specifications for each pin.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Use rounded corners with the largest radii possible on the protected traces between the TVS and the connector, thus eliminating any sharp corners.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or pin 2 is connected to ground, use a thick and short trace for this return path.

10.2 Layout Example

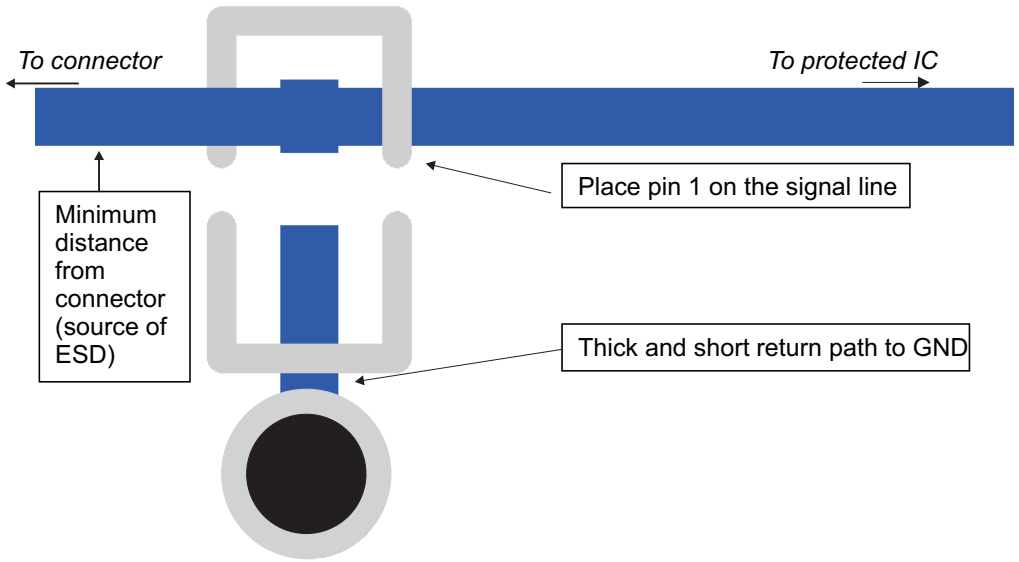


Figure 13. Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E10B09DPYR	ACTIVE	X1SON	DPY	2	10000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A1, A2, A6, BJ)	Samples
TPD1E10B09DPYT	ACTIVE	X1SON	DPY	2	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		(A1, A2, A6, BJ)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPD1E10B09 :

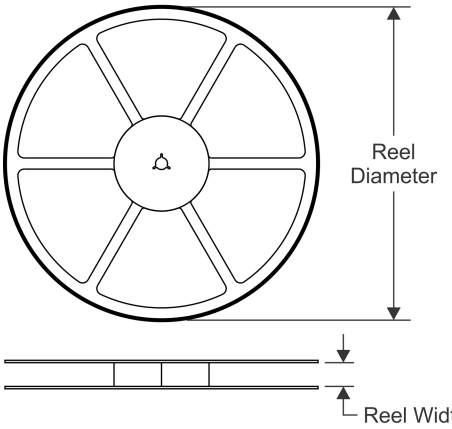
- Automotive: TPD1E10B09-Q1

NOTE: Qualified Version Definitions:

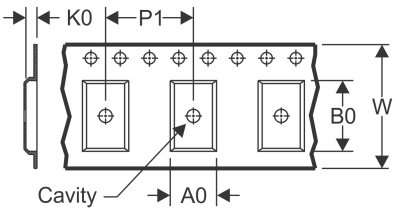
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

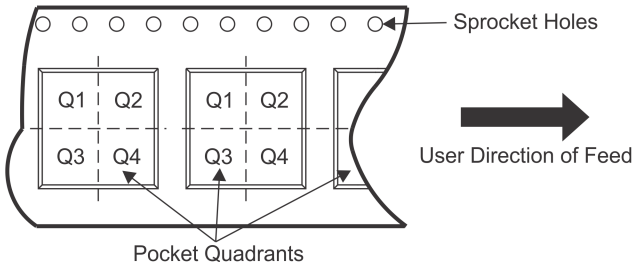


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

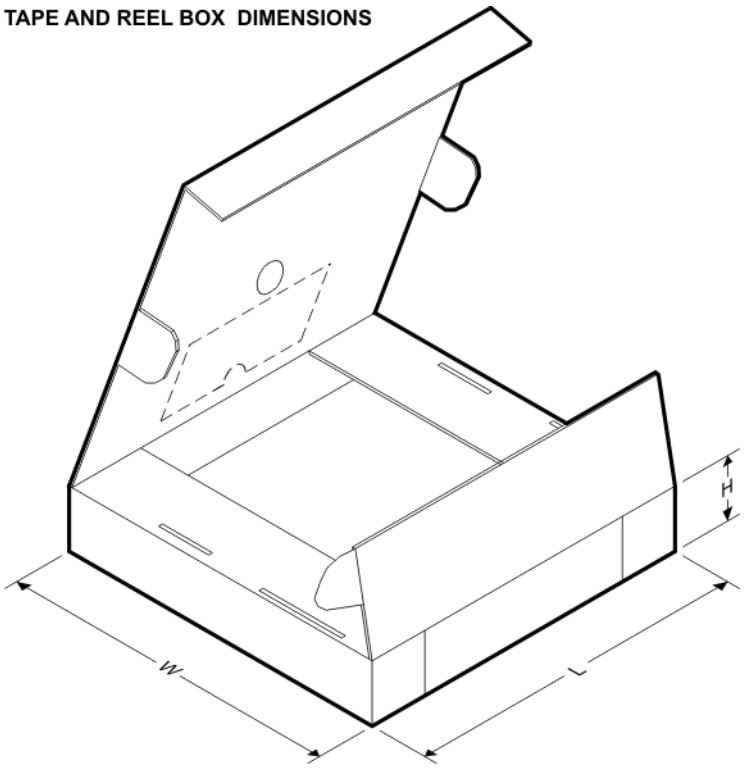
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E10B09DPYR	X1SON	DPY	2	10000	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E10B09DPYR	X1SON	DPY	2	10000	180.0	8.4	0.07	1.1	0.47	2.0	8.0	Q1
TPD1E10B09DPYR	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	180.0	8.4	0.07	1.1	0.47	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	180.0	9.5	0.72	1.12	0.43	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

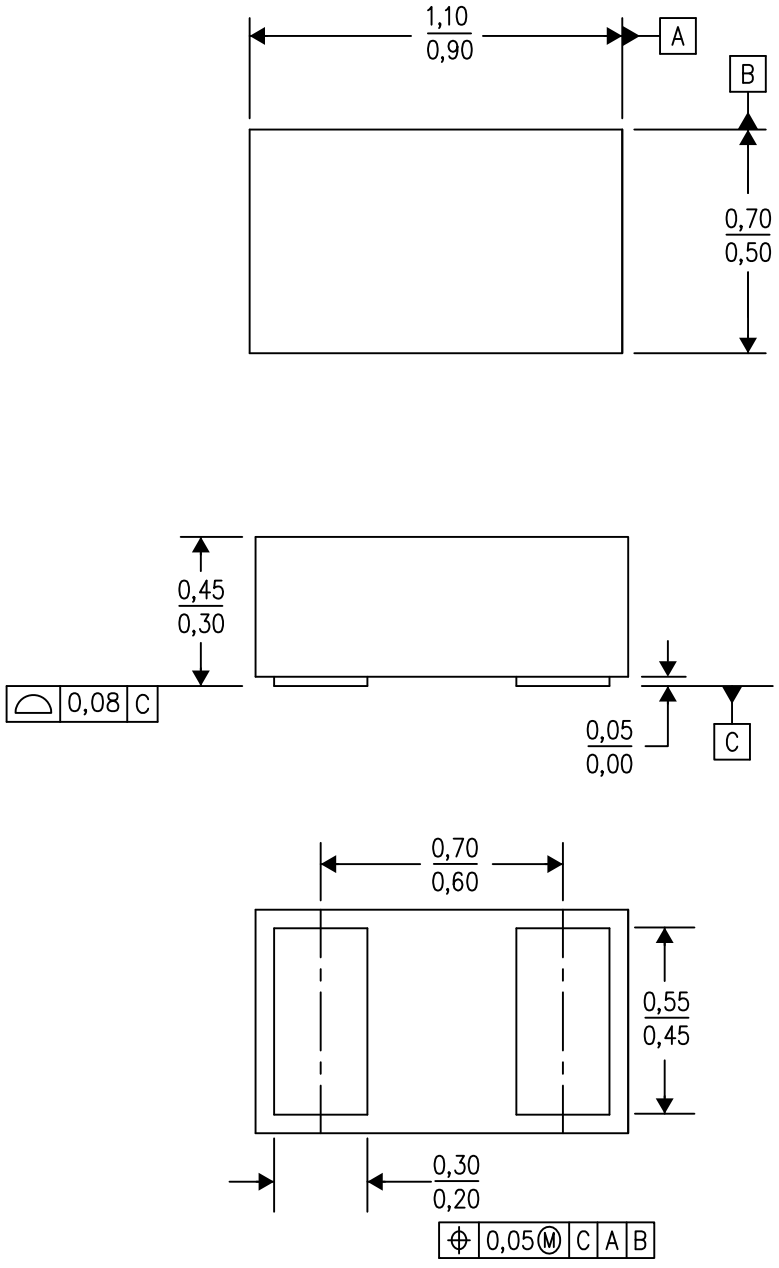
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E10B09DPYR	X1SON	DPY	2	10000	184.0	184.0	19.0
TPD1E10B09DPYR	X1SON	DPY	2	10000	203.2	196.8	33.3
TPD1E10B09DPYR	X1SON	DPY	2	10000	205.0	200.0	33.0
TPD1E10B09DPYT	X1SON	DPY	2	250	203.2	196.8	33.3
TPD1E10B09DPYT	X1SON	DPY	2	250	184.0	184.0	19.0
TPD1E10B09DPYT	X1SON	DPY	2	250	189.0	185.0	36.0
TPD1E10B09DPYT	X1SON	DPY	2	250	205.0	200.0	33.0

DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



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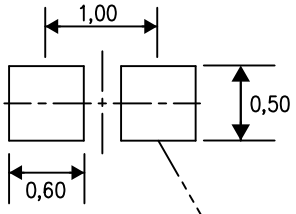
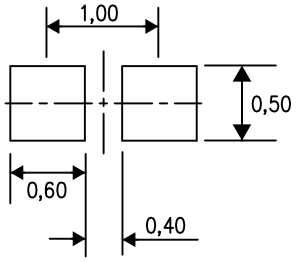
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

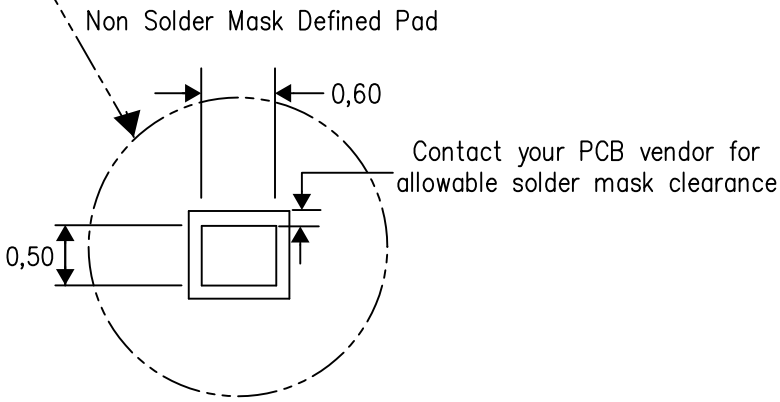
DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)





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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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